HI-7555/HI-C555

CMOS GENERAL PURPOSE TIMERS

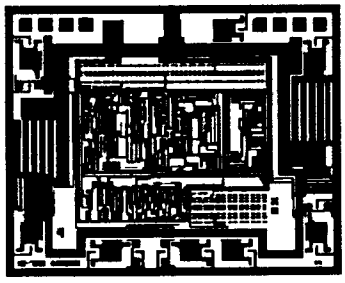
General Description

The HI-7555 and HI-C555 are highly stable CMOS devices capable of producing accurate time delays or frequencies. Terminals are provided for triggering or resetting the device as required. In the time delay mode of operation, the time is precisely controlled by one external resistor and a capacitor. In the oscillator mode, the free running frequency and duty cycle may be accurately controlled by two external resistors and a single external capacitor. The circuit is triggered or reset on the falling edge of the input waveforms.

Features

- Direct Replacement For SE555/NE555 Timers
- Extremely Low Power Consumption
  HI-7555 = 80 µA Typ.
  HI-C555 = 250 µA Typ.
- Power Supply Current Spike Suppression During Output Transitions
- 2V to 18V Single-Supply operation
- High Speed Operation HI-7555 = 500KHz Guaranteed
  HI-C555 = 2MHz Guaranteed
- Compatible With High Impedance Timing Elements
- Operates In Either The Astable Or Monostable Mode
- Adjustable Duty Cycle
- Fully Compatible CMOS\TTL\MOS Output
- Military Level Processing Available

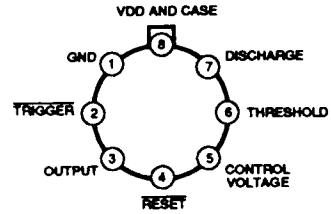
Chip Topography



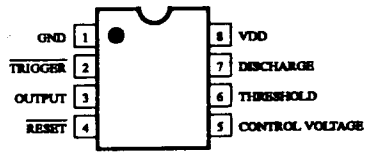
Applications

- Precision Timing
- Pulse Generation
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Sequential Timing
- Missing Pulse Detection
- Linear Ramp Generation

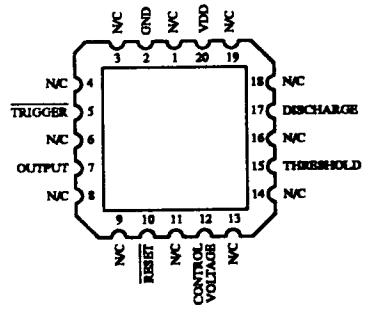
Pin Configurations



8 PIN TO-99



8 PIN DIP



20 PIN LEADLESS CHIP CARRIER (LCC)

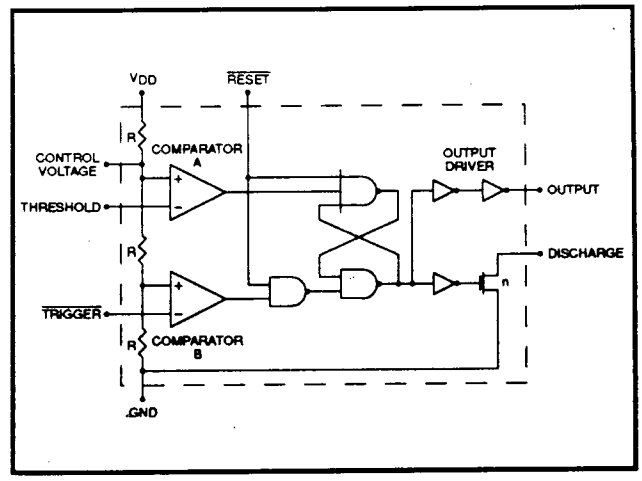
HOLT INC.
INTEGRATED CIRCUITS

Functional Description

Monostable Operation

The timer is configured as a one-shot in this mode of operation. Referring to figure 1, the external capacitor is initially held discharged by a transistor inside the timer. Upon application of a voltage less than the trigger level (1/3 V_{DD}) to the $\overline{\text{TRIGGER}}$ input, the latch is set which releases the short circuit across the external capacitor and drives the OUTPUT pin high. The voltage across the capacitor then increases exponentially with the time constant $t = R_A C_T$ until the voltage equals the threshold level (2/3 V_{DD}). The comparator then resets the latch which, in turn, rapidly discharges the capacitor and drives the OUTPUT pin to its low state. Once triggered, the circuit will remain in this state until the set time has elapsed, even if it is triggered again during this interval.

During monostable operation, the control voltage pin allows the trip voltage of the internal comparators to be externally controlled; thus, the pulse width can be controlled.



BLOCK DIAGRAM

Astable Operation

With the circuit configured as in figure 2 (pins 2 and 6 connected), the timer will trigger itself and run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. The frequency of operation may be determined by the equation:

$$\text{Frequency} = \frac{1.5}{(R_A + 2R_B)\,C_T}$$

The ratio of the two resistors sets the duty cycle per the equation:

$$\text{Duty Cycle} = \frac{R_B}{R_A + 2R_B}$$

High values of R and low values of C are recommended to minimize supply current consumption attributed to the external timing components.

Depending upon the voltage applied to the CONTROL VOLTAGE terminal, oscillation frequency modulation or suppression is possible.

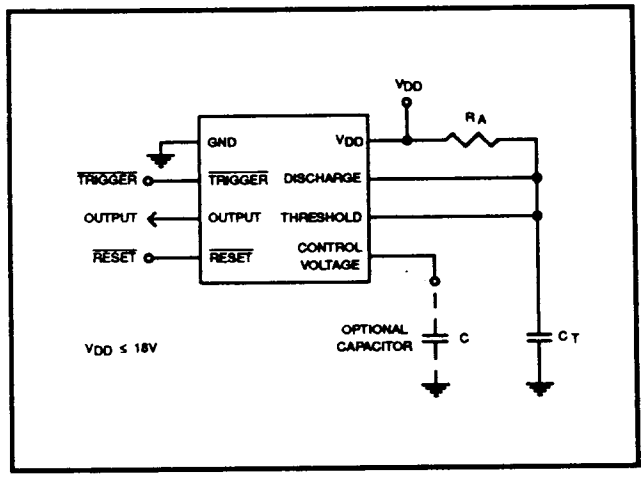


FIGURE 1. MONOSTABLE OPERATION

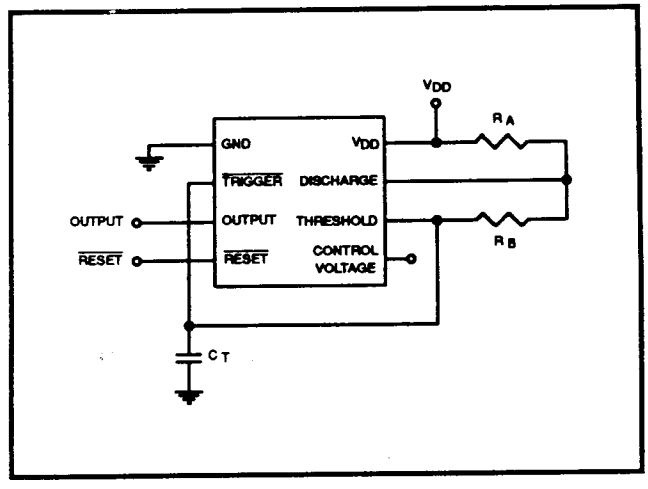


FIGURE 2. ASTABLE OPERATION

Truth Table

RESET	TRIGGER	THRESHOLD	OUTPUT	DISCHARGE TRANSISTOR
LOW	DON'T CARE	DON'T CARE	LOW	ON
HIGH	> 1/3 V_{DD}	> 2/3 V_{DD}	LOW	ON
HIGH	> 1/3 V_{DD}	< 2/3 V_{DD}	STABLE	STABLE
HIGH	< 1/3 V_{DD}	DON'T CARE	HIGH	OFF

NOTE: $\overline{\text{RESET}}$ overrides all other inputs. The $\overline{\text{TRIGGER}}$ input overrides THRESHOLD input.

Pin Descriptions

SYMBOL	FUNCTION	DESCRIPTION
GND	POWER	0.0V
$\overline{\text{TRIGGER}}$	INPUT	Sets internal latch when input is less than Trigger Voltage (≈ 1/3 V_{DD}).
OUTPUT	OUTPUT	Timer output
$\overline{\text{RESET}}$	INPUT	Resets internal latch which controls the OUTPUT and DISCHARGE outputs. Active Low.

SYMBOL	FUNCTION	DESCRIPTION
CONTROL VOLTAGE	INPUT	External control of Threshold and Trigger Voltages.
THRESHOLD	INPUT	Resets internal latch when THRESHOLD ≥ Threshold Voltage and $\overline{\text{TRIGGER}}$ ≥ Trigger Voltage.
DISCHARGE	OUTPUT	Single ended N-channel transistor. OUTPUT Low = On OUTPUT High = Hi-Impedence
V_{DD}	POWER	+ 2V TO + 18V

Absolute Maximum Ratings

– 55°C ≤ T_A ≤ +125°C, V_{DD} = +5V dc to +18V dc (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	HI-7555	HI-C555	UNIT
Supply Voltage	V_{DD}	DC Power Supply	18.0	18.0	V
Input Voltage Range	V_{IN}		≥ GND – 0.3 ≤ V_{DD} + 0.3	≥ GND – 0.3 ≤ V_{DD} + 0.3	V V
Output Sink Current	I_{SINK}		20.0	150.0	mA
Output Source Current	I_{SOURCE}		1.0	15.0	mA
Operating Temperature Range	T_A	Industrial Military	– 40 to + 85 – 55 to + 125	– 40 to + 85 – 55 to + 125	°C °C
Storage Temperature Range	T_{STG}	Industrial Military	– 50 to + 150 – 65 to + 150	– 50 to + 150 – 65 to + 150	°C °C
Lead Temperature		Soldering, 10 seconds	+ 300	+ 300	°C
Junction Temperature	T_J		+ 175	+ 175	°C
Power Dissipation	P_D	8 Pin TO-99 T_A = + 125°C 8 Pin DIP T_A = + 125°C 20 Pin Leadless Chip Carrier T_A = + 125°C	23 420 550	23 420 550	mW mW mW
Thermal Resistance, Junction - to - Case	$\varnothing_{JC}$	8 Pin TO-99 8 Pin DIP 20 Pin Leadless Chip Carrier	70 28 20	70 28 20	°C/W °C/W °C/W
Thermal Resistance, Junction - to - Ambient	$\varnothing_{JA}$	8 Pin TO-99 8 Pin DIP 20 Pin Leadless Chip Carrier	150 119 91	150 119 91	°C/W °C/W °C/W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

– 55°C ≤ T_A ≤ +125°C, V_{DD} = +2 to +18 Volts (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	HI-7555			HI-C555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Current	I_{DD}*	V_{DD} = 5V V_{DD} = 15V V_{DD} = 18V			300 300 350			700 1000 1000	µA µA µA
Trigger Voltage	V_{TR}	V_{DD} = 5V V_{DD} = 15V V_{DD} = 18V	1.30 4.30 5.20		1.80 4.80 5.80	1.30 4.30 4.20		1.80 4.80 5.80	V V V
Trigger Current	I_{TR}	V_{DD} = 5V +25°C ≤ T_A ≤ +125°C V_{DD} = 15V +25°C ≤ T_A ≤ +125°C V_{DD} = 18V +25°C ≤ T_A ≤ +125°C			± 50 ± 100 ± 100			± 50 ± 100 ± 100	nA nA nA
Threshold Voltage	V_{TH}	V_{DD} = 5V V_{DD} = 15V V_{DD} = 18V	2.90 9.20 11.00		3.40 9.70 11.60	2.90 9.20 11.00		3.40 9.70 11.60	V V V

* 1/3 V_{DD} ≤ V_{IN} ≤ 2/3 V_{DD}

DC Electrical Characteristics (cont.)

$-55°C \le T_A \le +125°C$, V_{DD} = +2 to +18 Volts (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	HI-7555			HI-C555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold Current	I_{TH}	V_{DD} = 5V, +25°C ≤ T_A ≤ +125°C			±50			±50	nA
		V_{DD} = 15V, +25°C ≤ T_A ≤ +125°C			±100			±100	nA
		V_{DD} = 18V, +25°C ≤ T_A ≤ +125°C			±100			±100	nA
High Level Output Voltage	V_{OH}	V_{DD} = 5V, I_{OH} = −1 mA				4.10			V
		V_{DD} = 15V, I_{OH} = −1 mA				14.20			V
		V_{DD} = 15V, I_{OH} = −5 mA				13.50			V
		V_{DD} = 15V, I_{OH} = −10 mA				12.50			V
		V_{DD} = 18V, I_{OH} = −1 mA				17.30			V
		V_{DD} = 5V, I_{OH} = −0.8 mA	3.80						V
		V_{DD} = 15V, I_{OH} = −0.8 mA	14.20						V
		V_{DD} = 18V, I_{OH} = −0.8 mA	17.30						V
Low Level Output Voltage	V_{OL}	V_{DD} = 5V, I_{OL} = 3.2 mA						0.40	V
		V_{DD} = 5V, I_{OL} = 5.0 mA						0.45	V
		V_{DD} = 5V, I_{OL} = 8.0 mA						0.60	V
		V_{DD} = 15V, I_{OL} = 10 mA						0.45	V
		V_{DD} = 15V, I_{OL} = 50 mA						1.50	V
		V_{DD} = 15V, I_{OL} = 100 mA						3.80	V
		V_{DD} = 18V, I_{OL} = 3.2 mA						0.40	V
		V_{DD} = 5V, I_{OL} = 3.2 mA		0.50					V
		V_{DD} = 15V, I_{OL} = 20 mA		1.25					V
		V_{DD} = 18V, I_{OL} = 20 mA		0.50					V
Discharge Transistor Leakage Current	I_{CEX}	V_{DD} = 5V, +25°C ≤ T_A ≤ +125°C		300				120	nA
		V_{DD} = 15V, +25°C ≤ T_A ≤ +125°C		300				120	nA
		V_{DD} = 18V, +25°C ≤ T_A ≤ +125°C		300				120	nA
Reset Current	I_R*	V_{DD} = 5V, +25°C ≤ T_A ≤ +125°C			±50			±50	nA
		V_{DD} = 15V, +25°C ≤ T_A ≤ +125°C			±100			±100	nA
		V_{DD} = 18V, +25°C ≤ T_A ≤ +125°C			±100			±100	nA
Discharge Transistor Saturation Voltage	V_{SAT}	V_{DD} = 5V, I_{OL} = 10 mA						0.60	V
		V_{DD} = 15V, I_{OL} = 100 mA						1.80	V
		V_{DD} = 18V, I_{OL} = 100 mA						1.60	V
		V_{DD} = 5V, I_{OL} = 10 mA		0.60					V
		V_{DD} = 15V, I_{OL} = 10 mA		0.60					V
		V_{DD} = 18V, I_{OL} = 10 mA		0.60					V
Reset Voltage Level	V_{RST}	+5V ≥ V_{DD} ≥ 18V	0.3		1.8	0.3		1.8	V
Control Voltage Level	V_{CV}	+5V ≥ V_{DD} ≥ 18V	61%		64%	61%		64%	V_{DD}

* 1/3 V_{DD} ≤ V_{IN} ≤ 2/3 V_{DD}

AC Electrical Characteristics

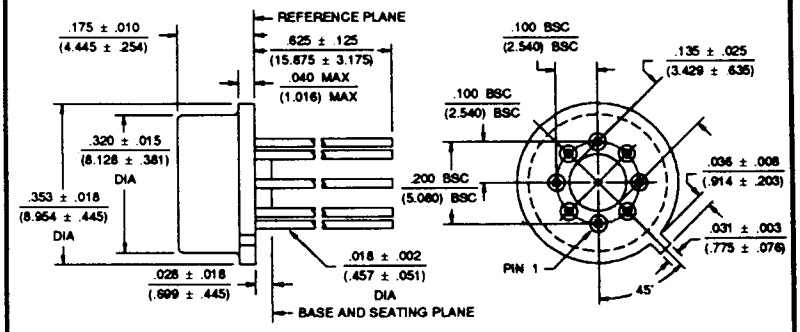
$-55°C \le T_A \le +125°C$, V_{DD} = +2 to +18 Volts (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	HI-7555			HI-C555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Monostable Timing Accuracy	t_{MON}	25°C	908		1110	908		1110	µs
		−55°C ≥ T_A ≥ +125°C	858		1161	858		1161	µs
		5V ≤ V_{DD} ≤ 15V, R_T = 10 kΩ, C_T = 0.1 µF, SEE FIGURE 1.							
Astable Timing Accuracy	t_{AST}	25°C	1818		2222	1818		2222	µs
		−55°C ≥ T_A ≥ +125°C	1717		2323	1717		2323	µs
		5V ≤ V_{DD} ≤ 15V, R_{TA} = 10 kΩ, R_{TB} = 10 kΩ, C_T = 0.1 µF, SEE FIGURE 2.							

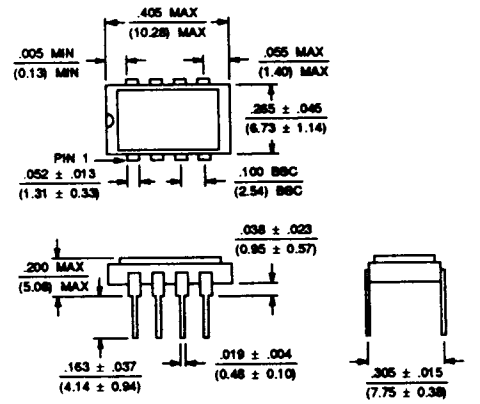
HI-7555/HI-C555 Standard Packaging

TERMINAL CONNECTIONS							
PIN	8 PIN TO-99	PIN	8 PIN DIP	PIN	20 PIN LEADLESS CHIP CARRIER (LCC)		
1	GND	1	GND	1	N/C	11	N/C
2	$\overline{\text{TRIGGER}}$	2	$\overline{\text{TRIGGER}}$	2	GND	12	CONTROL VOLTAGE
3	OUTPUT	3	OUTPUT	3	N/C	13	N/C
4	$\overline{\text{RESET}}$	4	$\overline{\text{RESET}}$	4	N/C	14	N/C
5	CONTROL VOLTAGE	5	CONTROL VOLTAGE	5	$\overline{\text{TRIGGER}}$	15	THRESHOLD
6	THRESHOLD	6	THRESHOLD	6	N/C	16	N/C
7	DISCHARGE	7	DISCHARGE	7	OUTPUT	17	DISCHARGE
8	V_{DD}	8	V_{DD}	8	N/C	18	N/C
				9	N/C	19	N/C
				10	$\overline{\text{RESET}}$	20	V_{DD}

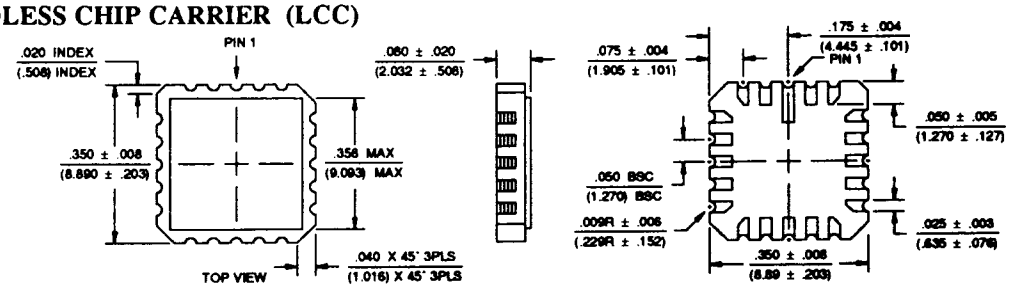
8 PIN TO-99



8 PIN DIP



20 PIN LEADLESS CHIP CARRIER (LCC)



Ordering Information

HI-7555T - TO-99, 8 pins, Industrial
HI-7555TM - TO-99, 8 pins, Military
HI-7555C - Ceramic DIP, 8 pins, Industrial
HI-7555CM - Ceramic DIP, 8 pins, Military
HI-7555S - Ceramic Chip Carrier (LCC), 20 pins, Industrial
HI-7555SM - Ceramic Chip Carrier (LCC), 20 pins, Military

HI-C555T - TO-99, 8 pins, Industrial
HI-C555TM - TO-99, 8 pins, Military
HI-C555C - Ceramic DIP, 8 pins, Industrial
HI-C555CM - Ceramic DIP, 8 pins, Military
HI-C555S - Ceramic Chip Carrier (LCC), 20 pins, Industrial
HI-C555SM - Ceramic Chip Carrier (LCC), 20 pins, Military

Additional packaging and screening options are available upon request.

Vender CAGE Number: 44270

HI-7555/HI-C555

NOTES:

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