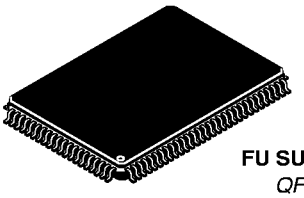
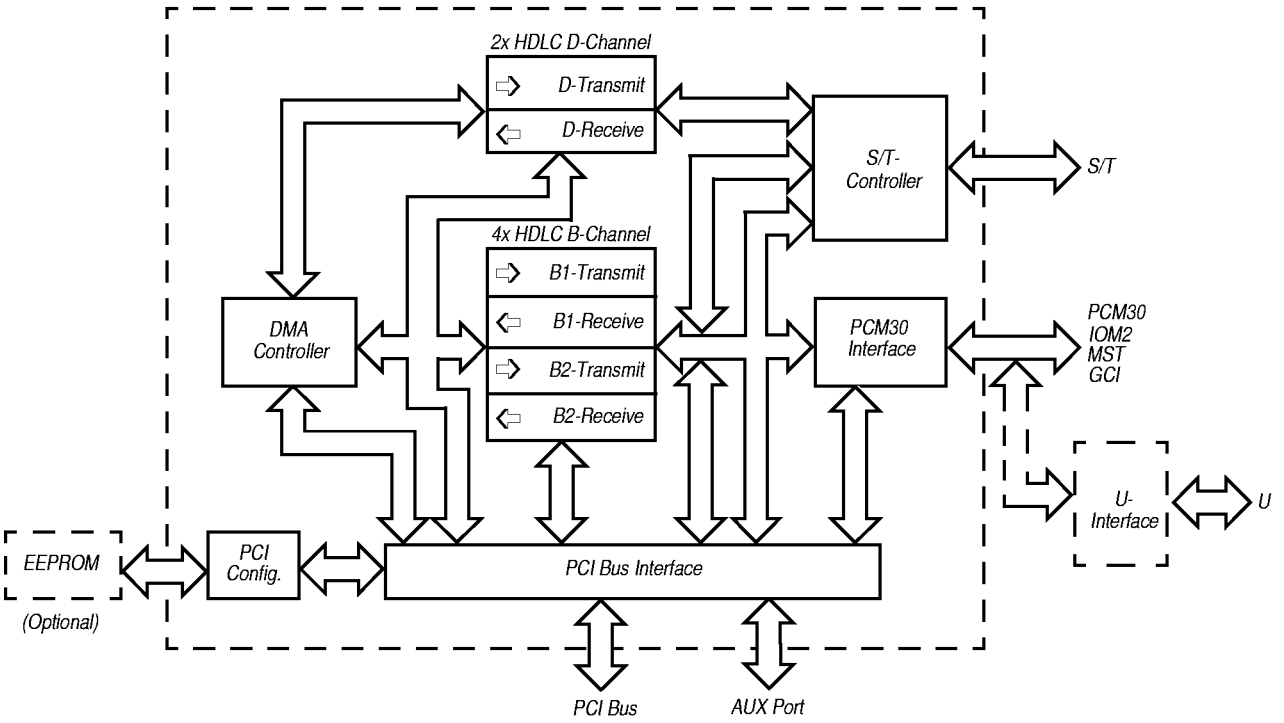
MC145575

ISDN S/T Transceiver with PCI Interface



FU SUFFIX
QFP
CASE 983A

ORDERING INFORMATION
MC145575FU *Quad Flat Package*



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SECTION 1
GENERAL DESCRIPTION

The MC145575 is an ISDN S/T HDLC basic rate controller for "passive" ISDN PC cards with integrated S/T interface and PCM30 highway interface. It is the first all-in-one solution for a PCI ISDN PC-card worldwide with power management and Windows 98™ support.

A 32 kbyte memory window of the PC is used for the deep FIFOs. An industrial standard serial interface for telecom peripheral ICs is also implemented. Codecs are normally connected to this interface.

1.1 FEATURES

- *Independent Read and Write HDLC-Channels for Two ISDN B-Channels and One ISDN D-Channel*
- *Independently Selectable B1- and B2-Channel Transparent Mode*
- *FIFO-Memory-Window: 4 x 7.5 kbyte (B-Channel) and 2 x 512 Byte (D-Channel)*
- *Maximum 31 HDLC Frames (B-Channel) and 15 HDLC Frames (D-Channel) per Channel and Direction in FIFO*
- *56 kbps Restricted Mode for US ISDN Lines Selectable*
- *I.430 ITU S/T ISDN Support in TE and NT Mode*
- *Supports ETSI Layer 1 ETR 300 012*
- *PCM30 Interface Configurable to Interface IOM2™ or GCI™ for Connection to Motorola U-Interface or Codecs*
- *Integrated PCI Specification Rev. 2.2 Bus Interface for 3.3 and 5 V Bus Signals*
- *Direct Access to PCM30 Interface for Tone Synthesis*
- *Complies with PCI Power Management Rev. 1.0*
- *3.3 and 5 V Supply Voltage*
- *Rectangular QFP 100-Pin Package*

1.2 APPLICATIONS

- *ISDN PCI PC Card*

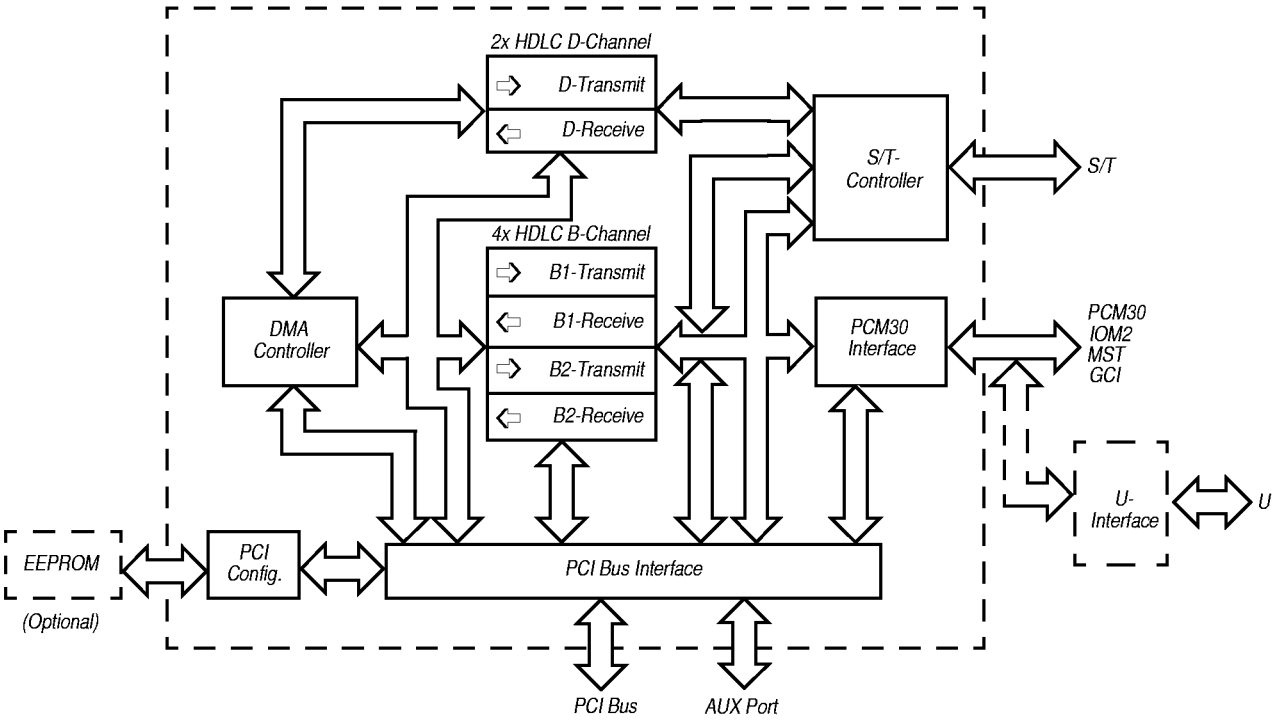


Figure 1–1. MC145575 Block Diagram

SECTION 2
PIN DESCRIPTION

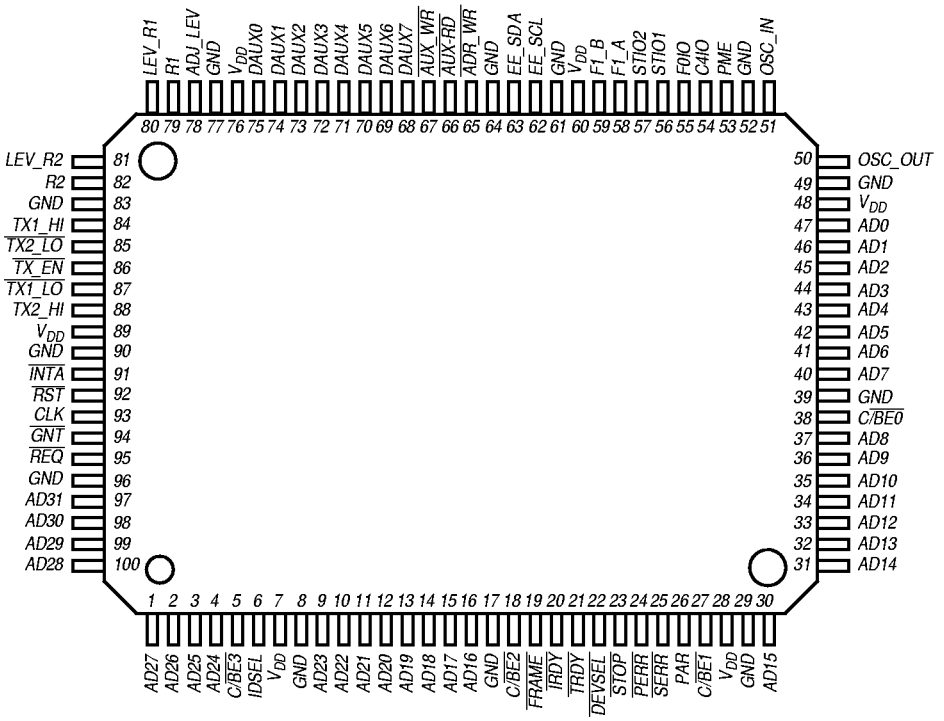


Figure 2–1. Pin Connection

2.1 PCI BUS INTERFACE

For further information, refer to the PCI Local Bus Specification.

PCI ADDRESS BUS

Pin No.	Pin Name	Input/ Output	Function
47	AD0	I/O	Address bit 0
46	AD1	I/O	Address bit 1
45	AD2	I/O	Address bit 2
44	AD3	I/O	Address bit 3
43	AD4	I/O	Address bit 4
42	AD5	I/O	Address bit 5
41	AD6	I/O	Address bit 6
40	AD7	I/O	Address bit 7
37	AD8	I/O	Address bit 8
36	AD9	I/O	Address bit 9
35	AD10	I/O	Address bit 10
34	AD11	I/O	Address bit 11
33	AD12	I/O	Address bit 12
32	AD13	I/O	Address bit 13
31	AD14	I/O	Address bit 14
30	AD15	I/O	Address bit 15
16	AD16	I/O	Address bit 16
15	AD17	I/O	Address bit 17
14	AD18	I/O	Address bit 18

PCI ADDRESS BUS (CONTINUED)

Pin No.	Pin Name	Input/ Output	Function
13	AD19	I/O	Address bit 19
12	AD20	I/O	Address bit 20
11	AD21	I/O	Address bit 21
10	AD22	I/O	Address bit 22
9	AD23	I/O	Address bit 23
4	AD24	I/O	Address bit 24
3	AD25	I/O	Address bit 25
2	AD26	I/O	Address bit 26
1	AD27	I/O	Address bit 27
100	AD28	I/O	Address bit 28
99	AD29	I/O	Address bit 29
98	AD30	I/O	Address bit 30
97	AD31	I/O	Address bit 31
26	PAR	I/O	Parity bit
38	C/BE0	I/O	Bus command and byte enable 0
27	C/BE1	I/O	Bus command and byte enable 1
18	C/BE2	I/O	Bus command and byte enable 2
5	C/BE3	I/O	Bus command and byte enable 3
93	CLK	I	PCI clock
92	$\overline{RST}$	I	Reset
19	$\overline{FRAME}$	I/O	Cycle frame
20	$\overline{IRDY}$	I/O	Initiator ready
21	$\overline{TRDY}$	I/O	Target ready
23	$\overline{STOP}$	I/O	Stop
6	IDSEL	I	Initialization device select
22	$\overline{DEVSEL}$	I/O	Device select
95	$\overline{REQ}$	O	Request
94	$\overline{GNT}$	I	Grant
24	$\overline{PERR}$	I/O	Parity error
25	$\overline{SERR}$	O	System error
53	PME	O	Power management event (high active) (See Figure 7–5)
91	$\overline{INTA}$	O	Interrupt A

2.2 AUXILIARY PORT

Pin No.	Pin Name	Input/ Output	Function
75	DAUX0	I/O	AUX data bit 0
74	DAUX1	I/O	AUX data bit 1
73	DAUX2	I/O	AUX data bit 2
72	DAUX3	I/O	AUX data bit 3
71	DAUX4	I/O	AUX data bit 4
70	DAUX5	I/O	AUX data bit 5
69	DAUX6	I/O	AUX data bit 6
68	DAUX7	I/O	AUX data bit 7
67	$\overline{AUX\_WR}$	O	AUX write
66	$\overline{AUX\_RD}$	O	AUX read
65	$\overline{ADR\_WR}$	I/O*	AUX address write

*I/O with internal pull down.

2.3 S/T INTERFACE TRANSMIT SIGNALS

Pin No.	Pin Name	Input/ Output	Function
88	TX2_HI	O	Transmit output 2
87	$\overline{TX1\_LO}$	O	GND driver for transmitter 1
86	$\overline{TX\_EN}$	O	Transmit enable
85	$\overline{TX2\_LO}$	O	GND driver for transmitter 2
84	TX1_HI	O	Transmit output 1

See also Section 7.2; External Transmitter Circuitry.

2.4 S/T INTERFACE RECEIVE SIGNALS

Pin No.	Pin Name	Input/ Output	Function
82	R2	I	Receive data 2
81	LEV_R2	I	Level detect for R2
80	LEV_R1	I	Level detect for R1
79	R1	I	Receive data 1
78	ADJ_LEV	O	Level generator

See also Section 7.1; External Receiver Circuitry.

2.5 OSCILLATOR

Pin No.	Pin Name	Input/ Output	Function
51	OSC_IN	I	Oscillator input or quartz connection 12.288 MHz
50	OSC_OUT	O	Oscillator output or quartz connection

2.6 GCI/IOM2 BUS INTERFACE

Pin No.	Pin Name	Input/ Output	Function
54	C4IO	I/O*	4.096 MHz clock GCI/IOM2 bus clock master: output GCI/IOM2 bus clock slave: input (reset default)
55	F0IO	I/O*	Frame synchronization, 8 kHz pulse for GCI/IOM2 bus frame synchronization GCI/IOM2 bus master: output GCI/IOM2 bus slave: input (reset default)
56	STIO1	I/O*	GCI/IOM2 bus data bus I Slotwise programmable as input or output
57	STIO2	I/O*	GCI/IOM2 bus data bus II Slotwise programmable as input or output

*I/O with internal pullup.

2.7 GCI/IOM2 TIMESLOT ENABLE SIGNALS

As an example, for PCM codecs.

Pin No.	Pin Name	Input/ Output	Function
58	*F1_A*	*O*	*Enable signal for external Codec A* *Programmable as positive (reset default) or negative pulse*
59	*F1_B*	*O*	*Enable signal for external Codec B* *Programmable as positive (reset default) or negative pulse*

2.8 EEPROM INTERFACE

The external EEPROM is optional. EE_SCL/EN and EE_SDA must be connected to GND if no external EEPROM is available.

Pin No.	Pin Name	Input/ Output	Function
63	*EE_SDA*	*I/O**	*Serial data of external EEPROM*
62	*EE_SCL/EN*	*I/O**	*Clock of external EEPROM/EEPROM enable*

**I/O with internal pullup.*

NOTE

EE_SCL/EN and EE_SDA must be connected to GND if no external EEPROM is available.

2.9 POWER SUPPLY

Pin No.	Pin Name	Function
7, 28, 48, 60, 76, 89	*V_{DD}*	*V_{DD} (+ 3.3 or 5 V)*
8, 17, 29, 39, 49, 52, 61, 64, 77, 83, 90, 96	*GND*	*GND*

NOTE

All power supply pins V_{DD} must be directly connected to each other. Also, all pins GND must be directly connected to each other.

To keep V_{DD} and GND bounce to a minimum, a bypass capacitor (10 nF to 100 nF) should be placed between each pair of V_{DD}/GND pins.

2.10 RESET CHARACTERISTICS

The reset signal (hardware reset or software reset) must be active for at least four clock cycles.

The GCI/IOM2 bus lines, STIO1, STIO2, and the interrupt lines are in three-state mode after a reset.

The MC145575 is in slave mode after reset. C4IO and F0IO are inputs.

The S/T state machine is stuck to 0 after reset. This means the MC145575 does not react to any signal on the S/T interface before the S/T state machine is initialized.

The registers' initial values are described in Section 4; Register Bit Description.

During initialization phase, the MC145575 must not be accessed. Bit 1 of the STATUS register is cleared to 0 to indicate that the initialization phase has been finished.

SECTION 3
FUNCTIONAL DESCRIPTION

3.1 PCI INTERFACE

3.1.1 PCI Access Types Used by MC145575

Table 3–1. PCI Command Types

C/$\overline{BE3}$	C/$\overline{BE2}$	C/$\overline{BE1}$	C/$\overline{BE0}$	Command Type	MC145575 Mode
0	*0*	*1*	*0*	*I/O Read*	*Target Mode*
0	*0*	*1*	*1*	*I/O Write*	*Target Mode*
0	*1*	*1*	*0*	*Memory Read*	*Target Mode and Master Mode*
0	*1*	*1*	*1*	*Memory Write*	*Target Mode and Master Mode*
1	*0*	*1*	*0*	*Configuration Read*	*Target Mode*
1	*0*	*1*	*1*	*Configuration Write*	*Target Mode*

3.1.2 PCI Modes Supported

The MC145575 supports both target mode and master mode. Before the MC145575 can operate in master mode, the 32K Memory Window Base Address register (MWBA) must be configured.

Afterwards, all FIFO data accesses are done by the MC145575 automatically by PCI master accesses.

Only control and configuration register accesses must be done using PCI target accesses by the host CPU.

3.1.3 PCI Buffer Signaling Environment

The MC145575 supports 5 and 3.3 V PCI bus signaling environment. The environment mode is set during RESET ($\overline{RST}$ low) by the input value of $\overline{ADR\_WR}$.

PCI Bus Signaling Environment	$\overline{ADR\_WR}$
3.3 V	*High*
5 V	*Low*

3.1.4 PCI Configuration Registers

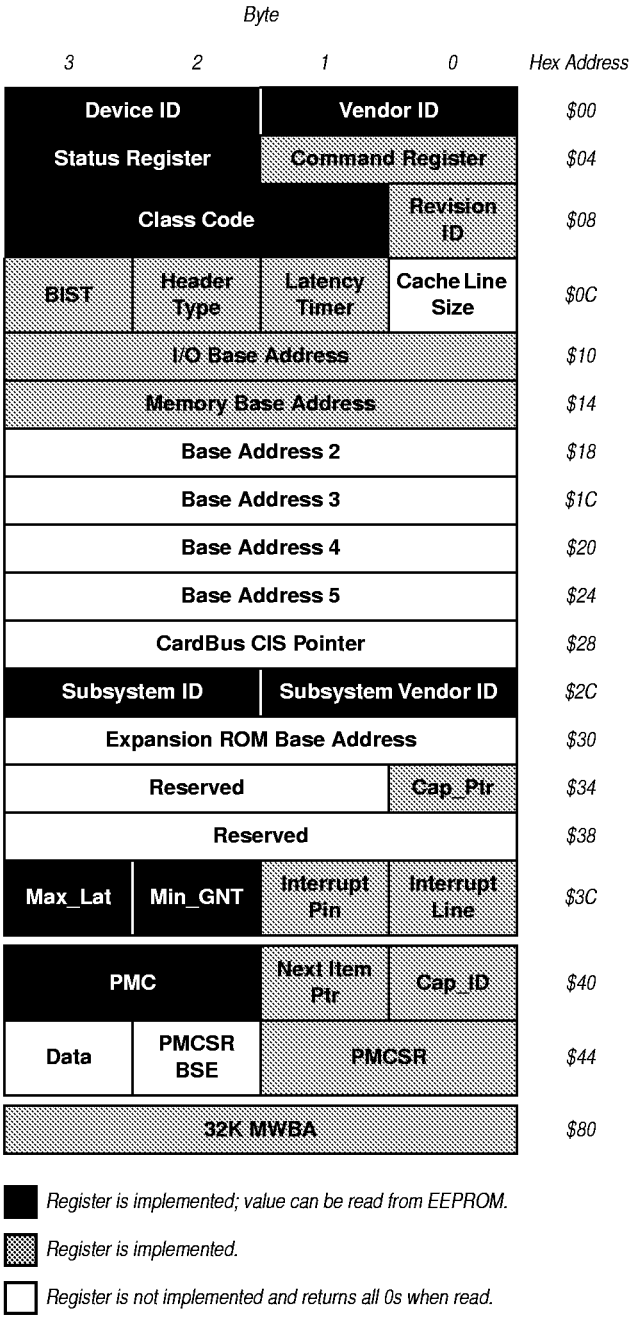


Figure 3–1. PCI Configuration Space

The external EEPROM is optional. If no EEPROM is available, EE_SCL/EN must be connected to GND. Without EEPROM, the PCI configuration registers will be loaded with the default values shown in Table 3–2.

All registers which can be read from EEPROM can also be written by configuration write accesses. The addresses for configuration write are shown in Table 3–2.

Table 3–2. PCI Configuration Registers' Initial Values

Register Name	Default Value	Remarks
Vendor ID	*$1057*	*Value can be read from EEPROM. Base address for configuration write is C0h.*
Device ID	*$0100*	*Value can be read from EEPROM. Base address for configuration write is C0h.*
Command Register		**Bits** **Function** *0* *Enables/disables I/O space accesses* *1* *Enables/disables memory space accesses* *2* *Enables/disables master accesses* *5..3* *Fixed to 0* *6* *$\overline{PERR}$ enable/disable* *7* *Fixed to 0* *8* *$\overline{SERR}$ enable/disable* *15..9* *Fixed to 0*
Status Register	*$0210*	*Bits[7:0] can be read from EEPROM. Base address for configuration write is C4h.* **Bits** **Function** *3..0* *Reserved* *4* *Fixed to 1* *5* *66 MHz capable* *6* *User-definable features supported* *7* *Fast back-to-back capable* *8* *Data parity error detected* *10..9* *Fixed to 01: timing of $\overline{DEVSEL}$ is medium* *11* *Signaled target abort (fixed to 0)* *12* *Received target abort* *13* *Received master abort* *14* *Signaled system error (address parity error)* *15* *Detected parity error*
Revision ID	*$01*	
Class Code	*$02 80 00*	*Value can be read from EEPROM. Base address for configuration write is C8h.*
Latency Timer	*$10*	*Set to 16 clocks; value is fixed*
Header Type	*$00*	*Header type 0*
BIST	*$00*	*No built-in self-test supported*
I/O Base Address		*Bits[31:3] are R/W by configuration accesses*
Memory Base Address		*Bits[31:8] are R/W by configuration accesses*
Subsystem Vendor ID	*$1057*	*Value can be read from EEPROM. Base address for configuration write is ECh.*
Subsystem ID	*$0100*	*Value can be read from EEPROM. Base address for configuration write is ECh.*
Cap_Ptr	*$40*	*Offset to power management register block*
Interrupt Line	*$FF*	*This register must be configured by configuration write*
Interrupt Pin	*$01*	*INTA supported*
Min_Gnt	*$00*	*Value can be read from EEPROM. Base address for configuration write is FCh.*
Max_Lat	*$10*	*Value can be read from EEPROM. Base address for configuration write is FCh.*
Cap_ID	*$01*	*Capability ID: $01 identifies the linked list item as PCI power management registers*
Next Ptr	*$00*	*There are no next items in the linked list*
PMC	*$7E21*	*Power management capabilities (see also PCI Bus Power Management Interface Specification); this register's value can be read from EEPROM. Base address for configuration write is E0h.* *$\overline{PME}$ can be asserted from D0, D1, D2, and $D3_{hot}$* *Device specific initialization is required* *The MC145575 does not require PCI clock to generate $\overline{PME}$ (if S/T change state is selected)* *This function complies with the PCI Power Management Specification Version 1.0*

Table 3–2. PCI Configuration Registers' Initial Values (Continued)

Register Name	Default Value	Remarks
PMCSR	*$0000*	*Power Management Control/Status* **Bits** **Function** *15* *PME_Status — This bit is set when the function would normally assert the $\overline{PME}$ signal independent of the state of the PME_En bit* *Writing a 1 to this bit will clear it and cause the function to stop asserting a $\overline{PME}$ (if enabled)* *Writing a 0 has no effect* *14..9* *Fixed to 0* *8* *PME_En — A 1 enables the function to assert $\overline{PME}$* *when 0, $\overline{PME}$ assertion is disabled* *7..2* *Fixed to 0* *1..0* *PowerState — This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state* *00b – D0* *01b – D1* *10b – D2* *11b – $D3_{hot}$* *All states except D0 disable MC145575 master accesses*
32K MWBA	*$0000*	*Bits[31:15] are R/W by configuration accesses* *The 32K Memory Window is for MC145575 internal use and for the B- and D-channel FIFOs; this register must be written to enable the MC145575 to operate in master mode*

Unimplemented registers return all 0s when read.

3.2 INTERNAL MC145575 REGISTER DESCRIPTION

If the MC145575 is used in memory-mapped mode, all registers can be directly accessed by adding their CIP address to the configured Memory Base Address.

In I/O address-mapped mode, the MC145575 occupies eight bytes in the I/O address space. Byte 0 is for data read/write, byte 4 for register selection. The AUX-port address is selected by byte 3, AUX-port data is read/written by byte 1.

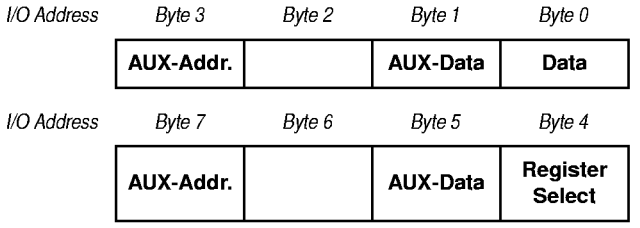


Figure 3–2. MC145575 in I/O Address-Mapped Mode

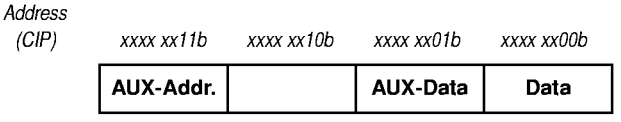


Figure 3–3. MC145575 in Memory Address-Mapped Mode

3.2.1 Registers of the S/T Section

CIP / I/O-Address		Name	R/W	Function
Binary	Hex			
1100 0000b	$C0	STATES	R/W	State of the TE/NT state machine
1100 0100b	$C4	SCTRL	W	S/T control register
1100 1000b	$C8	SCTRL_E	W	S/T control register (extended)
1100 1100b	$CC	SCTRL_R	W	Receive enable for B-channels
1101 0000b	$D0	SQ_REC	R	Receive register for S/Q bits
		SQ_SEND	W	Send register for S/Q bits
1101 1100b	$DC	CLKDEL	W	Setup of the delay time between receive and send direction (TE) receive data sample time (NT)
1111 0000b	$F0	B1_REC*	R	B1-channel receive register
		B1_SEND*	W	B1-channel transmit register
1111 0100b	$F4	B2_REC*	R	B2-channel receive register
		B2_SEND*	W	B2-channel transmit register
1111 1000b	$F8	D_REC*	R	D-channel receive register
		D_SEND*	W	D-channel transmit register
1111 1100b	$FC	E_REC*	R	E-channel receive register

*These registers are read/written automatically by the HDLC FIFO controller (HFC) or GCI/IOM2 bus controller and need not be accessed by the user. To read/write data, the FIFOs in the Memory Window should be used.

3.2.2 Registers of the GCI/IOM2 Bus Section

GCI/IOM2 MONITOR AND C/I REGISTERS

CIP / I/O-Address		Name	R/W	Function
Binary	Hex			
0000 1000b	$08	C/I	R/W	C/I command/indication register
0000 1100b	$0C	TRxR	R	Monitor Tx ready handshake
0010 1000b	$28	MON1_D	R/W	First monitor byte
0010 1100b	$2C	MON2_D	R/W	Second monitor byte

GCI/IOM2 BUS TIMESLOT SELECTION REGISTERS

CIP / I/O-Address		Name	R/W	Function
Binary	Hex			
1000 0000b	$80	B1_SSL	W	B1-channel transmit slot (0..31)
1000 0100b	$84	B2_SSL	W	B2-channel transmit slot (0..31)
1000 1000b	$88	AUX1_SSL	W	AUX1-channel transmit slot (0..31)
1000 1100b	$8C	AUX2_SSL	W	AUX2-channel transmit slot (0..31)
1001 0000b	$90	B1_RSL	W	B1-channel receive slot (0..31)
1001 0100b	$94	B2_RSL	W	B2-channel receive slot (0..31)
1001 1000b	$98	AUX1_RSL	W	AUX1-channel receive slot (0..31)
1001 1100b	$9C	AUX2_RSL	W	AUX2-channel receive slot (0..31)

GCI/IOM2 BUS DATA REGISTERS

CIP / I/O-Address		Name	R/W	Function
Binary	Hex			
1010 0000b	$A0	B1_D*	R/W	GCI/IOM2 bus B1-channel data register
1010 0100b	$A4	B2_D*	R/W	GCI/IOM2 bus B2-channel data register
1010 1000b	$A8	AUX1_D	R/W	AUX1-channel data register
1010 1100b	$AC	AUX2_D	R/W	AUX2-channel data register

*These registers are read/written automatically by the HDLC FIFO controller (HFC), or by the S/T controller, and need not be accessed by the user.

GCI/IOM2 BUS CONFIGURATION REGISTERS

CIP / I/O-Address		Name	R/W	Function
Binary	Hex			
1011 0100b	*$B4*	*MST_EMOD*	*W*	*Extended mode register for GCI/IOM2 bus*
1011 1000b	*$B8*	*MST_MODE*	*W*	*Mode register for GCI/IOM2 bus*
1011 1100b	*$BC*	*CONNECT*	*W*	*Connect functions for S/T, HFC, GCI/IOM2*

3.2.3 Interrupt and Status Registers

CIP / I/O-Address		Name	R/W	Function
Binary	Hex			
0100 0100b	*$44*	*FIFO_EN*	*W*	*FIFO enable/disable*
0100 1000b	*$48*	*TRM*	*W*	*Transparent mode interrupt mode register*
0100 1100b	*$4C*	*B_MODE*	*W*	*Mode of B-channels*
0101 1000b	*$58*	*CHIP_ID*	*R*	*Register for chip identification*
0110 0000b	*$60*	*CIRM*	*W*	*Interrupt selection and soft reset register*
0110 0100b	*$64*	*CTMT*	*W*	*Transparent mode and time control register*
0110 1000b	*$68*	*INT_M1*	*W*	*Interrupt mask register 1*
0110 1100b	*$6C*	*INT_M2*	*W*	*Interrupt mask register 2*
0111 1000b	*$78*	*INT_S1*	*R*	*Interrupt status register 1*
0111 1100b	*$7C*	*INT_S2*	*R*	*Interrupt status register 2*
0111 0000b	*$70*	*STATUS*	*R*	*Common status register*

3.3 TIMER

The MC145575 includes a timer with interrupt capability. The timer counts F0IO pulses. So, the timer counter is incremented every 125 µs. It can be reset by bit 7 of the CTMT register. Furthermore, the timer is reset at every MC145575 access when bit 5 of the CTMT register is set. Seven different timer values can be selected.

3.4 FIFOS

All FIFOs are located in the 32K Memory Window (MW) in the host PC's memory.

There are six FIFOs with six HDLC-Controllers handled by the MC145575. The HDLC circuits are located on the S/T device side of the MC145575. So always plain data is stored in the FIFO. Zero insertion and deletion is done in HDLC mode:

- *If the data goes to the S/T or GCI/IOM device in send FIFOs, and*
- *When the HDLC data comes from the S/T device or GCI/IOM2 bus in receive operation*

There is a send and a receive FIFO for each of the two B-channels and for the D-channel.

The FIFOs are realized as ring buffers in the 32K MW in the host PC's memory. To control them, there are counters.

	B-Channel	D-Channel
Z1: FIFO Input Counter	*13 Bit*	*9 Bit*
Z2: FIFO Output Counter	*13 Bit*	*9 Bit*

Each counter points to a byte position in the MW. This is an offset to the 32K MWBA in the configuration space. On a FIFO input operation, Z1 is incremented. On an output operation, Z2 is incremented.

After every pulse on the F0IO signal two HDLC-bytes are written into the S/T interface (FIFOs No. 0 and 2) and two HDLC-bytes are read from the S/T interface (FIFOs No. 1 and 3).

D-channel data is handled in a similar way, but only two bits are processed.

NOTE

Instead of the S/T interface also GCI/IOM2 bus is selectable for each B-channel (see CONNECT register).

If Z1 = Z2, the FIFO is empty.

Additionally, there are two counters F1 and F2 for every FIFO channel (5-bit for B-channel, 4-bit for D-channel). They count the HDLC-frames in the FIFOs and form a ring buffer as Z1 and Z2 do, too.

F1 is incremented when a complete frame has been received and stored in the FIFO. F2 is incremented when a complete frame has been read from the FIFO.

If F1 = F2, there is no complete frame in the FIFO.

When the RESET line is active or software reset is active, Z1, Z2, F1, and F2 are all initialized to all 1s.

All Zx and Fx counters are also stored in the MW, so it is easy to read and write the counters by simple host memory accesses.

Because the MC145575 is limited to the 32K MW, data in different regions of the host PC can not be overwritten even if counter and pointer values are handled in a wrong way.

NOTE

The counter state $0200 of the Z-counters follows counter state $1FFF in the B-channel FIFOs.

The counter state $000 of the Z-counters follows counter state $1FF in the D-channel FIFOs.

The counter state $00 of the F-counters follows counter state $1F in the B-channel FIFOs.

The counter state $10 of the F-counters follows counter state $1F in the D-channel FIFOs.

3.4.1 FIFO Counters Location in Memory Window

For each FIFO one F1 and one F2 counter is available. The counters are located at the following offsets to the MWBA in the MW.

Table 3–3. F1 and F2 Counter Locations

FIFO	Counter	Offset to MW Base Address	Counter Size in Bytes
B1-Transmit	*F1*	*$2080*	*1*
	*F2**	*$2081*	*1*
B1-Receive	*F1**	*$6080*	*1*
	F2	*$6081*	*1*
B2-Transmit	*F1*	*$2180*	*1*
	*F2**	*$2181*	*1*
B2-Receive	*F1**	*$6180*	*1*
	F2	*$6181*	*1*
D-Transmit	*F1*	*$20A0*	*1*
	*F2**	*$20A1*	*1*
D-Receive	*F1**	*$60A0*	*1*
	F2	*$60A1*	*1*

**These counters are handled by the MC145575 automatically and must not be written by software.*

For each FIFO, an array of Z1 and Z2 counters is available. The offset of the counters to the MWBA can be calculated as shown in the following table.

Table 3–4. Z1 and Z2 Counter Locations

FIFO	Counter	Offset to MW Base Address	Counter Size in Bytes
B1-Transmit	*Z1*	*$2000 + (Fx * 4)*	*2*
	*Z2**	*$2000 + (Fx * 4) + 2*	*2*
B1-Receive	*Z1**	*$6000 + (Fx * 4)*	*2*
	Z2	*$6000 + (Fx * 4) + 2*	*2*
B2-Transmit	*Z1*	*$2100 + (Fx * 4)*	*2*
	*Z2**	*$2100 + (Fx * 4) + 2*	*2*
B2-Receive	*Z1**	*$6100 + (Fx * 4)*	*2*
	Z2	*$6100 + (Fx * 4) + 2*	*2*
D-Transmit	*Z1*	*$2080 + (Fx * 4)*	*2*
	*Z2**	*$2080 + (Fx * 4) + 2*	*2*
D-Receive	*Z1**	*$6080 + (Fx * 4)*	*2*
	Z2	*$6080 + (Fx * 4) + 2*	*2*

**These counters are handled by the MC145575 automatically and must not be written by software.*

Fx is either F1 or F2. F1 is used for input data in transmit FIFOs, F2 is used for output data in receive FIFOs.

3.4.2 FIFO Data Location in Memory Window

Table 3–5. Data Location in MW

FIFO	Starting at Offset	Ending at Offset	Offset to Add to Z-Counters Value
B1-transmit	*$0200*	*$1FFF*	*$0000*
B1-receive	*$4200*	*$5FFF*	*$4000*
B2-transmit	*$2200*	*$3FFF*	*$2000*
B2-receive	*$6200*	*$7FFF*	*$6000*
D-transmit	*$0000*	*$01FF*	*$0000*
D-receive	*$4000*	*$41FF*	*$4000*

3.4.3 FIFO Channel Operation

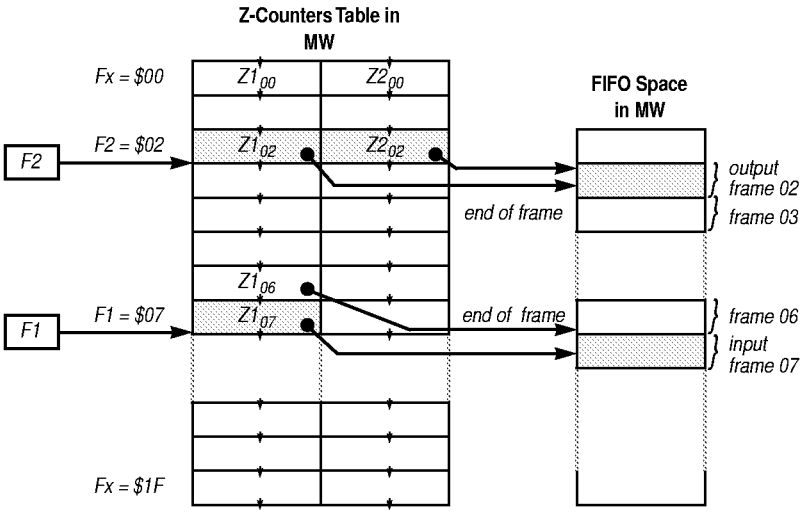


Figure 3–4. FIFO Organization (Shown for B-Channel, Similar for D-Channel)

3.4.3.1 SEND CHANNELS (B1, B2, AND D TRANSMIT). *The send channels send data from the host bus interface to the FIFO and the MC145575 converts the data into HDLC code and transfers it from the FIFO into the S/T or/and the GCI/IOM2 bus interface write registers.*

The MC145575 checks Z1 and Z2. If Z1 = Z2 (FIFO empty), the MC145575 generates an HDLC-Flag (01111110) and sends it to the S/T device. In this case, Z2 is not incremented. Also, if F1 = F2, only HDLC flags are sent to the S/T interface and all counters remain unchanged. If the frame counters are unequal, F2 is incremented and the MC145575 tries to send the next frame to the output device. After the end of a frame (Z2 reaches Z1), it automatically generates the 16-bit CRC checksum and adds the ending flag. If there is another frame in the FIFO (F1 ≠ F2), the F2 counter is incremented.

With every byte being sent from the host bus side to the FIFO, Z1 is incremented automatically. If a complete frame has been sent, F1 must be incremented to send the next frame. If the frame counter F1 is incremented also, the Z-counters may change because Z1 and Z2 are functions of F1 and F2. So there are Z1(F1), Z2(F1), Z1(F2), and Z2(F2) (see Figure 3–4).

Z1(F1) is used for the frame that is just written from the PC-bus side. Z2(F2) is used for the frame that is just being transmitted to the S/T device side of the MC145575. Z1(F2) is the end of frame pointer of the current output frame.

In the send channels, F1 is only changed from the PC interface side if the software driver wants to say, "end of send frame." Then, the current value of Z1 is stored, F1 is incremented, and Z1 is used as start address of the next frame. Z1(F2) and Z2(F2) can not be accessed.

3.4.3.2 AUTOMATICALLY D-CHANNEL FRAME REPETITION. *The D-channel send FIFO has a special feature. If the S/T interface signals a D-channel contention before the CRC is sent, the Z2 counter is set to the starting address of the current frame and the MC145575 tries to repeat the frame automatically.*

NOTE

The MC145575 begins to transmit bytes from a FIFO at the moment Z1 ≠ Z2. So, if the Z1 pointer is updated by software after writing the transmit data into the FIFO space of the MW, the transmission starts.

3.4.3.3 FIFO FULL CONDITION IN SEND CHANNELS. *FIFO full condition can easily be calculated from the Z1/Z2 table in the MW.*

Remember that an increment of Z-value $1FFF is $0200 in the B-channels.

There are two different FIFO full conditions. The first one is met when the FIFO content comes up to 31 frames (B-channel) or 15 frames (D-channel). The MC145575 can not manage more frames, even if the frames are very small.

The second limitation is the size of the FIFO, which is 512 bytes for the D-channel and 7.5 kbytes for the B-channels.

3.4.3.4 RECEIVE CHANNELS (B1, B2, AND D RECEIVE). *The receive channels receive data from the S/T or GCI/IOM2 bus interface read registers. The data is converted from HDLC into plain data and is sent to the FIFO. The data can then be read via the host bus interface.*

The MC145575 checks the HDLC incoming data. If it finds a flag or more than five consecutive 1s, it does not generate any output data. In this case, Z1 is not incremented. Valid HDLC data received is converted by the MC145575 into plain data. After the ending flag of a frame, the MC145575 checks the HDLC CRC checksum. If it is correct, one byte with all 0s is inserted behind the CRC data in the FIFO named STAT. This last byte of a frame in the FIFO is different from all 0s if there is no correct CRC field at the end of the frame.

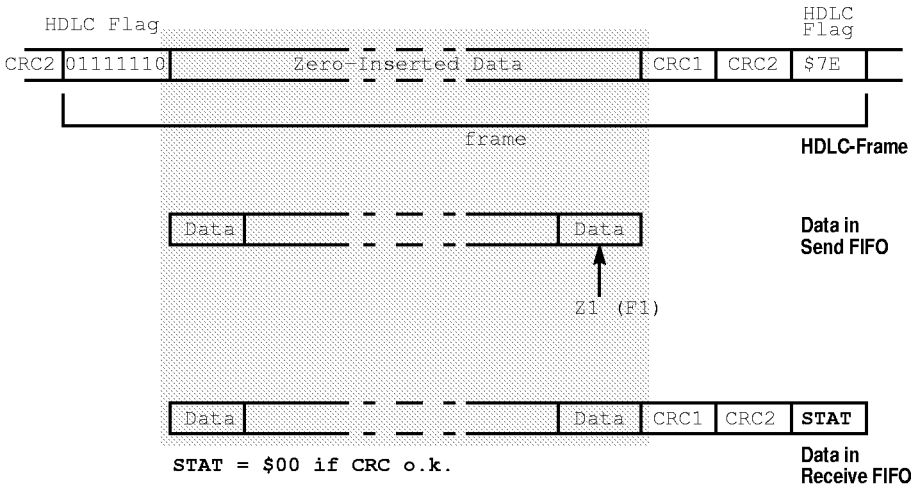


Figure 3–5. FIFO Data Organization

The ending flag of an HDLC-frame can also be the starting flag of the next frame.

After a frame is received completely, F1 is incremented by the MC145575 automatically and the next frame can be received.

After reading a frame via the host bus interface, F2 must be incremented. If the frame counter F2 is incremented also, the Z-counters may change because Z1 and Z2 are functions of F1 and F2. So there are Z1(F1), Z2(F1), Z1(F2), and Z2(F2) (see Figure 3–4).

Z1(F1) is used for the frame that is just received from the S/T device side of the HFC. Z2(F2) is used for the frame that is just being transmitted to the host bus interface. Z1(F2) is the end-of-frame pointer of the current output frame.

To calculate the length of the current receive frame, the software has to evaluate Z1 – Z2 + 1.

In the receive channels, F2 must be incremented to point to the next Z1/Z2 pair. If Z1 = Z2 and F1 = F2, the FIFO is totally empty.

3.4.3.5 FIFO FULL CONDITION IN RECEIVE CHANNELS. *Because the ISDN B- and D-channels have no hardware-based flow control, there is no opportunity to stop input data if a receive FIFO is full. Therefore, there is no FIFO full condition implemented in the MC145575. The MC145575 assumes that the FIFOs are so deep that the host processor hardware and software is able to avoid any overflow of the receive FIFOs. Overflow conditions are again more than 31 input frames (15 frames for D-channel), or a real overflow of the FIFO because of excessive data.*

Because HDLC procedures only know a window size of seven frames, no more than seven frames are sent without software intervention. Due to the great size of the FIFOs of the MC145575, it is easy to poll counters in the MW even in large time intervals without having to fear a FIFO overflow condition.

To avoid undetected FIFO overflows, the software driver should check the number of frames in the FIFO, which is F1 – F2. An overflow exists if the number (F1 – F2) is less than the number in the last reading, even if there was no reading of a frame in between.

After a detected FIFO overflow condition, this FIFO must be reset.

3.4.3.6 FIFO INITIALIZATION. *All counters Z1, Z2, F1, and F2 of all FIFOs are initialized to all 1s after a RESET.*

The result is Z1 = Z2 = $1FFF and F1 = F2 = $1F for the B-channels and Z1 = Z2 = $1FF and F1 = F2 = $1F for the D-channel. This information is written in the MW for initialization.

Please mask bit 4 of D-channel from counter F1, F2.

The same initialization is done if the bit 3 in the CIRM register is set (soft reset).

During the initialization phase, the MC145575 must not be accessed. Bit 1 of the STATUS register is cleared to 0 to indicate that the initialization phase has been finished.

3.4.4 Transparent Mode of MC145575

You can switch off HDLC operation for each B-channel independently. There is one bit for each B-channel in the CTMT control register. If this bit is set, data in the FIFO is sent directly to the S/T or GCI/IOM2 bus interface and data from the S/T or GCI/IOM2 bus interface is sent directly to the FIFO.

Be sure to switch into transparent mode only if F1 = F2. Being in transparent mode, the Fx counters remain unchanged. Z1 and Z2 are the input and output pointers, respectively. Because F1 = F2, both Z-counters are always accessible and have valid data.

If a send FIFO channel changes to FIFO empty condition, no CRC is generated and the last data byte written into the FIFO is repeated until there is new data.

In receive channels, there is no check on flags or correct CRCs and no status byte is added.

The byte boundaries are not arbitrary like in HDLC mode where byte synchronization is achieved with HDLC-flags. The data is just the same as it comes from the S/T or GCI/IOM2 bus interface, or is sent to this.

Send and receive transparent data can be handled in two ways. The usual way is transmitting B-channel data with the LSB first, as is usual in HDLC mode. The second way is sending the bytes in reverse bit order as it is usual for PWM data; so the first bit is the MSB. The bit order can be reversed by setting the corresponding bits in the CIRM register.

SECTION 4
REGISTER BIT DESCRIPTION

4.1 REGISTER BIT DESCRIPTION OF S/T SECTION

Name	Addr.	Bits	R/W	Function
STATES	*$C0*	*3..0*	*R* *W*	*Binary value of actual state (NT: Gx, TE: Fx)* *Prepare for new state xxxx*
		4	*W*	*1— loads the prepared state (bit 3..0) and stops the state machine; this bit needs to be set for a minimum period of 5.21 µs and must be cleared by software* *(reset default)* *0 — enables the state machine* *After writing an invalid state, the state machine goes to deactivated state (G1, F2)*
		5	*W*	*0 — prepare deactivation* *1 — prepare activation*
		6	*W*	*1 — start activation/deactivation as selected by bit 5* *This bit is automatically cleared after activation/deactivation*
		7	*W*	*0 — no operation* *1 — in NT mode allows transition from G2 to G3* *This bit is automatically cleared after the transition*

NOTE

The state machine is stuck to 0 after a reset. Writing a 0 to bit 4 of the STATES register restarts the state machine.

In this state, the MC145575 sends no signal on the S/T-line and it is not possible to activate it by incoming INFOx.

NT mode: *The NT state machine does not change automatically from G2 to G3 if the TE side sends INFO3 frames. This transition must be activated each time by bit 7 of the STATES register.*

Name	Addr.	Bits	R/W	Function
SCTRL	*$C4*			*B-channel enable*
		0	*W*	*0 — B1 send data disabled (permanent 1 sent in activated states, reset default)* *1 — B1 data enabled*
		1	*W*	*0 — B2 send data disabled (permanent 1 sent in activated states, reset default)* *1 — B2 data enabled*
		2	*W*	*S/T interface mode* *0 — TE mode (reset default)* *1 — NT mode*
		3	*W*	*D-channel priority* *0 — high priority 8/9 (reset default)* *1 — low priority 10/11*
		4	*W*	*S/Q bit transmission* *0 — S/Q bit disable (reset default)* *1 — S/Q bit and multiframe enable*
		5	*W*	*0 — normal operation (reset default)* *1 — send 96 kHz transmit test signal (alternating 0s)*
		6	*W*	*TX_LO line setup* *This bit must be configured depending on the used S/T module and circuitry to match to 400 Ω pulse mask test.* *0 — capacitive line mode (reset default)* *1 — non-capacitive line mode*
		7	*W*	*Power down* *0 — power up, oscillator active (reset default)* *1 — power down, oscillator stopped*
SCTRL_E	*$C8*	*0*	*W*	*Power down mode bit* *0 — S/T awake disable (reset default)* *Power up can only be programmed by register access (SCTRL bit 7)* *1 — S/T awake enable; oscillator starts on every non-INFO0 S/T signal*
		1	*W*	*Must be 0*
		2	*W*	*D reset* *0 — normal operation (reset default)* *1 — D bits are forced to 1*
		3	*W*	*D_U enable* *0 — normal operation (reset default)* *1 — D channel is always send enabled regardless of E receive bit*
		6..4	*W*	*must be 0*
		7	*W*	*0 — normal operation (reset default)* *1 — B1/B2 are exchanged in the S/T interface*

Name	Addr.	Bits	R/W	Function
SCTRL_R	*$CC*	*0* *1*	*W* *W*	*B1-channel receive enable* *B2-channel receive enable* *0 — B-receive bits are forced to 1* *1 — normal operation*
		7..2	*W*	*unused*
SQ_REC	*$D0*	*3..0*	*R*	*TE mode: S bits (bit 3 = S1, bit 2 = S2, bit 1 = S3, bit 0 = S4)* *NT mode: Q bits (bit 3 = Q1, bit 2 = Q2, bit 1 = Q3, bit 0 = Q4)*
		4	*R*	*1 — a complete S or Q dataword has been received* *Reading SQ_REC clears this bit*
		6..5	*R*	*Not defined*
		7	*R*	*1 — ready to send a new S or Q dataword* *Writing to SQ_SEND clears this bit*
SQ_SEND	*$D0*	*3..0*	*W*	*TE mode: Q bits (bit 3 = Q1, bit 2 = Q2, bit 1 = Q3, bit 0 = Q4)* *NT mode: S bits (bit 3 = S1, bit 2 = S2, bit 1 = S3, bit 0 = S4)*
		7..4	*W*	*Not defined*
CLKDEL	*$DC*	*3..0*	*W*	*TE: 4-bit delay value to configure the 2-bit delay time between receive and transmit direction; the delay of the external S/T-interface circuit can be compensated; the lower the value the smaller the delay between receive and transmit direction (see also Figure 9–1)* *NT: Data sample point; the lower the value the earlier the input data is sampled* *The steps are 163 ns at 12.288 MHz clock frequency*
		6..4	*W*	*NT mode only* *Early edge input data shaping* *Low pass characteristic of extended bus configurations can be compensated; the lower the value the earlier input data pulse is sampled; no compensation means a value of 6 (110b)* *Step size is the same as for bits 3 – 0*
		7	*W*	*Unused*

NOTE

The register is not initialized with a 0 after reset. The register should be initialized as follows before activating the TE/NT state machine in 12.288 MHz mode:

TE mode: $0D .. $0F *NT mode: $6C*

4.2 REGISTER BIT DESCRIPTION OF GCI/IOM2 BUS SECTION

TIMESLOTS FOR TRANSMIT DIRECTION

Name	Addr.	Bits	R/W	Function
B1_SSL	*$80*	*4..0*	*W*	*Select GCI/IOM2 bus transmission slot (0..31)*
B2_SSL	*$84*	*5*	*W*	*Unused*
AUX1_SSL *AUX2_SSL*	*$88* *$8C*	*6*	*W*	*Select GCI/IOM2 bus data lines* *0 — STIO1 output* *1 — STIO2 output*
		7	*W*	*Transmit channel enable for GCI/IOM2 bus* *0 — disable (reset default)* *1 — enable*

NOTE

Enabling more than one channel on the same slot causes undefined output data.

TIMESLOTS FOR RECEIVE DIRECTION

Name	Addr.	Bits	R/W	Function
B1_RSL	*$90*	*4..0*	*W*	*Select GCI/IOM2 bus receive slot (0..31)*
B2_RSL	*$94*	*5*	*W*	*Unused*
AUX1_RSL *AUX2_RSL*	*$98* *$9C*	*6*	*W*	*Select GCI/IOM2 bus data lines* *0 — STIO2 is input* *1 — STIO1 is input*
		7	*W*	*Receive channel enable for GCI/IOM2 bus* *0 — disable (reset default)* *1 — enable*

DATA REGISTERS

Name	Addr.	Bits	R/W	Function
B1_D *B2_D* *AUX1_D* *AUX2_D*	*$A0* *$A4* *$A8* *$AC*	*0..7*	*W*	*Read/write data registers for selected timeslot data*

NOTE

If the data registers AUX1_D and AUX2_D are not overwritten, the transmission slots AUX1_SSL and AUX2_SSL mirror the data received in AUX1_RSL and AUX2_RSL slots. This is useful for an internal connection between two codecs. This mirroring is disabled by setting bit 1 in the MST_EMOD register.

Name	Addr.	Bits	R/W	Function
MST_MODE	*$B8*	*0*	*W*	*GCI/IOM2 bus mode* *0 — slave (reset default) (C4IO and F0IO are inputs)* *1 — master (C4IO and F0IO are outputs)*
		1	*W*	*Polarity of C4- and C2O-clock* *0 — F0IO is sampled on negative clock transition* *1 — F0IO is sampled on positive clock transition*
		2	*W*	*Polarity of F0-signal* *0 — F0 positive pulse* *1 — F0 negative pulse*
		3	*W*	*Duration of F0-signal* *0 — F0 active for one C4-clock (244 ns) (reset default)* *1 — F0 active for two C4-clocks (488 ns)*
		5, 4	*W*	*Timeslot for codec-A signal F1_A* *00 — B1 receive slot* *01 — B2 receive slot* *10 — AUX1 receive slot* *11 — signal C2O (pin F1_A → C2O is 2048 kHz clock)*
		7, 6	*W*	*Timeslot for codec-B signal F1_B* *00 — B1 receive slot* *01 — B2 receive slot* *10 — AUX1 receive slot* *11 — AUX2 receive slot*

The pulse shape and polarity of the codec signals F1_A and F1_B is the same as the pulse shape of the F0IO signal. The polarity of C2O can be changed by bit 1.

RESET sets register MST_MODE to all 0s.

Name	Addr.	Bits	R/W	Function
MST_EMOD	*$B4*	*0*	*W*	*Slow down C4IO clock adjustment (see Figure 10–2)* *0 — C4IO clock is adjusted in timeslot 31 twice for one-half clock cycle (reset default)* *1 — C4IO clock is adjusted in timeslot 31 once for one-half clock cycle*
		1	*W*	*Enable/disable AUX channel mirroring* *0 — normal operation (reset default)* *1 — disable AUX channel data mirroring*
		2	*W*	*Unused*
		5..3	*W*	*Select D-channel data flow (see also: CONNECT register)* **Destination** ← **Source** *Bit 3 0 D-HFC ← D-S/T* *1 D-HFC ← D-GCI/IOM2* *Bit 4: 0 D-S/T ← D-HFC* *1 D-S/T ← D-GCI/IOM2* *Bit 5: 0 D-GCI/IOM2 ← D-HFC* *1 D-GCI/IOM2 ← D-S/T*
		6	*W*	*Unused*
		7	*W*	*Enable GCI/IOM2 write slots* *0 — disable GCI/IOM2 write slots; slot #2 and slot #3 may be used for normal data* *1 — enables slot #2 and slot #3 as master, D-, and C/I-channel*
C/I	*$08*	*3..0*	*R/W*	*On read: indication* *On write: command*
		7..4		*Unused*
TRxR	*$0C*	*0*	*R*	*1 — monitor receive ready (two bytes received)* *This bit is reset after read of second monitor byte (MON2_D)*
		1	*R*	*1 — Monitor transmitter ready* *Writing on MON2_D starts transmission and resets this bit*
		5..2	*R*	*Reserved*
		6	*R*	*STIO2 in*
		7	*R*	*STIO1 in*

RESET sets register MST_EMOD to all 0s.

4.3 REGISTER BIT DESCRIPTION OF CONNECT REGISTER

Name	Addr.	Bits	R/W	Function
CONNECT	*$BC*	*2..0*	*W*	*Select B1-channel data flow* **Destination** ← **Source** *Bit 0: 0 B1-HFC ← B1-S/T* *1 B1-HFC ← B1-GCI/IOM2* *Bit 1: 0 B1-S/T ← B1-HFC* *1 B1-S/T ← B1-GCI/IOM2* *Bit 2: 0 B1-GCI/IOM2 ← B1-HFC, D-HFC* *1 B1-GCI/IOM2 ← B1-S/T, D-S/T*
		5..3	*W*	*Select B2-channel data flow* **Destination** ← **Source** *Bit 3: 0 B2-HFC ← B2-S/T* *1 B2-HFC ← B2-GCI/IOM2* *Bit 4: 0 B2-S/T ← B2-HFC* *1 B2-S/T ← B2-GCI/IOM2* *Bit 5: 0 B2-GCI/IOM2 ← B2-HFC* *1 B2-GCI/IOM2 ← B2-S/T*
		7..6	*W*	*Unused*

RESET sets CONNECT register to all 0s.

Figure 4–1 shows the different options for switching the B-channels with the CONNECT register.

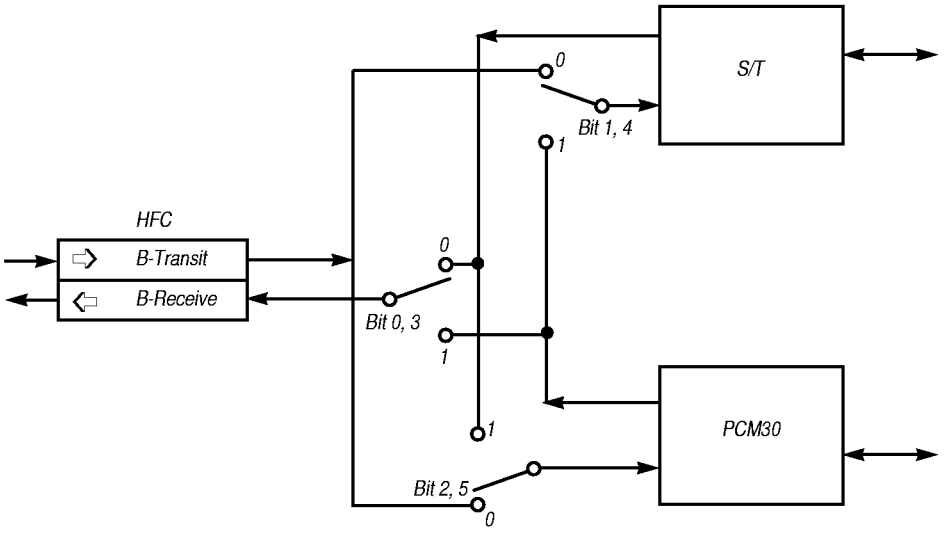


Figure 4–1. Function of the CONNECT Register Bits

4.4 REGISTER BIT DESCRIPTION OF AUXILIARY AND CROSS DATA REGISTERS

Name	Addr.	Bits	R/W	Function
CIRM	*$60*	*2..0*	*W*	*Defines the length of the auxiliary port access* **Value Cycle Time (AUX_WR or AUX_RD low)** *000b 1 PCI-Clock* *001b 3 PCI-Clocks* *010b 5 PCI-Clocks* *011b 7 PCI-Clocks* *100b 9 PCI-Clocks* *101b 11 PCI-Clocks* *110b 13 PCI-Clocks* *111b 15 PCI-Clocks*
		3	*W*	*Soft reset, similar as hardware reset; the registers CIP, CIRM, and CTMT are not changed, the PCI interface is not reset; the reset is active until the bit is cleared* *0 — deactivate reset (reset default)* *1 — activate reset*
		5..4	*W*	*Must be 0*
		6	*W*	*Select bit order for B1-channel* *0 — normal read/write data operation* *1 — reverse bit order read/write data operation*
		7	*W*	*Select bit order for B2-channel* *0 — normal read/write data operation* *1 — reverse bit order read/write data operation*
FIFO_EN	*$44*	*5..0*	*W*	*FIFO enable/disable (1 = enable (reset default))* **Bit FIFO** *0 B1-transit* *1 B1-receive* *2 B2-transmit* *3 B2-receive* *4 D-transmit* *5 D-receive* *The enable/disable change becomes valid between 0 and 250 µs after the bit has been written; all PCI bus accesses and FIFO activities are disabled for the selected FIFOs; to avoid unnecessary PCI transfers, all unused FIFOs should be disabled*
		7..6	*W*	*Unused; should be 0*

Name	Addr.	Bits	R/W	Function
CTMT	$64	0	W	HDLC/transparent mode for B1-channel 0 — HDLC mode (reset default) 1 — transparent mode
		1	W	HDLC/transparent mode for B2-channel 0 — HDLC mode (reset default) 1 — transparent mode
		4..2	W	select timer (bit 4 = MSB) **Timer** 000 off 001 3.125 ms 010 6.25 ms 011 12.5 ms 100 25 ms 101 50 ms 110 400 ms 111 800 ms
		5	W	Timer reset mode 0 — reset timer by CTMT bit 7 (reset default) 1 — automatically reset timer at each access to MC145575
		6	W	Ignored
		7	W	Reset timer 1 — reset timer This bit is automatically cleared
CHIP_ID	$58	0	R	Power supply 0 — 5 V power supply 1 — 3.3 V power supply
		3..1	R	Reserved
		7..4	R	Chip identification 0011b MC145575
B_MODE	$4C	1..0	W	Unused
		2	W	In 64 kbps mode: must be 0 In 56 kbps mode: value of the LSB in 7-bit mode
		3	W	Unused
		4	W	56 kbps mode selection bit for B1-channel 0 — 64 kbps mode (reset default) 1 — 56 kbps mode
		5	W	56 kbps mode selection bit for B2-channel 0 — 64 kbps mode (reset default) 1 — 56 kbps mode
		6	W	0 — data not inverted for B1-channel (reset default) 1 — data inverted for B1-channel
		7	W	0 — data not inverted for B2-channel (reset default) 1 — data inverted for B2-channel
INT_M1	$68	0	W	Interrupt mask for channel B1 in transmit direction
		1	W	Interrupt mask for channel B2 in transmit direction
		2	W	Interrupt mask for channel D in transmit direction
		3	W	Interrupt mask for channel B1 in receive direction
		4	W	Interrupt mask for channel B2 in receive direction
		5	W	Interrupt mask for channel D in receive direction
		6	W	Interrupt mask for state change of TE/NT state machine
		7	W	Interrupt mask for timer

For mask bits, a 1 enables and a 0 disables interrupt. RESET clears all bits to 0.

Name	Addr.	Bits	R/W	Function
INT_M2	*$6C*	*0*	*W*	*Interrupt mask for processing/non-processing phase transition*
		1	*W*	*Interrupt mask for GCI I-change*
		2	*W*	*Interrupt mask for GCI monitor receive*
		3	*W*	*Enable for interrupt output (1 = enable)*
		6..4	*W*	*Unused*
		7	*W*	*PMESEL* *0 — PME triggered on D-channel receive int* *1 — PME triggered on S/T interface state change*

For mask bits, a 1 enables and a 0 disables interrupt. RESET clears all bits to 0.

Name	Addr.	Bits	R/W	Function
TRM	*48*	*1..0*	*W*	*Interrupt in transparent mode is generated if Z1 in receive FIFOs or Z2 in transmit FIFOs change from:* *00: x xxxx x011 1111 → x xxxx x100 0000* *01: x xxxx 0111 1111 → x xxxx 1000 0000* *10: x xxx0 1111 1111 → x xxx1 0000 0000* *11: x 0111 1111 1111 → x 1000 0000 0000*
		4..2	*W*	*Must be 0*
		5	*W*	*E → B2 receive channel* *When set, the E receive channel of the S/T interface is connected to the B2 receive channel*
		6	*W*	*B1 + B2 mode* *0 — normal operation (reset default)* *1 — B1 + B2 are combined into one HDLC or transparent channel; all settings for data shape and connect are derived from B1*
		7	*W*	*IOM test loop* *When set, the MST output is looped to the MST input*

Name	Addr.	Bits	R/W	Function
INT_S1	*$78*	*0* *1*	*R* *R*	*B1-channel interrupt status in transmit direction* *B2-channel interrupt status in transmit direction* *In HDLC mode:* *1 — a complete frame has been transmitted, the frame counter F2 has been incremented* *In Transparent mode:* *1 — interrupt as selected in TRM register bits 1..0*
		2	*R*	*D-channel interrupt status in transmit direction* *1 — a complete frame was transmitted, the frame counter F2 was incremented*
		3 *4*	*R* *R*	*B1-channel interrupt status in receive direction* *B2-channel interrupt status in receive direction* *In HDLC mode:* *1 — a complete frame has been transmitted, the frame counter F1 has been incremented* *In transparent mode:* *1 — interrupt as selected in TRM register bits 1..0*
		5	*R*	*D-channel interrupt status in receive direction* *1 — a complete frame was received, the frame counter F1 was incremented*
		6	*R*	*TE/NT state machine interrupt status* *1 — state of state machine changed*
		7	*R*	*Timer interrupt status* *1 — timer is elapsed*
INT_S2	*$7C*	*0*	*R*	*Processing/non-processing transition interrupt status* *1 — the MC145575 has changed from processing to non-processing state*
		1	*R*	*GCI I-change interrupt* *1 — a different I-value on GCI was detected*
		2	*R*	*Receiver ready (RxR) of monitor channel* *1 — 2 monitor bytes have been received*
		6..3	*R*	*Unused, 0*
		7	*R*	*1 — fatal error: synchronization lost; PCI performance too low for MC145575; only soft reset recovers from this situation*

NOTE

Reading the INT_S1 or INT_S2 register resets all active read interrupts in the INT_S1 or INT_S2 register. New interrupts may occur during read. These interrupts are reported at the next read of INT_S1 or INT_S2.

All interrupt bits are reported regardless of the mask register settings (INT_M1 and INT_M2). The mask register settings only influence the interrupt output condition.

The interrupt output goes inactive during the read of INT_S1 or INT_S2. If interrupts occur during this read, the interrupt line goes active immediately after the read is finished. So, processors with level or transition triggered interrupt inputs can be connected.

Name	Addr.	Bits	R/W	Function
STATUS	*$70*	*0*	*R*	*Always 0*
		1	*R*	*Processing/non-processing status* *1 — the MC145575 is in processing phase (every 125 μs)* *0 — the MC145575 is not in processing phase*
		2	*R*	*Processing/non-processing transition interrupt status* *1 — the MC145575 has finished internal processing phase (every 125 μs)*
		3	*R*	*Always 0*
		4	*R*	*Timer status* *0 — timer not elapsed* *1 — timer elapsed*
		5	*R*	*TE/NT state machine interrupt state* *1 — state of state machine has changed*
		6	*R*	*FRAME interrupt has occurred (any data channel interrupt)* *All masked D-channel and B-channel interrupts are OR'd*
		7	*R*	*ANY interrupt* *All masked interrupts are OR'd*

Reading the STATUS register clears no bit.

SECTION 5
ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	*– 0.3 to + 7.0*	*V*
Input Voltage	V_I	*– 0.3 to V_{DD} + 0.3*	*V*
Output Voltage	V_O	*– 0.3 to V_{DD} + 0.3*	*V*
Storage Temperature Range	T_{stg}	*– 40 to + 125*	*°C*

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	*V_{DD} = 5 V* *V_{DD} = 3.3 V*	*4.75* *3.15*	*5.0* *3.3*	*5.25* *3.45*	*V*
Operating Temperature	T_A		*0*	—	*+ 70*	*°C*

ELECTRICAL CHARACTERISTICS FOR 5 V POWER SUPPLY

V_{DD} = 4.75 to 5.25 V, T_A = – 0 to + 70°C

Parameter	Symbol	Condition	TTL Level			CMOS Level			Unit
			Min	Typ	Max	Min	Typ	Max	
Input LOW Voltage	V_{IL}		—	—	*0.8*	—	—	*1.0*	*V*
Input HIGH Voltage	V_{IH}		*2.0*	—	—	*3.5*	—	—	*V*
Output LOW Voltage	V_{OL}		—	—	*0.4*	—	—	*0.4*	*V*
Output HIGH Voltage	V_{OH}		*2.4*	—	—	*2.4*	—	—	*V*
Output Leakage Current	$\lvert I_{OZ} \rvert$	*High Z*	—	—	*10*	—	—	*10*	*µA*
Pullup Resistor Input Current	$\lvert I_{IL} \rvert$	$V_I = V_{SS}$	—	*50*	—	—	*50*	—	*µA*

ELECTRICAL CHARACTERISTICS FOR 3.3 V POWER SUPPLY

V_{DD} = 3.15 to 3.45 V, T_A = – 0 to + 70°C

Parameter	Symbol	Condition	TTL Level			CMOS Level			Unit
			Min	Typ	Max	Min	Typ	Max	
Input LOW Voltage	V_{IL}		—	—	*0.8*	—	—	*1.0*	*V*
Input HIGH Voltage	V_{IH}		*2.0*	—	—	*2.3*	—	—	*V*
Output LOW Voltage	V_{OL}		—	—	*0.4*	—	—	*0.4*	*V*
Output HIGH Voltage	V_{OH}		*2.4*	—	—	*2.4*	—	—	*V*

I/O CHARACTERISTICS

Input	Interface Level
AD0 – AD31	PCI
PAR	PCI
C/$\overline{BE0}$ – C/$\overline{BE3}$	PCI
$\overline{RST}$	PCI
$\overline{FRAME}$	PCI
$\overline{IRDY}$	PCI
$\overline{TRDY}$	PCI
$\overline{STOP}$	PCI
IDSEL	PCI
$\overline{DEVSEL}$	PCI
$\overline{GNT}$	PCI
$\overline{PERR}$	PCI
DAUX0 – DAUX7	TTL
C4IO	TTL, Internal Pullup Resistor
F0IO	TTL, Internal Pullup Resistor
STIO1 – STIO2	TTL, Internal Pullup Resistor
EE_SDA	TTL, Internal Pullup Resistor
EE_SCL/EN	TTL, Internal Pullup Resistor

	Driver Capability			
	Low		High	
Output	0.4 V	0.6 V	V_{DD} – 0.4 V	Unit
AD0 – AD31*	6	—	3	mA
PAR*	6	—	3	mA
C/$\overline{BE0}$ – C/$\overline{BE3}$*	6	—	3	mA
$\overline{FRAME}$	6	—	3	mA
$\overline{IRDY}$*	6	—	3	mA
$\overline{TRDY}$*	6	—	3	mA
$\overline{STOP}$*	6	—	3	mA
$\overline{DEVSEL}$*	6	—	3	mA
$\overline{REQ}$*	6	—	3	mA
$\overline{PERR}$*	6	—	3	mA
$\overline{SERR}$*	6	—	3	mA
PME	2	—	1	mA
$\overline{INTA}$*	6	—	3	mA
DAUX0 – DAUX7	4	—	2	mA
$\overline{AUX\_WR}$	2	—	1	mA
$\overline{AUX\_RD}$	2	—	1	mA
$\overline{ADR\_WR}$	8	—	4	mA
TX2_HI	6	—	3	mA
$\overline{TX1\_LO}$	6	—	3	mA
$\overline{TX\_EN}$	4	—	2	mA
$\overline{TX2\_LO}$	6	—	3	mA
TX1_HI	6	—	3	mA
ADJ_LEV	1	—	0.5	mA
C4IO	8	—	4	mA
F0IO	8	—	4	mA
STIO1 – STIO2	8	—	4	mA
F1_A – F1_B	6	—	3	mA
EE_SDA	1	—	0.5	mA
EE_SCL/EN	1	—	0.5	mA

*All PCI buffers are PCI Spec. 2.1 compliant.

SECTION 6
TIMING CHARACTERISTICS

6.1 PCI BUS TIMING

The timing characteristics of the MC145575 integrated PCI bus interface is compliant with version 2.1 of the PCI Local Bus specification.

6.2 GCI/IOM2 BUS CLOCK AND DATA ALIGNMENT FOR MITEL ST BUS

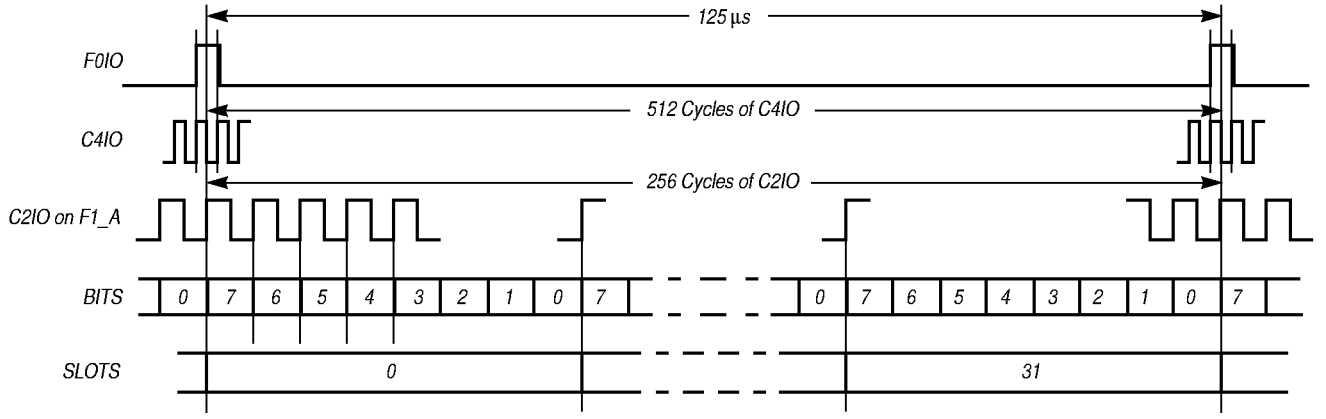
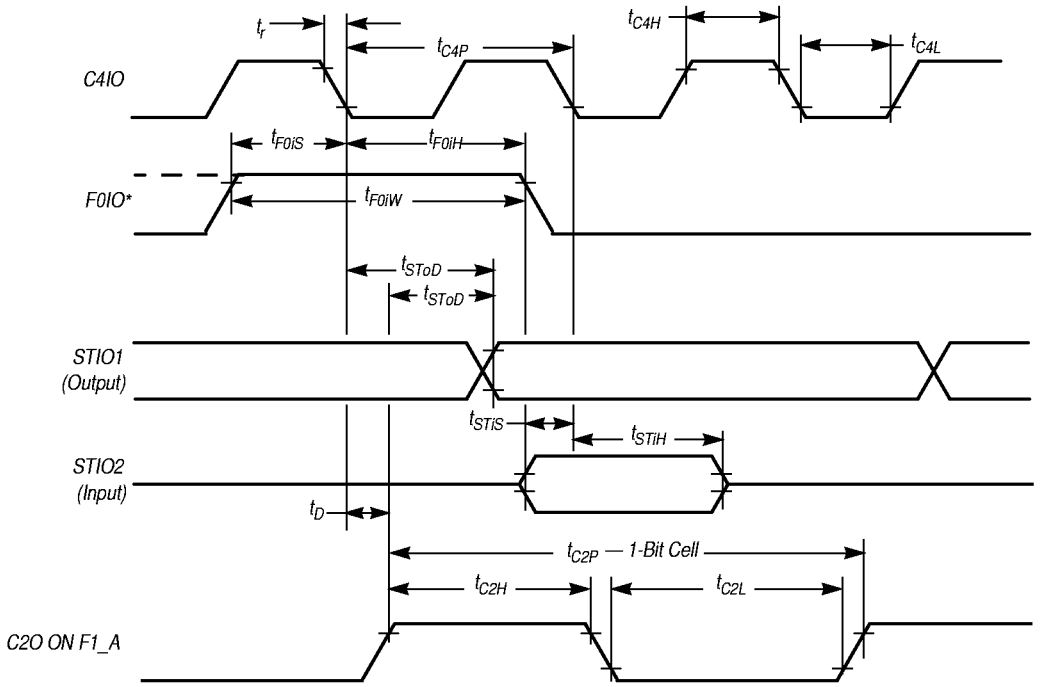


Figure 6–1. GCI/IOM2 Bus Clock and Data Alignment

6.3 GCI/IOM2 TIMING



**F0IO starts one C4IO clock earlier if bit 3 in MST_MODE register is set. If this bit is set, F0IO is also awaited one C4IO clock cycle earlier.*

Figure 6–2. GCI/IOM2 Timing Diagram

Symbol	Characteristics	Min	Max	Unit
t_{C4P}	Clock C4IO Period (4.096 MHz)	243.9	244.4	ns
t_{C4H}	Clock C4IO High Width	110	134	ns
t_{C4L}	Clock C4IO Low Width	110	134	ns
t_{C2P}	Clock C2O Period	487.8	488.8	ns
t_{C2H}	Clock C2O High Width	220	268	ns
t_{F0iS}	F0IO Setup Time	50	150	ns
t_{F0iH}	F0IO Hold Time	50	150	ns
t_{F0iW}	F0IO Width	200	300	ns
t_{SToD}	STIO1 Delay Level 1 Output	20	125	ns
t_{SToD}	STIO1 Delay Level 2 Output	20	125	ns
t_{STiS}	STIO2 Setup Time	30	—	ns
t_{STiH}	STIO2 Hold Time	2	30	ns

All specifications are for 2.048 Mbps Streams and f_{CLK} = 12.288 MHz.

6.4 EEPROM ACCESS

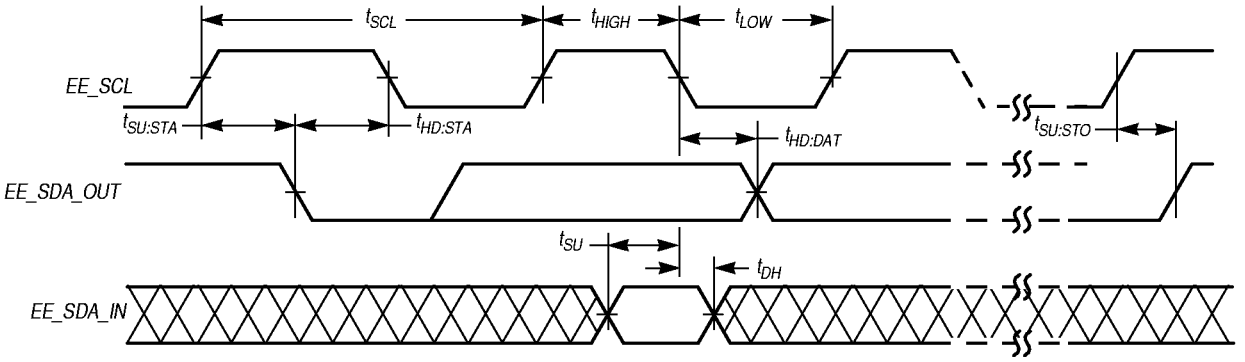


Figure 6–3. EEPROM Access Timing Diagram

Symbol	Characteristics	Typ	Unit
f_{SCL}	Serial Clock Frequency	32.2*	kHz
t_{SCL}	Serial Clock Period	1 / f_{SCL}	
$t_{HD:STA}$	Start Condition Hold Time	3/4 t_{SCL}	
t_{LOW}	Clock Low Period	1/2 t_{SCL}	
t_{HIGH}	Clock High Period	1/2 t_{SCL}	
$t_{SU:STA}$	Start Condition Setup Time	3/4 t_{SCL}	
$t_{HD:DAT}$	Output Data Change After Clock↓	10	ns
t_{SU}	Data In Setup Time	100	ns
t_{DH}	Data In Hold Time	100	ns

*With 33 MHz PCI clock.

SECTION 7
S/T INTERFACE CIRCUITRY

In order to comply to the physical requirements of ITU-T recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the MC145575 needs some additional circuitry, which is shown in the following figures.

7.1 EXTERNAL RECEIVER CIRCUITRY

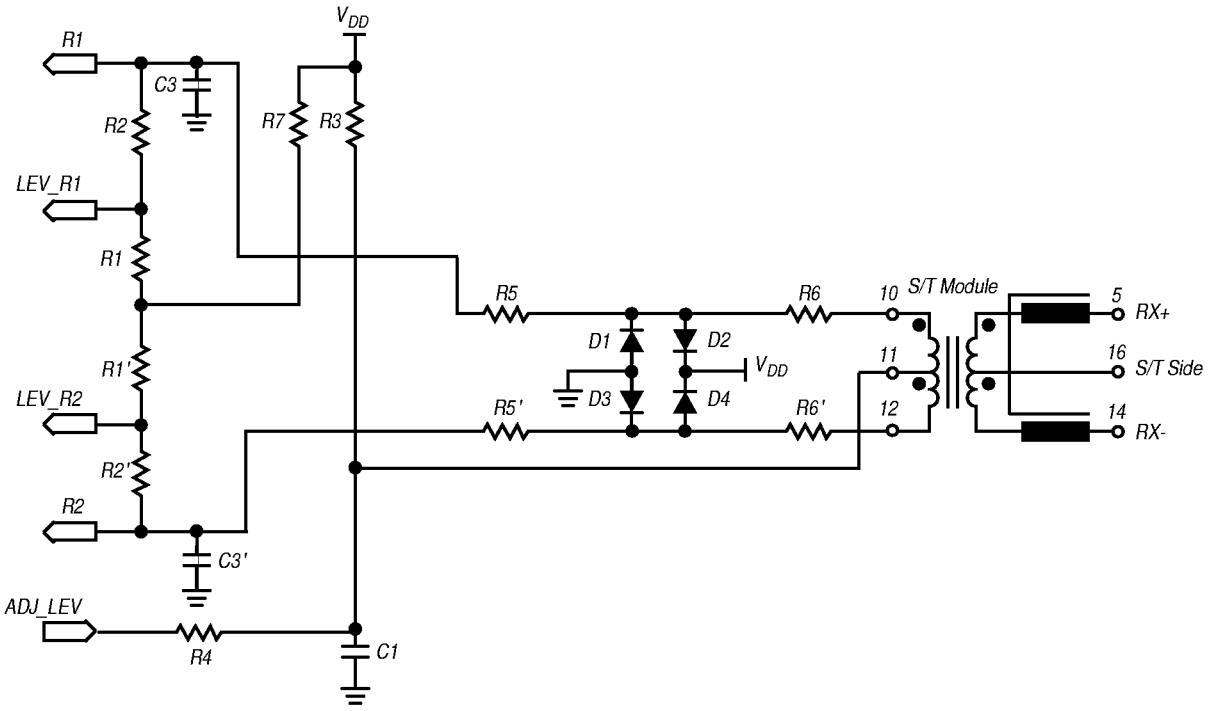


Figure 7–1. External Receiver Circuitry

PARTS LIST

V_{DD}	5 V	3.3 V
R1, R1'	33 kΩ	
R2, R2'	100 kΩ	
R3	1 MΩ	680 kΩ
R4	3.9 kΩ	
R5, R5'	4.7 kΩ	
R6, R6'	4.7 kΩ	
R7	1.8 MΩ	1.2 MΩ
C1	47 nF	
C3, C3'	22 pF	
D1, D2	1N4148 or LL4148	
D3, D4	1N4148 or LL4148	
S/T Module	See Table 7–1	

C3, C3' are for reduction of high-frequency input noise and should be located as close as possible to the MC145575. All resistors are 5% tolerant, unless otherwise specified.

7.2 EXTERNAL TRANSMITTER CIRCUITRY

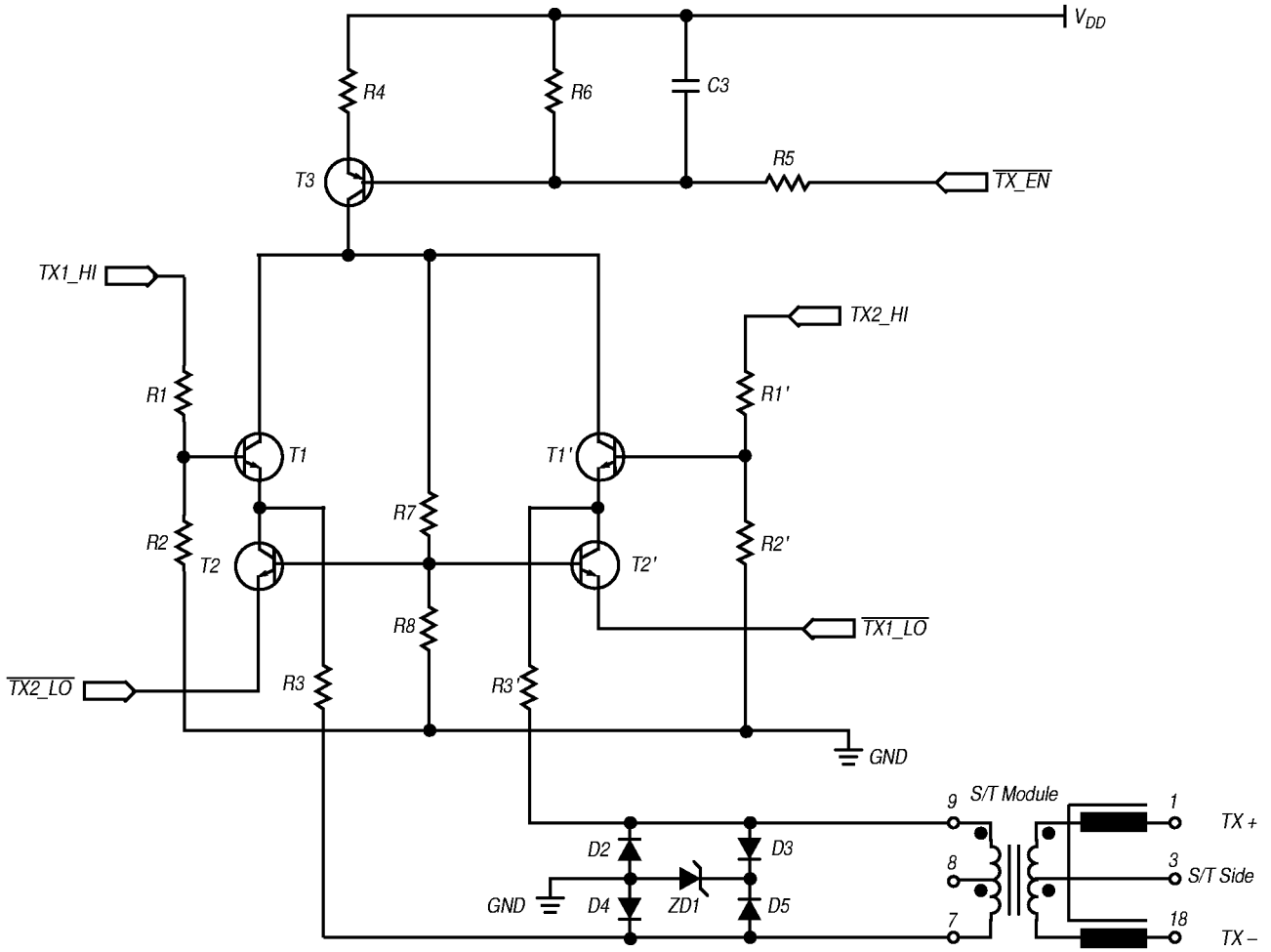


Figure 7–2. External Transmitter Circuitry

PARTS LIST

V_{DD}	5 V	3.3 V
R1, R1'	*2.2 kΩ ± 1%*	*560 Ω ± 1%*
R2, R2'	*3.0 kΩ ± 1%*	*3.9 kΩ ± 1%*
*R3, R3' **	*18 Ω*	
R4	*100 Ω*	*50 Ω*
R5	*5.6 kΩ*	*3.3 kΩ*
R6	*3.3 kΩ*	*2.2 kΩ*
R7	*3.3 kΩ*	*1.8 kΩ*
R8	*2.2 kΩ*	
C3	*470 pF*	
D2, D3	*1N4148 or LL4148*	
D4, D5	*1N4148 or LL4148*	
ZD1	*Z-Diode 2.7 V (e.g., BZV 55C 2V7)*	
T1, T1'	*BC550C, BC850C, or Similar*	
T2, T2'	*BC550C, BC850C, or Similar*	
T3	*BC560C, BC860C, or Similar*	
S/T Module	*See Table 7–1*	

**Value depends on the S/T module used.*

Table 7–1. S/T Module Part Numbers for Advanced Power Components

Part Number	Description
APC5568-3V	*Pin Through Package for 3.3 V Applications*
APC5568-5V	*Pin Through Package for 5.0 V Applications*
APC5568DS-3V	*SMD Package for 3.3 V Applications*
APC5568DS-5V	*SMD Package for 5.0 V Applications*

Table 7–2. S/T Module Manufacturers

Manufacturer	Address or Web Site
Advanced Power Components	*United Kingdom* *Phone: +44 1634-290588* *Fax: +44 1634-290591* *http://www.apcisdn.com*
FEE GmbH	
Pulse Engineering, Inc.	*http://www.pulseeng.com*
VAC GmbH	*http://www.vacuumschmelze.de*
Valor Electronics, Inc.	*http://www.valorinc.com*
Vogt Electronic AG	*http://www.vogt-electronic.com*
UMEC GmbH	*http://www.umec.de*

7.3 OSCILLATOR CIRCUITRY

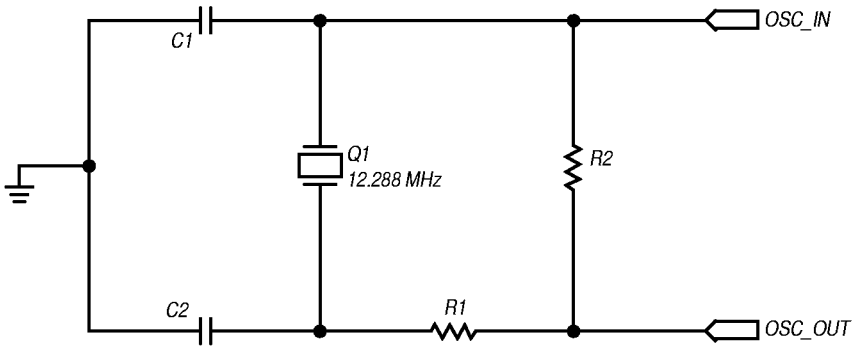


Figure 7–3. Oscillator Circuitry

The values of C1, C2, and R1 depend on the quartz used.

For a load-free check of the oscillator frequency, the C4O clock of the GCI/IOM2 bus should be measured (MC145575 as master, S/T interface deactivated, 4.096 MHz frequency intended on the C4IO).

Table 7–3. Crystal Specifications

Parameter	Value
Frequency	*12.288 MHz*
Adjustment Tolerance @ 25°C	*± 30 ppm*
Load Capacitance	*30 pF (preferred)*
Frequency Stability in Operating Temperature Range	*± 50 ppm*
Operating Temperature Range	*- 20 to + 70°C*
Drive Level	*0.1 mW*
Aging	*< 5 ppm/year*

7.4 EEPROM CIRCUITRY

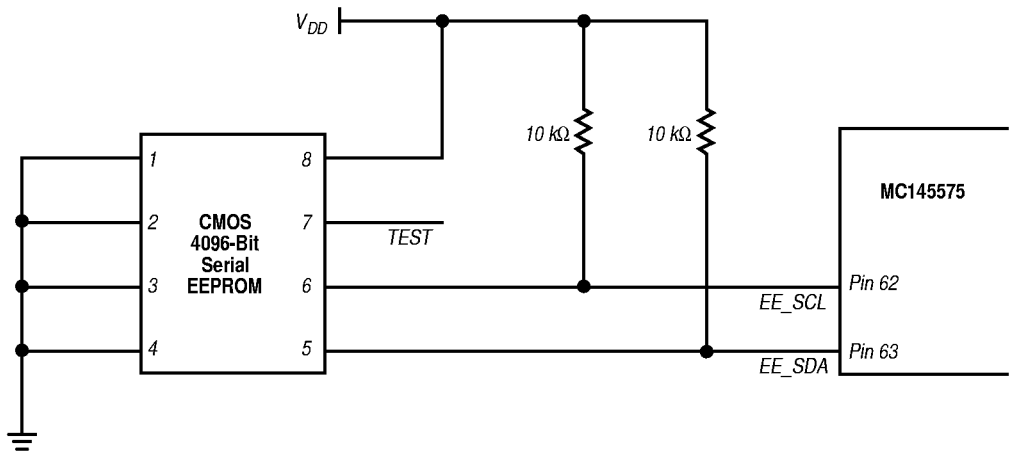


Figure 7–4. EEPROM Circuitry

7.5 PME PIN CIRCUITRY

The PME pin (pin 53) on the MC145575 is active high. To connect it to the active low $\overline{PME}$ pin on the PCI bus, the following circuitry is necessary.

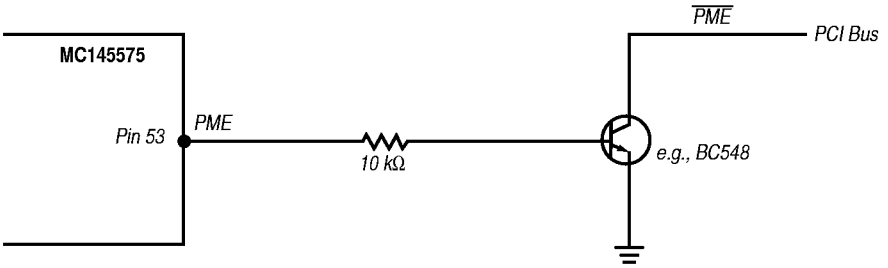


Figure 7–5. PME Pin Circuitry

SECTION 8
STATE MATRICES FOR NT AND TE

8.1 S/T INTERFACE ACTIVATION/DEACTIVATION LAYER 1 FOR FINITE STATE MATRIX FOR NT

Table 8–1. Activation/Deactivation Layer 1 for Finite State Matrix for NT

State Name / Event	Reset	Deactive	Pending Activation	Active	Pending Deactivation
State No.	G0	G1	G2	G3	G4
INFO Sent	INFO 0	INFO 0	INFO 2	INFO 4	INFO 0
State Machine Release (Note 1)	G2	|	|	|	|
Activate Request	G2 (Note 2)	G2 (Note 2)	|	|	G2 (Note 2)
Deactivate Request	—	|	Start Timer T2 G4	Start Timer T2 G4	|
Expiry T2 (Note 3)	—	—	—	—	G1
Receiving INFO 0	—	—	—	G2	G1
Receiving INFO 1	—	G2 (Note 2)	—	/	—
Receiving INFO 3	—	/	G3 (Note 2)	—	—
Lost Framing	—	/	/	G2	—

_ No state change.
/ Impossible by the definition of peer-to-peer physical layer procedures for internal system reasons.
| Impossible by the definition of the physical layer service.

NOTES:
1. After reset, the state machine is fixed to G0.
2. Timer 1 (T1) is not implemented in the MC145575 and must be implemented in software.
3. Timer 2 (T2) prevents unintentional reactivation. Its value is 32 ms (256 x 125 µs). This implies that a TE has to recognize INFO 0 and react to it within this time.

8.2 ACTIVATION/DEACTIVATION LAYER 1 FOR FINITE STATE MATRIX FOR TE

Table 8–2. Activation/Deactivation Layer 1 for Finite State Matrix for TE

State Name / Event		Reset	Sensing	Deacti-vated	Awaiting Signal	Identifying Input	Synchron-ized	Activated	Lost Framing
State No.		F0	F2	F3	F4	F5	F6	F7	F8
INFO Sent		INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
State Machine Release (Note 1)		F2	/	/	/	/	/	/	/
Activate Request	Receiving Any Signal	—	|	F5	|	|	—	|	—
	Receiving INFO 0	—	|	F4	|	|	—	|	—
Expiry T3 (Note 2)		—	/	—	F3	F3	F3	—	—
Receiving INFO 0		—	F3	—	—	—	F3	F3	F3
Receiving Any Signal (Note 3)		—	—	—	F5	—	/	/	—
Receiving INFO 2 (Note 4)		—	F6	F6	F6	F6	—	F6	F6
Receiving INFO 4 (Note 4)		—	F7	F7	F7	F7	F7	—	F7
Lost Framing (Note 5)		—	/	/	/	/	F8	F8	—

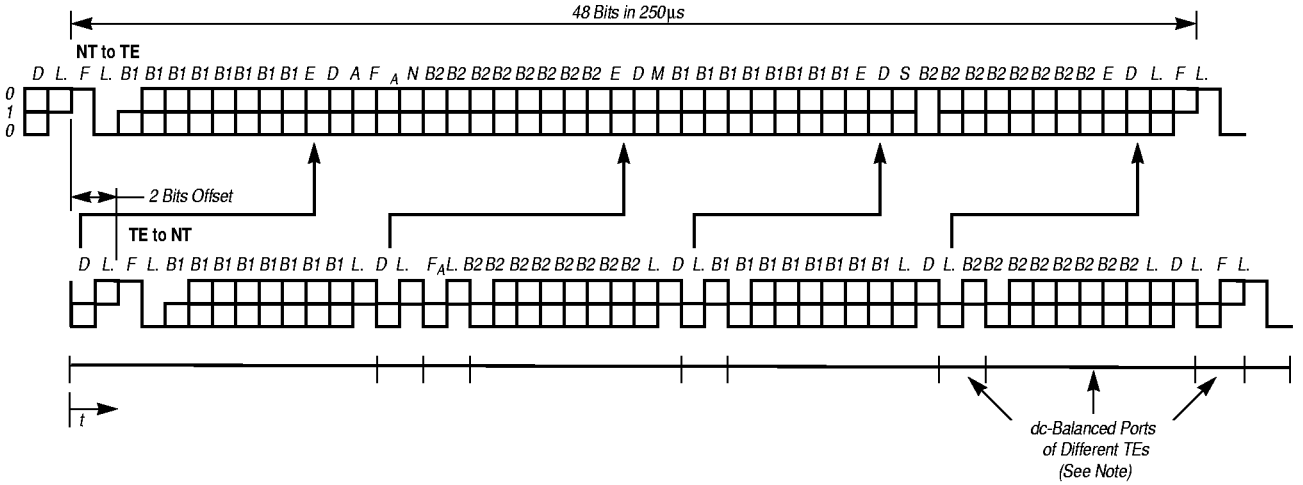
_ No change, no action.
/ Impossible by the definition of layer 1 service.
| Impossible situation.

NOTES:
1. After reset, the state machine is fixed to F0.
2. Timer 3 (T3) is not implemented in the MC145575 and must be implemented in software.
3. This event reflects the case where a signal is received and the TE has not (yet) determined whether it is INFO 2 or INFO 4.
4. Bit- and frame-synchronization achieved.
5. Loss of bit- or frame-synchronization.

SECTION 9
BINARY ORGANIZATION OF THE FRAMES

9.1 S/T FRAME STRUCTURE

The frame structures are different for each direction of transmission. Both structures are illustrated in Figure 9–1.



F	Framing bit	N	Bit set to a binary value $N - \overline{F}_A$ (NT to TE)
L	dc balancing bit	B1	Bit within B-channel 1
D	D-channel bit	B2	Bit within B-channel 2
E	D-echo-channel bit	A	Bit used for activation
F_A	Auxiliary framing bit	S	S-channel bit
M	Multiframing bit		

Figure 9–1. Frame Structure at Reference Point S and T

NOTE

Lines demarcate those parts of the frame that are independently dc-balanced.

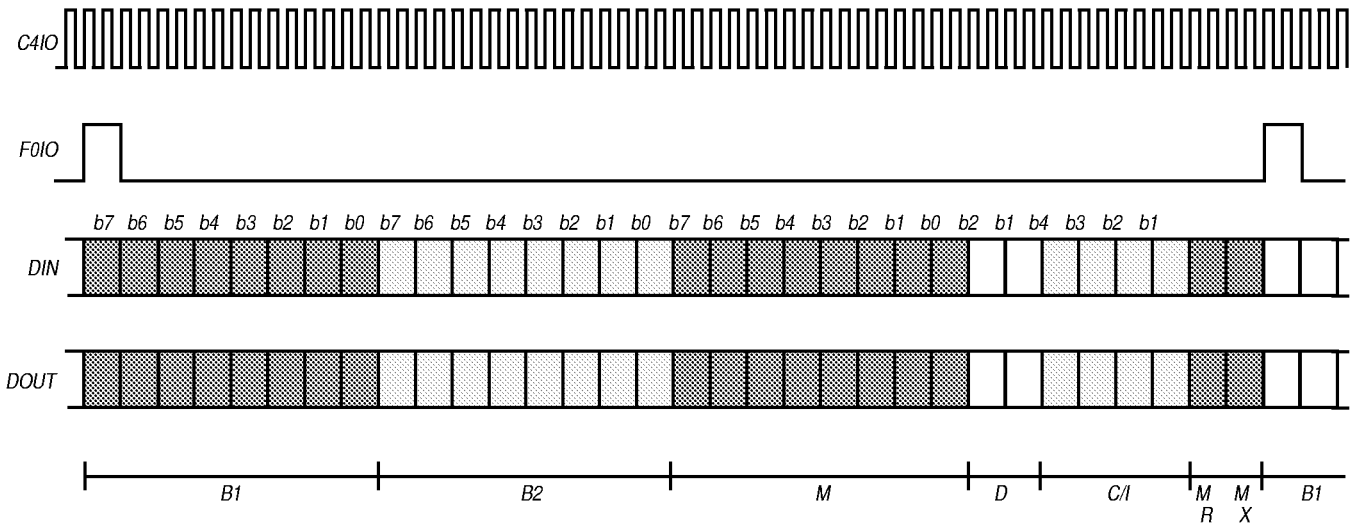
The F_A bit in the direction TE to NT is used as Q bit in every fifth frame if S/Q bit transmission is enabled (see SCTRL register).

The nominal 2-bit offset is as seen from the TE. The offset can be adjusted with the CLKDEL register in TE mode. The corresponding offset at the NT may be greater due to delay in the interface cable and varies by configuration.

HDLC-B-channel data start with the LSB, PCM-B-channel data start with the MSB.

9.2 GCI FRAME STRUCTURE

The binary organization of a single GCI channel frame is described below.



B1	B-channel 1 data	C/I	Command/indication bits for controlling activation/deactivation and for additional control functions
B2	B-channel 2 data	MR	Handshake bit for monitor channel
M	Monitor channel data	MX	Handshake bit for monitor channel
D	D-channel data		

Figure 9–2. Single Channel GCI Format

SECTION 10
CLOCK SYNCHRONIZATION

10.1 CLOCK SYNCHRONIZATION IN NT MODE

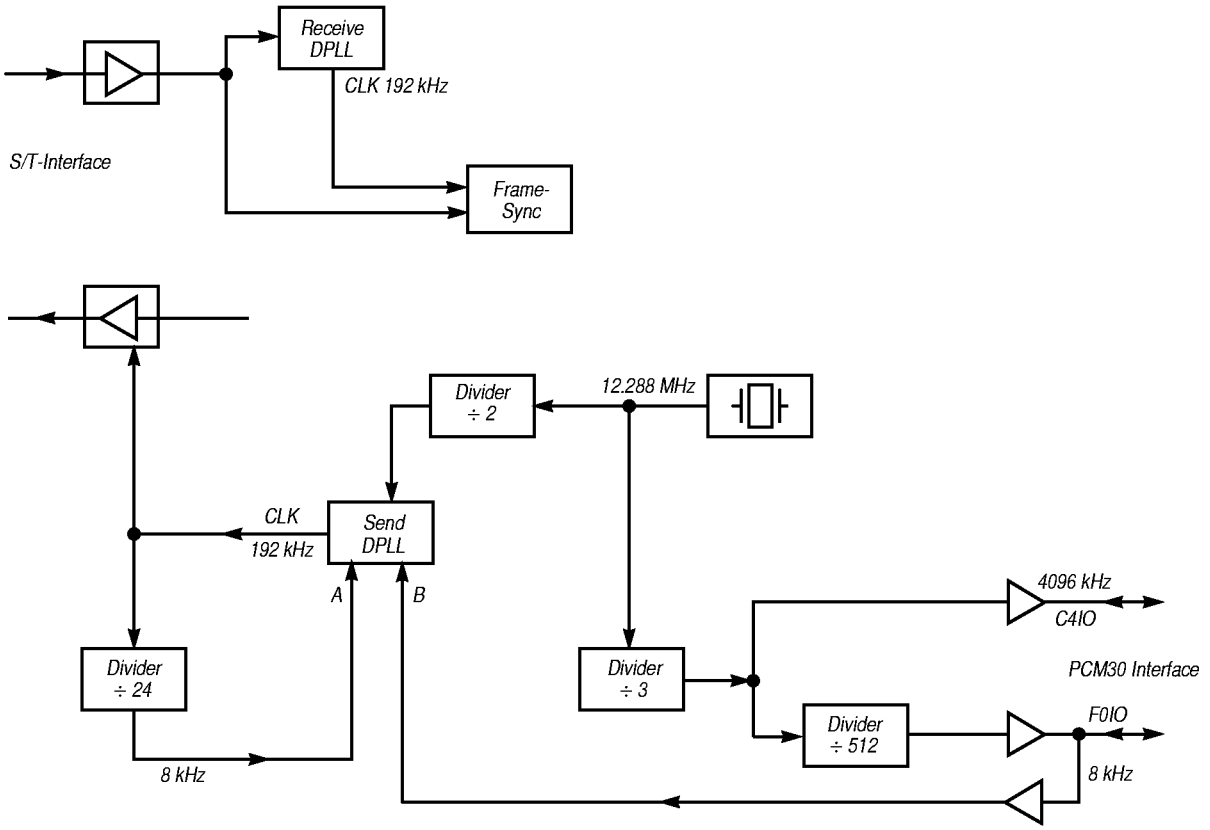


Figure 10–1. Clock Synchronization in NT Mode

10.2 CLOCK SYNCHRONIZATION IN TE MODE

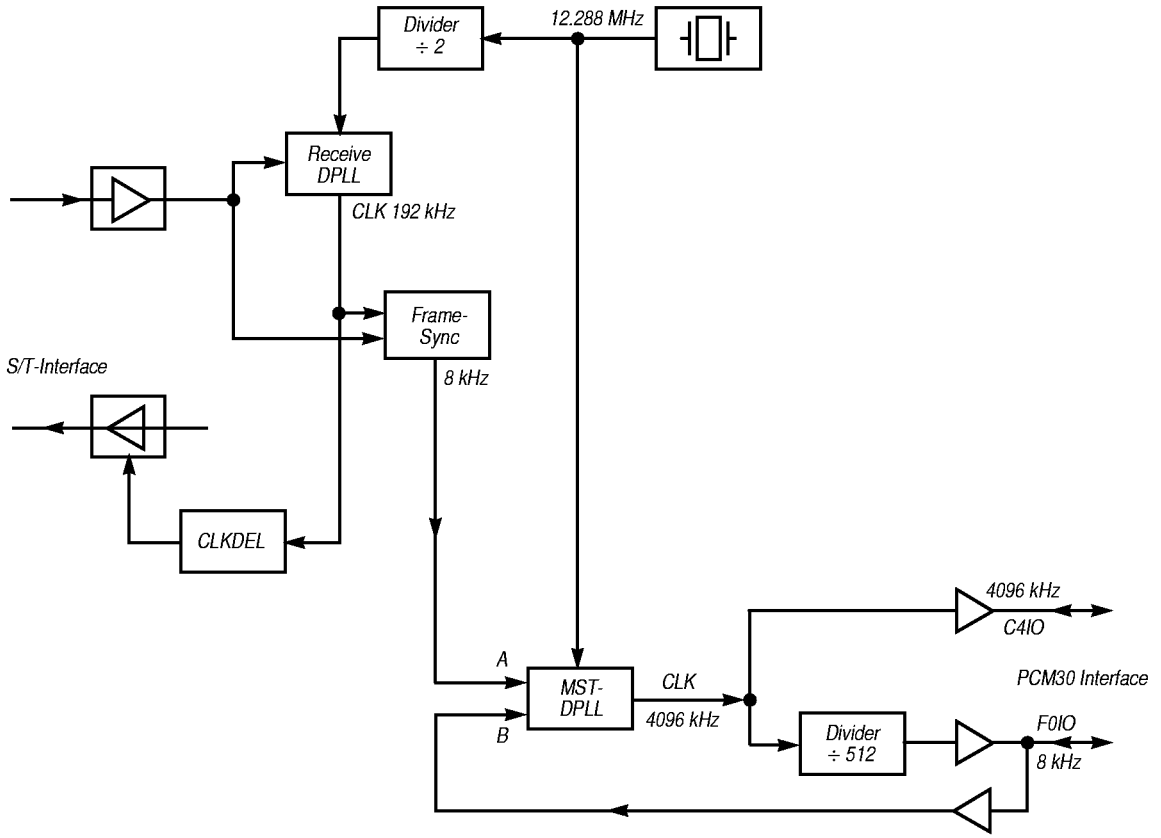
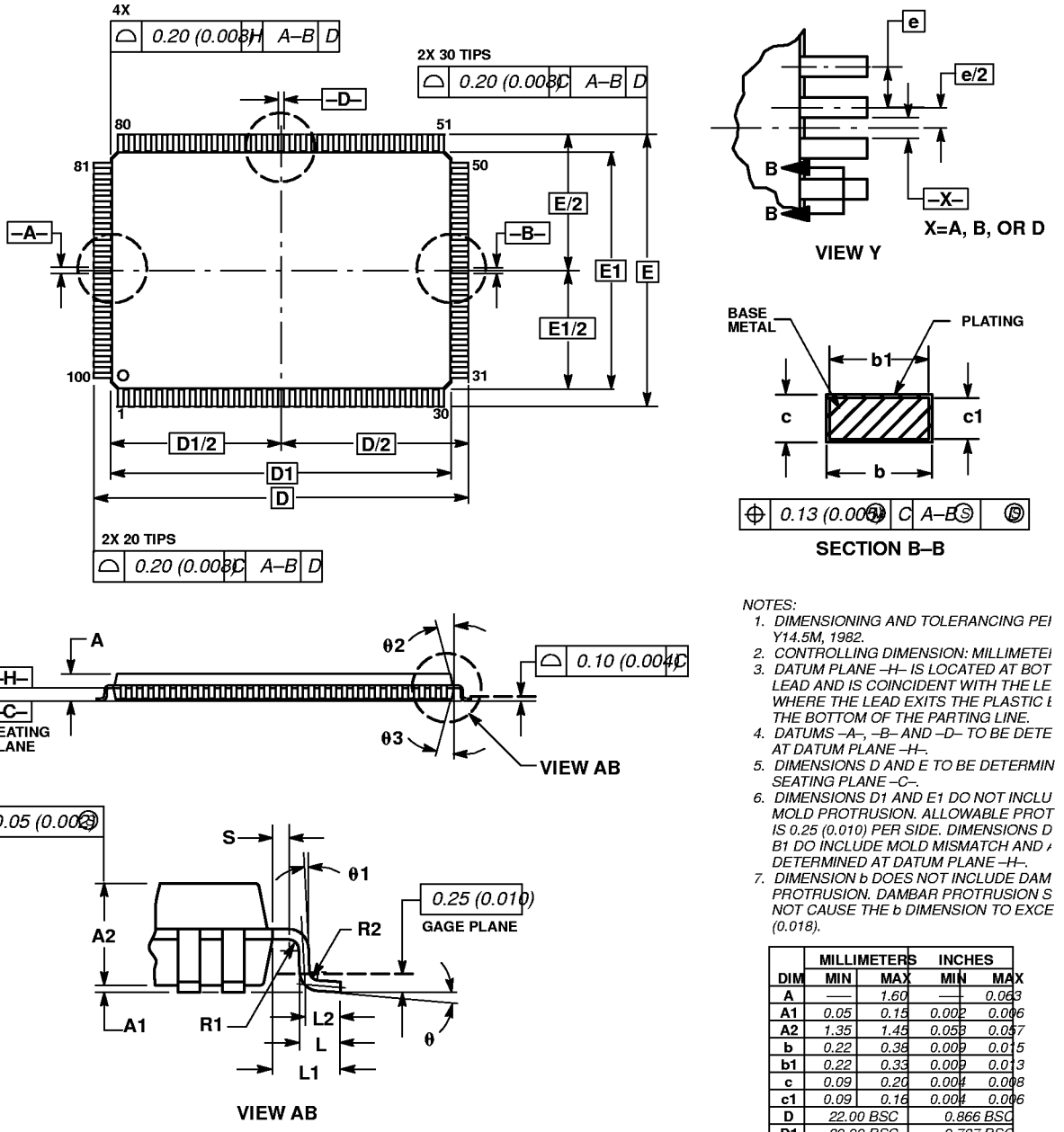


Figure 10–2. Clock Synchronization in TE Mode

The C4IO clock is adjusted in timeslot 31 at the GCI/IOM bus twice for half a clock cycle. This can be reduced to one adjustment of half a clock cycle. This is useful if another MC145575 is connected as a slave in the NT mode to the GCI/IOM2 bus.

SECTION 11
MC145575 PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PEI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETEI
3. DATUM PLANE –H– IS LOCATED AT BOT LEAD AND IS COINCIDENT WITH THE LE WHERE THE LEAD EXITS THE PLASTIC E THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETE AT DATUM PLANE –H–.
5. DIMENSIONS D AND E TO BE DETERMIN SEATING PLANE –C–.
6. DIMENSIONS D1 AND E1 DO NOT INCLU MOLD PROTRUSION. ALLOWABLE PROT IS 0.25 (0.010) PER SIDE. DIMENSIONS D B1 DO INCLUDE MOLD MISMATCH AND A DETERMINED AT DATUM PLANE –H–.
7. DIMENSION b DOES NOT INCLUDE DAM PROTRUSION. DAMBAR PROTRUSION S NOT CAUSE THE b DIMENSION TO EXCE (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	—	0.008	—
R1	0.08	—	0.003	—
R2	0.08	0.20	0.003	0.008
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	11°	13°	11°	13°
θ3	11°	13°	11°	13°

Figure 11–1. MC145575 Package Dimensions – Case 983A-01 (Quad Flat Package)

SECTION 12
REFERENCE DESIGN
AND APPLICATION SCHEMATICS

12.1 REFERENCE DESIGN

This section describes the Motorola PCI Passive ISDN TA reference design (MISDN/TA/PCIEVK) with ISDN software stack and drivers. The MISDN/TA/PCIEVK is a highly integrated single-chip solution with up to 128 kbps high-speed internet access via ISDN. This plug and play card is a cost-effective PCI solution, offering customers a productizable reference platform for faster time-to-market. The full turnkey design includes schematics, Gerber files, bill of materials, and software.

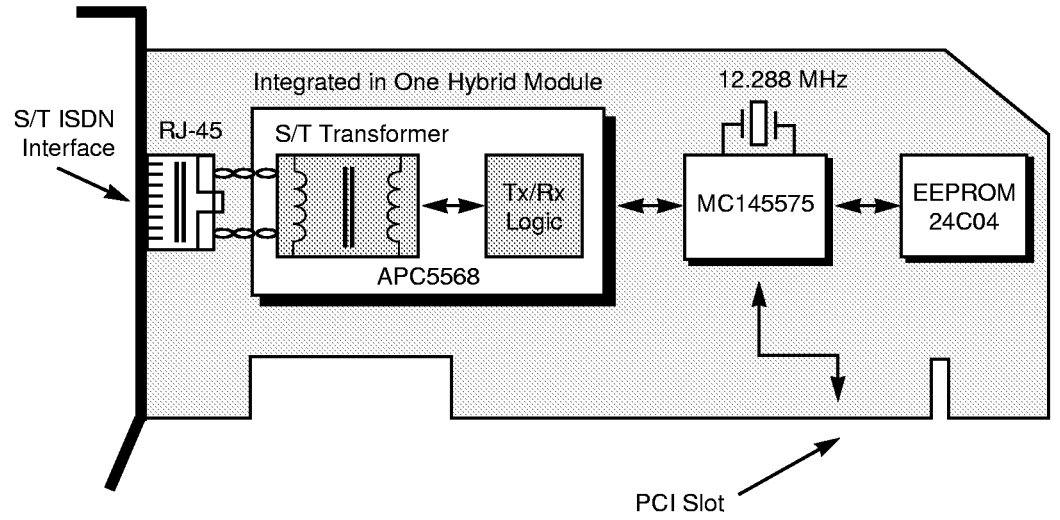


Figure 12–1. MISDN/TA/PCIEVK Block Diagram

12.1.1 Software

This card is bundled with the essential ISDN software stack and drivers. The license is available from Motorola. The software addresses the requirements of ISDN CAPI 2.0 and NDIS WAN, with additional drivers for a variety of Windows environments and different D channel protocols to meet specific customer and market requirements.

- *Supports Windows™ 95/98 VxD Driver with Power Management*
- *Windows NT™ 4.0 Driver*
- *Windows 98/Windows NT 5.0 WDM Driver**
- *Multi-Language Support*
- *B Channel Protocol Transparent and HDLC Supported*
- *Supports D Channel Protocols*
- *CAPI 2.0*
- *NDIS WAN Miniport (PPP/MLPPP)**
- *Multi-Link PPP Aggregates Both B Channels to Provide Full 128 kbps*

**NOTE: Check with your local Motorola sales office or distributor for availability.*

12.1.2 Ordering Information

The reference design kit part number is MISDN/TA/PCIEVK. Contact your local Motorola sales office or distributor for more information.

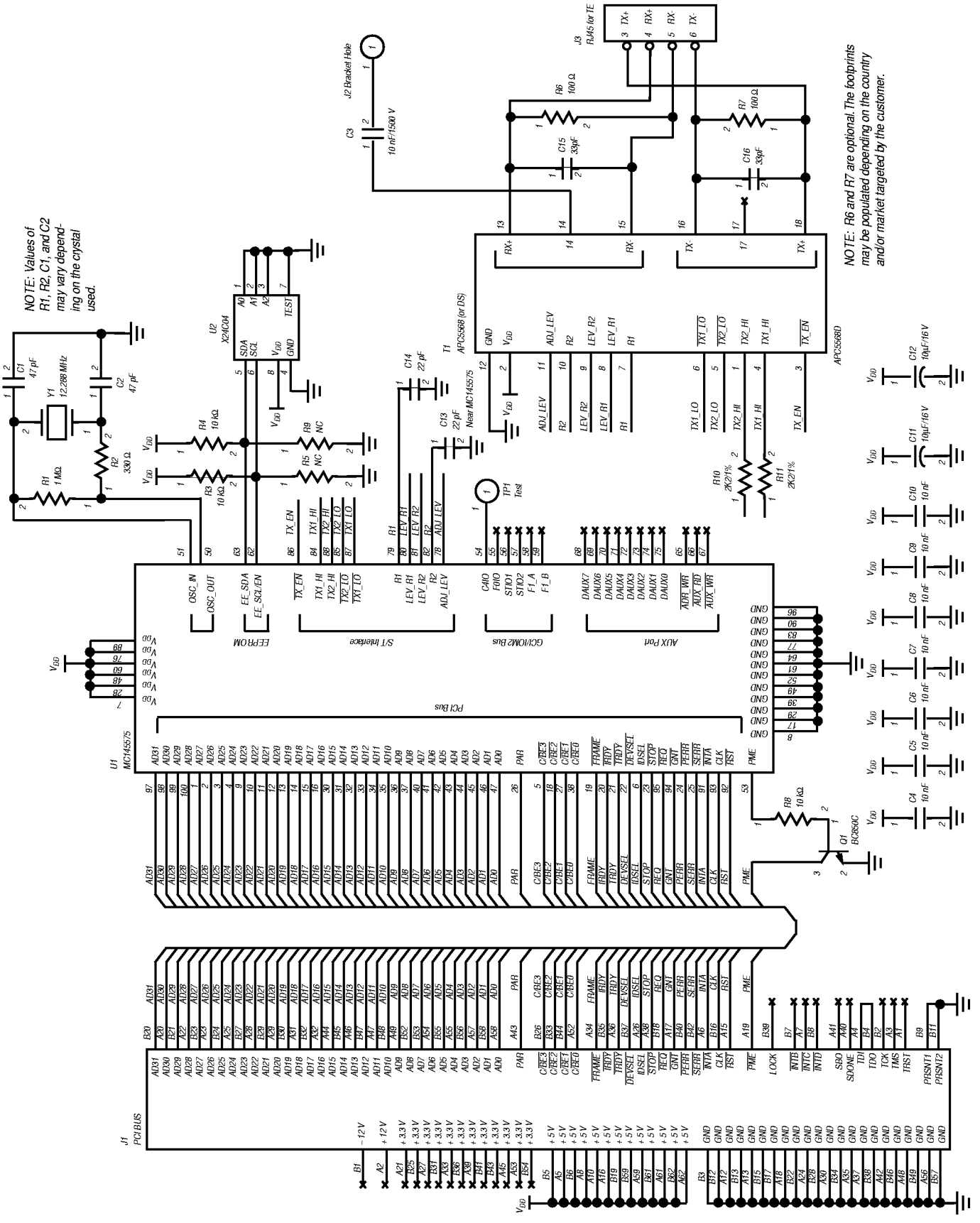


Figure 12–2. 5 V MC145575 Reference Board

Table 12–1. Bill of Materials for 5 V MC145575 Reference Board

Item	Qty.	Description	Reference	Reference Designator	Manufacturer
1	*2*	*Capacitor 0805*	*47 pF*	*C1, C2*	
2	*1*	*Capacitor*	*10 nF / 1500 V*	*C3*	
3	*7*	*Capacitor 0805*	*10 nF*	*C4, C5, C6, C7, C8, C9, C10*	
4	*2*	*Capacitor*	*10 µF / 16 V*	*C11, C12*	
5	*2*	*Capacitor 0805*	*22 pF*	*C13, C14*	
6	*2*	*Capacitor 0805*	*33 pF*	*C15, C16*	
7	*1*	*PCI Bracket*	*GDI 0320*		
8	*1*	*RJ45 Connector*	*95001-2881 (or 6881)*	*J3*	
9	*1*	*Transistor SOT23*	*BC850C*	*Q1*	
10	*1*	*Resistor 0805*	*1M / 5%*	*R1*	
11	*1*	*Resistor 0805*	*330 / 5%*	*R2*	
12	*3*	*Resistor 0805*	*10k / 5%*	*R3, R4, R8*	
13	*2*	*Resistor 0805*	*100 / 5%*	*R6, R7*	
14	*2*	*Resistor 0805*	*2K2 / 1%*	*R10, R11*	
15	*1*	*Hybrid Module*	*APC5568DS-5V*	*T1*	*APC*
16	*1*	*ISDN Transceiver*	*MC145575FU*	*U1*	*Motorola*
17	*1*	*EEPROM*	*X24C04S8*	*U2*	
18	*1*	*Crystal*	*12.288 MHz - TQ3330S*	*Y1*	*LPE-Téléquartz*

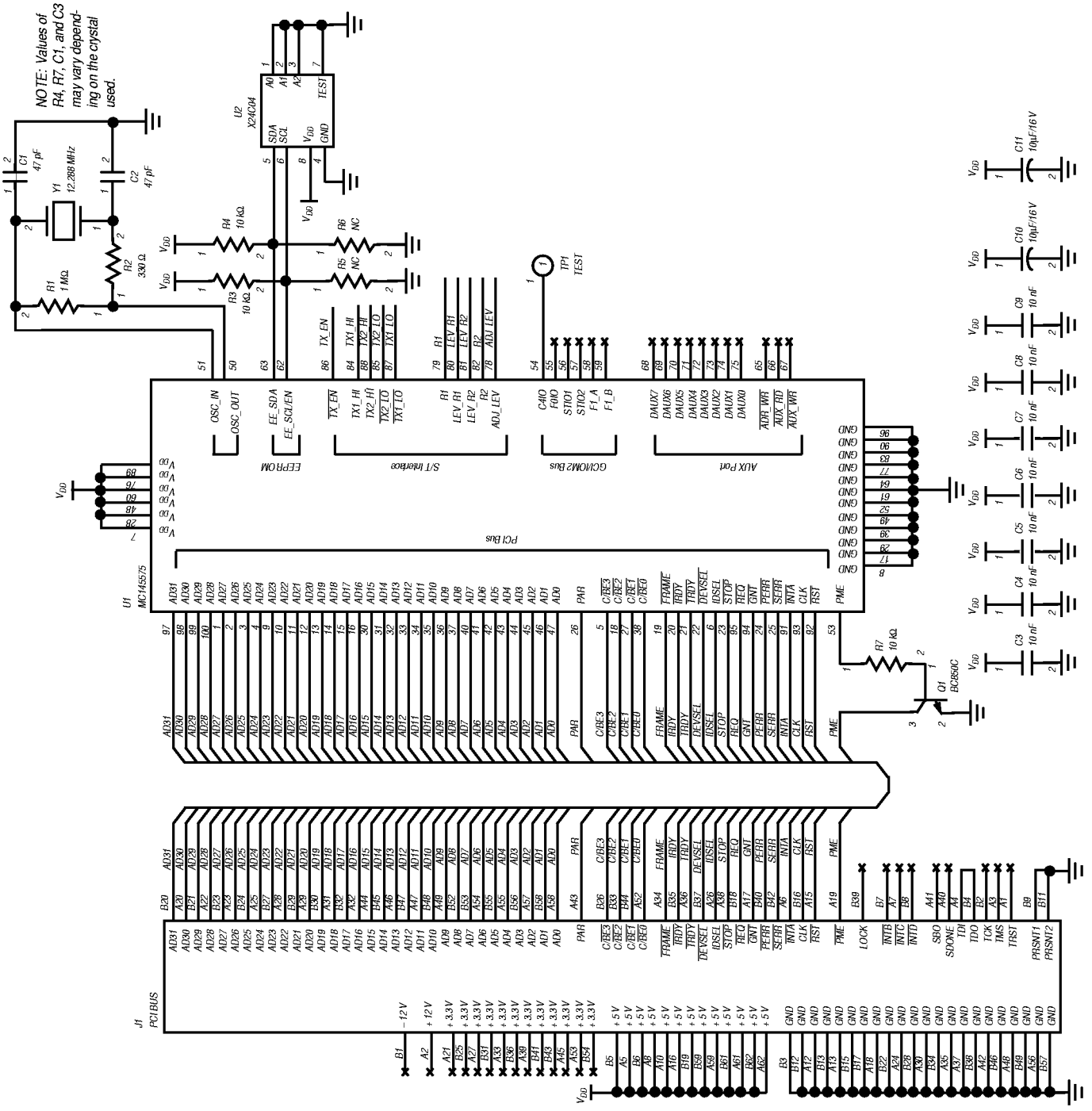


Figure 12–3. 5 V MC145575 Application Schematics — Part 1

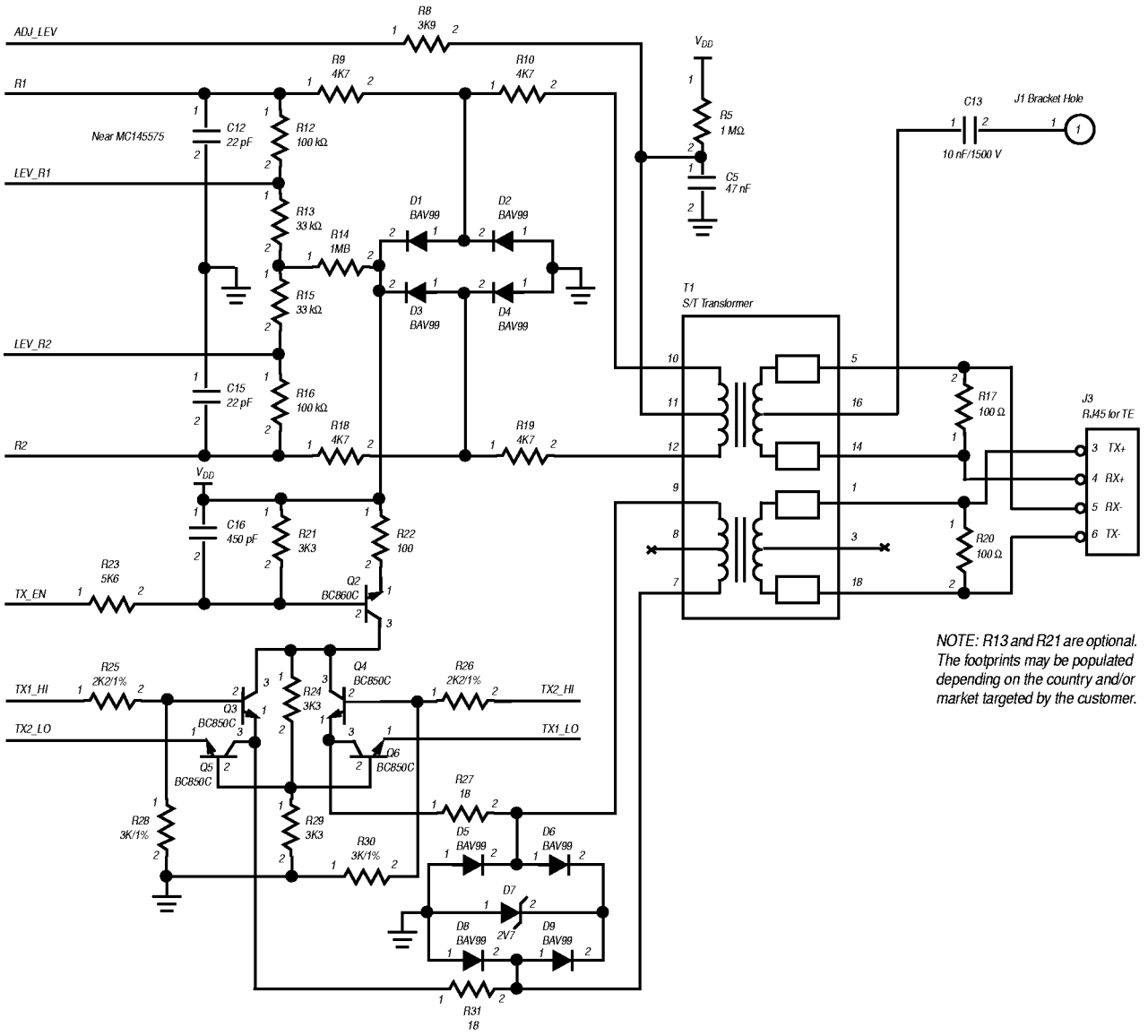


Figure 12–4. 5 V MC145575 Application Schematics — Part 2

Table 12–2. Bill of Materials for 5 V MC145575 Application with Discrete AFE

Item	Qty.	Description	Reference	Reference Designator
1	2	Capacitor	47 pF	C1, C2
2	2	Capacitor	22 pF	C2, C6
3	1	Capacitor	10 nF / 1500 V	C13
4	1	Capacitor	47 nF	C5
5	1	Capacitor	470 pF	C7
6	7	Capacitor	10 nF	C3, C4, C5, C6, C7, C8, C9
7	2	Capacitor	10 μF / 16 V	C10, C11
8	8	Diode	BAV99	D1, D2, D3, D4, D5, D6, D8, D9
9	1	Zener Diode	2V7	D7
10	1	PCI Bracket	GDI 0320	
11	1	RJ45 Connector	95001-2881 (or 6881)	J3
12	1	Transistor	BC860C	Q2
13	2	Transistor	BC850C	Q1, Q3, Q4, Q5, Q6
14	1	Resistor	3K9 / 5% / 0805	R8, R9
15	4	Resistor	4K7 / 5% / 0805	R9, R10, R18, R19
16	2	Resistor	1M / 5% / 0805	R1, R11
17	2	Resistor	100K / 5% / 0805	R12, R16
18	1	Resistor	330 / 5% / 0805	R2
19	2	Resistor	33K / 5% / 0805	R13, R15
20	1	Resistor	1M8 / 5% / 0805	R14
21	3	Resistor	10K / 5% / 0805	R3, R4, R7
22	3	Resistor	100 / 5% / 0805	R17, R20, R22
23	3	Resistor	3K3 / 5% / 0805	R21, R24, R29
24	1	Resistor	5K6 / 5% / 0805	R23
25	2	Resistor	2K2 / 5% / 0805	R25, R26
26	2	Resistor	18 / 5% / 0805	R27, R31
27	2	Resistor	3K / 1% / 0805	R28, R30
28	1	ISDN Transformer	Cf Data Sheet	T1
29	1	ISDN Transceiver	MC145575FU	U1
30	1	EEPROM	X24C04S8	U2
31	1	Crystal	12.288 MHz - TQ3330S	Y1

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