NCP360

USB Positive Overvoltage Protection Controller with Internal PMOS FET and Status FLAG

NCP360 is able to disconnect the systems from its output pin in case wrong VBUS operating conditions is detected. The system is positive over-voltage protected up to +20 V.

Thanks to this device using internal PMOS FET, no external device is necessary, reducing the system cost and the PCB area of the application board.

NCP360 is able to instantaneously disconnect the output from the input if the input voltage exceeds the overvoltage threshold (OVLO).

NCP360 provides a negative going flag ($\overline{\text{FLAG}}$) output, which alerts the system that a fault has occurred.

In addition, the device has ESD-protected input (15 kV Air) when bypassed with a 1 μF or larger capacitor.

Features

- Very Fast Protection, Up to 20 V, with 25 μA Current Consumption
- On-chip PMOS Transistor
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Alert $\overline{\text{FLAG}}$ Output
- $\overline{\text{EN}}$ Enable Pin
- Thermal Shutdown
- Compliance to IEC61000-4-2 (Level 4)
  8 kV (Contact)
  15 kV (Air)
- ESD Ratings: Machine Model = B
  Human Body Model = 3
- 6 Lead UDFN 2x2 mm Package
- 5 Lead TSOP 3x3 mm Package
- These are Pb-Free Devices

Applications

- USB Devices
- Mobile Phones
- Peripheral
- Personal Digital Applications
- MP3 Players

ON Semiconductor®

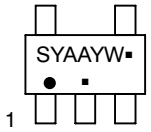
http://onsemi.com

MARKING DIAGRAMS

UDFN6
TBD SUFFIX
CASE 517AB

M = Date Code

TSOP-5
TBD SUFFIX
CASE 483



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP360MUTBG	UDFN6 (Pb-Free)	3000/Tape & Reel
NCP360MUTXG	UDFN6 (Pb-Free)	10000/Tape & Reel
NCP360SNT1G	TSOP-5 (Pb-Free)	3000/Tape & Reel
NCP360SNT3G	TSOP-5 (Pb-Free)	10000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN CONNECTIONS

(Top Views)

PIN FUNCTION DESCRIPTION (UDFN6 Package)

Pin No.	Name	Type	Description
1	$\overline{EN}$	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin shall be connected to GND to a pull down or to a I/O pin. This pin does not have an impact on the fault detection.
2	GND	POWER	Ground
3	IN	POWER	Input Voltage Pin. This pin is connected to the VBUS. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
4, 5	OUT	OUTPUT	Output Voltage Pin. The output is disconnected from the VBUS power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 μF capacitor must be connected to these pins. The two OUT pins must be hardwired to common supply.
6	$\overline{FLAG}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on VBUS pin. The $\overline{FLAG}$ pin goes low when input voltage exceeds OVLO threshold. Since the $\overline{FLAG}$ pin is open drain functionality, an external pull up resistor to V_{CC} must be added.
-	PAD1	POWER	Exposed Pad. Can be connected to GND or isolated plane. Must be used to thermal dissipation.

PIN FUNCTION DESCRIPTION (TSOP-5 Package)

Pin No.	Name	Type	Description
1	IN	POWER	Input Voltage Pin. This pin is connected to the VBUS. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
2	GND	POWER	Ground
3	$\overline{EN}$	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin shall be connected to GND to a pull down or to a I/O pin. This pin does not have an impact on the fault detection.
4	$\overline{FLAG}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on VBUS pin. The $\overline{FLAG}$ pin goes low when input voltage exceeds OVLO threshold. Since the $\overline{FLAG}$ pin is open drain functionality, an external pull up resistor to V_{CC} must be added.
5	OUT	OUTPUT	Output Voltage Pin. The output is disconnected from the VBUS power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 μF capacitor must be connected to this pin.

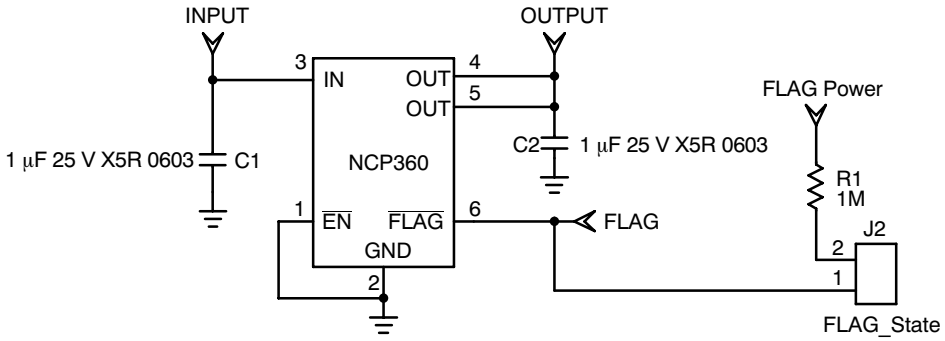


Figure 1. Typical Application Circuit (UDFN Pinout)

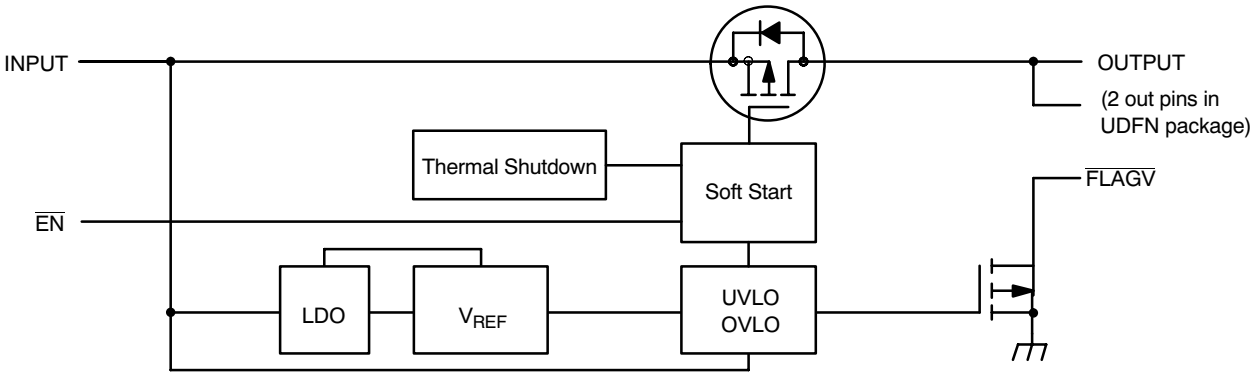


Figure 2. Functional Block Diagram

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Minimum Voltage (IN to GND)		$Vmin_{in}$	-0.3	V
Minimum Voltage (All others to GND)		Vmin	-0.3	V
Maximum Voltage (IN to GND)		$Vmax_{in}$	21	V
Maximum Voltage (All others to GND)		Vmax	7.0	V
Maximum Current from Vin to Vout (PMOS)		Imax	600	mA
Thermal Resistance, Junction-to-Air (Note 1)	TSOP-5 UDFN	$R_{\theta JA}$	305 260	°C/W
Operating Ambient Temperature Range		T_A	-40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Junction Operating Temperature		T_J	150	°C
ESD Withstand Voltage (IEC 61000-4-2) Human Body Model (HBM), Model = 2 (Note 2) Machine Model (MM) Model = B (Note 3)		Vesd	15 Air, 8.0 Contact 2000 200	kV V V
Moisture Sensitivity		MSL	Level 1	-

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. $R_{\theta JA}$ is highly dependent on the PCB heat sink area (connected to PAD1, UDFN). See PCB Recommendations.
2. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
3. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
4. Compliant with JEDEC Latch-up Test, up to maximum voltage range.

ELECTRICAL CHARACTERISTICS

(Min/Max limits values (-40°C < T_A < +85°C) and V_{in} = +5.0 V. Typical values are T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}		1.2		20	V
Undervoltage Lockout Threshold	UVLO	V_{in} falls down UVLO threshold	2.85	3.0	3.15	V
Uvervoltage Lockout Hysteresis	$UVLO_{hyst}$		50	70	90	mV
Overvoltage Lockout Threshold	OVLO	V_{in} rises up OVLO threshold	5.43	5.675	5.9	V
Overvoltage Lockout Hysteresis	$OVLO_{hyst}$		50	100	125	mV
V_{in} versus V_{out} Dopout	V_{drop}	V_{in} = 5 V, I charge = 500 mA		105	200	mV
Supply Quiescent Current	Idd	No Load, V_{in} = 5.25 V		24	35	μA
OVLO Supply Current	Idd_{uvlo}	V_{in} = 7 V		50	85	μA
Output Off State Current	I_{std}	V_{in} = 5.25 V, EN = 1.2 V		26	37	μA
FLAG Output Low Voltage	Vol_{flag}	V_{in} > OVLO, Sink 1 mA on $\overline{FLAG}$ pin			400	mV
FLAG Leakage Current	$FLAG_{leak}$	$\overline{FLAG}$ level = 5 V		5.0		nA
$\overline{EN}$ Voltage High	V_{ih}	V_{in} from 3.3 V to 5.25 V	1.2			V
$\overline{EN}$ Voltage Low	V_{ol}	V_{in} from 3.3 V to 5.25 V			0.4	V
EN Leakage Current	EN_{leak}	EN = 5.5 V or GND		170		nA
TIMINGS						
Start Up Delay	t_{on}	From V_{in} > UVLO to V_{out} = 0.8xV_{in}, See Fig 3		4.0	15	ms
FLAG going up Delay	t_{start}	From V_{in} > UVLO to $\overline{FLAG}$ = 1.2 V, See Fig 3		3.0		μs
Output Turn Off Time	t_{off}	From V_{in} > OVLO to V_{out} ≤ 0.3 V, See Fig 4 V_{in} increasing from 5 V to 8 V at 1 V/μs. No output capacitor.		0.8	1.5	μs
Alert Delay	t_{stop}	From V_{in} > OVLO to $\overline{FLAG}$ ≤ 0.4 V, See Fig 4 V_{in} increasing from 5 V to 8 V at 3 V/μs		1.0	2.0	μs
Disable Time	t_{dis}	From $\overline{EN}$ 0.4 to 1.2V to V_{out} ≤ 0.3 V, See Fig 5 V_{in} = 4.75 V. No output capacitor.		2.0		μs
Thermal Shutdown Temperature	T_{sd}			150		°C
Thermal Shutdown Hysteresis	T_{sdhyst}			30		°C

NOTE: Thermal Shutdown parameter has been fully characterized and guaranteed by design.

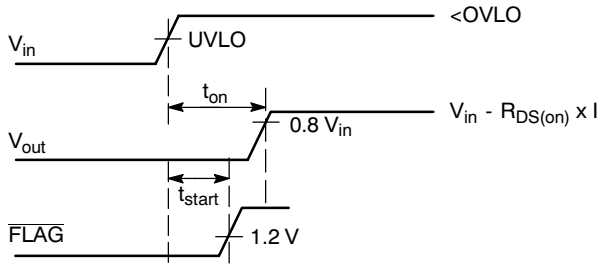


Figure 3. Start Up Sequence

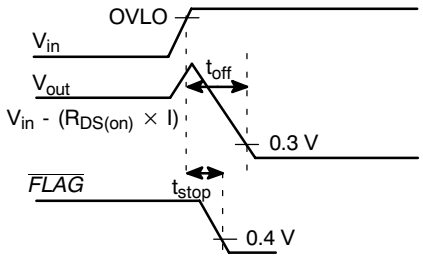


Figure 4. Shutdown on Over Voltage Detection

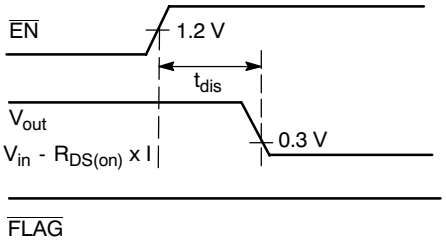


Figure 5. Disable on $\overline{EN}$ = 1

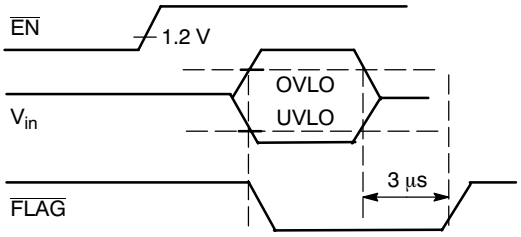


Figure 6. $\overline{FLAG}$ Response with $\overline{EN}$ = 1

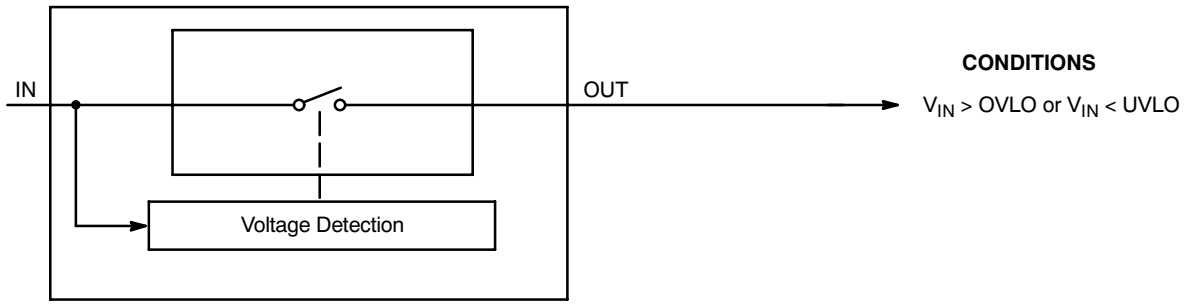


Figure 7.

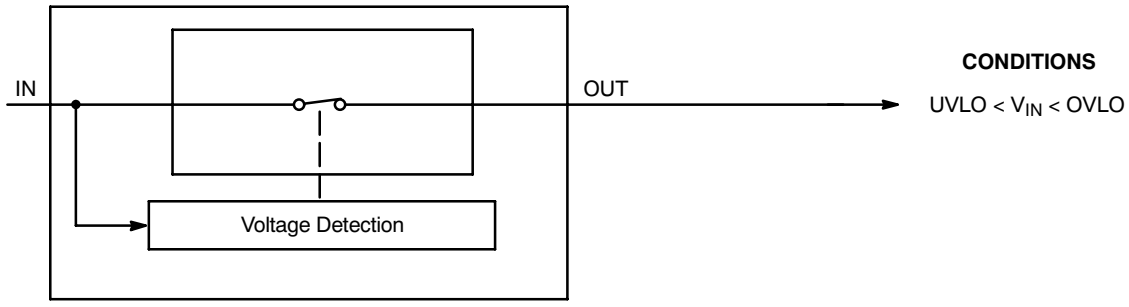


Figure 8.

TYPICAL OPERATING CHARACTERISTICS

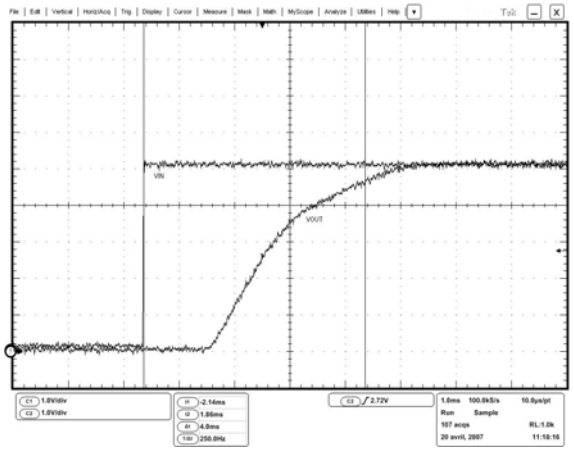


Figure 9. Startup
V_{in} = Ch1, V_{out} = Ch3

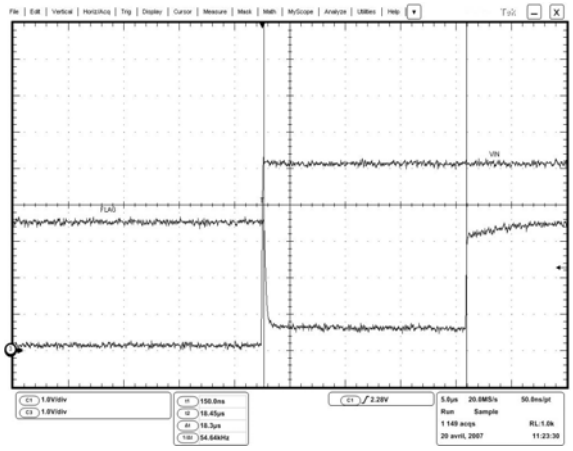


Figure 10. FLAG Going Up Delay
V_{out} = Ch3, FLAG = Ch2

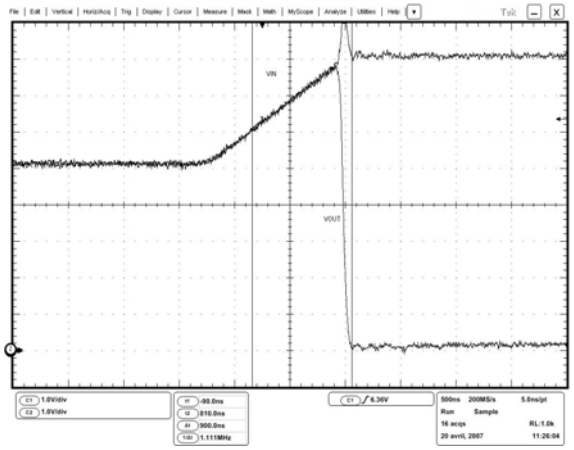


Figure 11. Output Turn Off Time
V_{in} = Ch1, V_{out} = Ch2

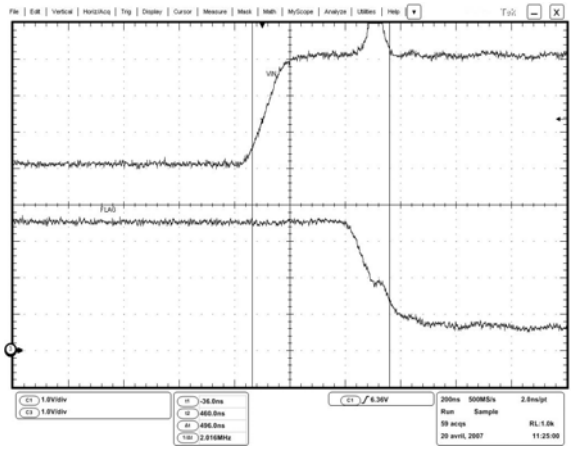


Figure 12. Alert Delay
V_{out} = Ch1, FLAG = Ch3

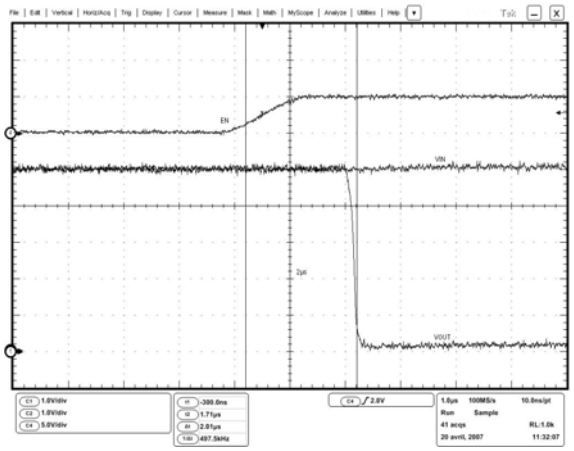


Figure 13. Disable Time
EN = Ch1, V_{out} = Ch2, FLAG = Ch3

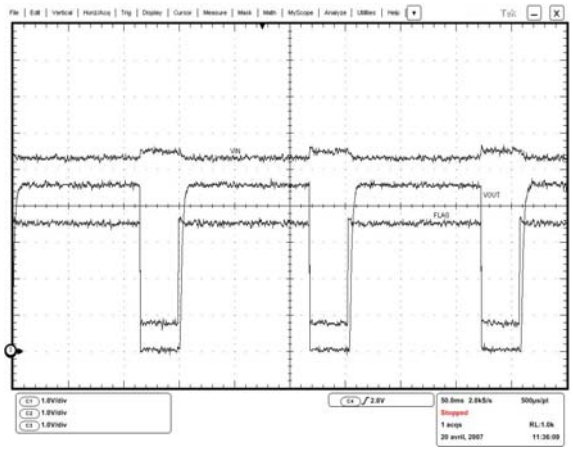


Figure 14. Thermal Shutdown
V_{in} = Ch1, V_{out} = Ch2, FLAG = Ch3

TYPICAL OPERATING CHARACTERISTICS

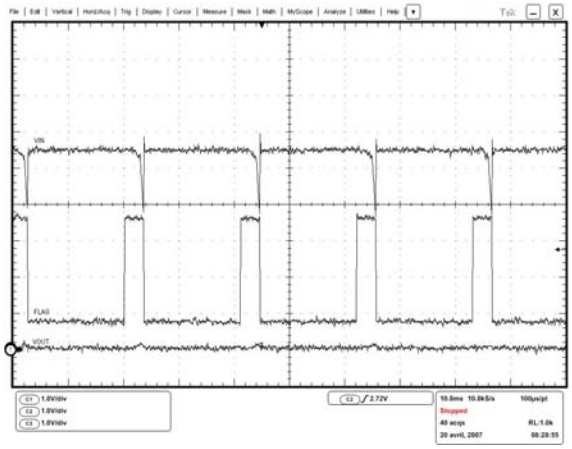


Figure 15. Direct Output Short Circuit

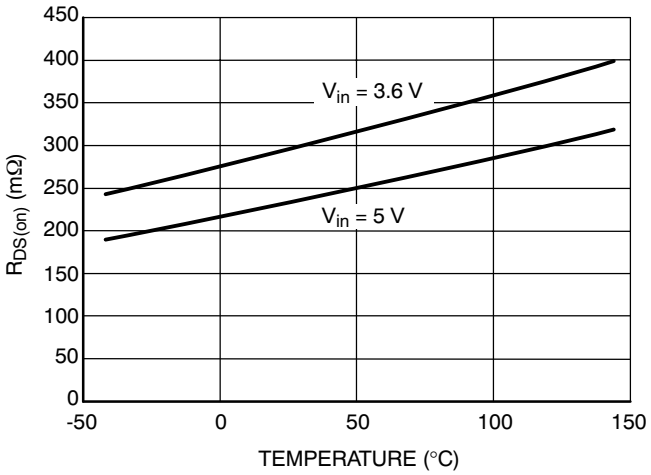


Figure 16. $R_{DS(on)}$ vs. Temperature (Load = 500 mA)

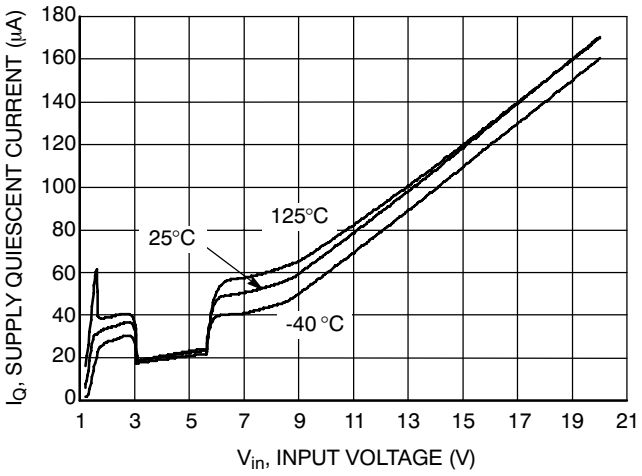


Figure 17. Supply Quiescent Current vs. V_{in}

In Operation

NCP360 provides overvoltage protection for positive voltage, up to 20 V. A PMOS FET protects the systems (i.e.: VBUS) connected on the V_{out} pin, against positive over-voltage. The Output follows the VBUS level until OVLO threshold is overtaken.

Undervoltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built-in undervoltage lock out (UVLO) circuit. During V_{in} positive going slope, the output remains disconnected from input until V_{in} voltage is above 3.2 V nominal. The $\overline{FLAGV}$ output is pulled to low as long as V_{in} does not reach UVLO threshold. This circuit has a 50 mV hysteresis to provide noise immunity to transient condition.

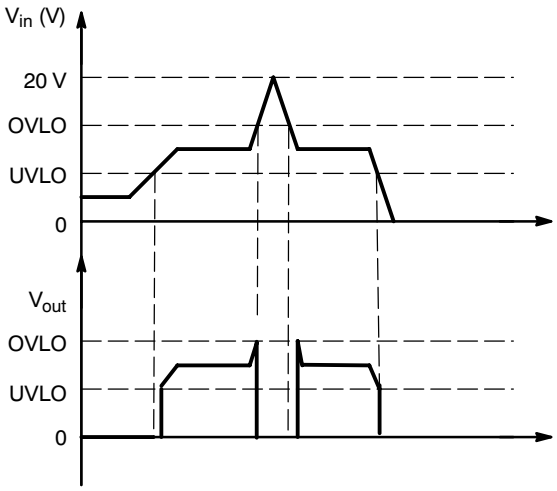


Figure 18. Output Characteristic vs. V_{in}

Overvoltage Lockout (OVLO)

To protect connected systems on V_{out} pin from overvoltage, the device has a built-in overvoltage lock out (OVLO) circuit. During overvoltage condition, the output remains disabled until the input voltage exceeds OVLO - Hysteresis.

$\overline{FLAG}$ output is tied to low until V_{in} is higher than OVLO. This circuit has a 100 mV hysteresis to provide noise immunity to transient conditions.

$\overline{FLAG}$ Output

NCP360 provides a $\overline{FLAG}$ output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon the OVLO threshold is exceeded When V_{in} level recovers normal condition, $\overline{FLAG}$ is held high. The pin is an open drain output, thus a pull up resistor (typically 1 MΩ- Minimum 10 kΩ) must be provided to $V_{battery}$. $\overline{FLAG}$ pin is an open drain output.

$\overline{EN}$ Input

To enable normal operation, the $\overline{EN}$ pin shall be forced to low or connected to ground. A high level on the pin disconnects OUT pin from IN pin. $\overline{EN}$ does not overdrive an OVLO or UVLO fault.

Internal PMOS FET

NCP360 includes an internal PMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the R_{DSon}, during normal operation, will create low losses on V_{out} pin, characterized by V_{in} versus V_{out} dropout. (See Figure 16).

ESD Tests

NCP360 fully support the IEC61000-4-2, level 4 (Input pin, 1 μF mounted on board).

That means, in Air condition, V_{in} has a ±15 kV ESD protected input. In Contact condition, V_{in} has ±8 kV ESD protected input.

Please refer to Fig 19 to see the IEC 61000-4-2 electrostatic discharge waveform.

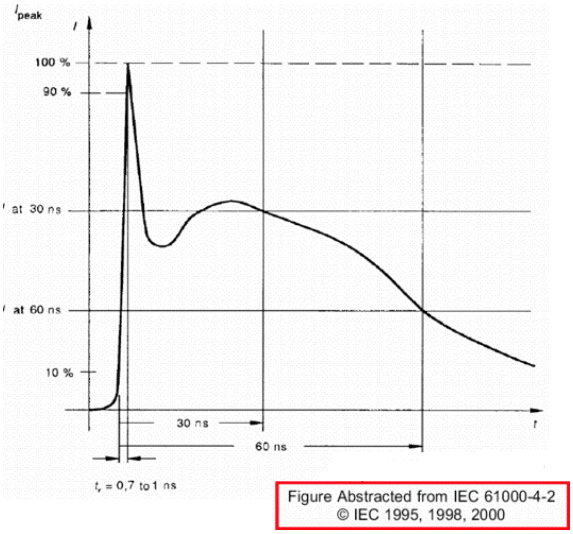


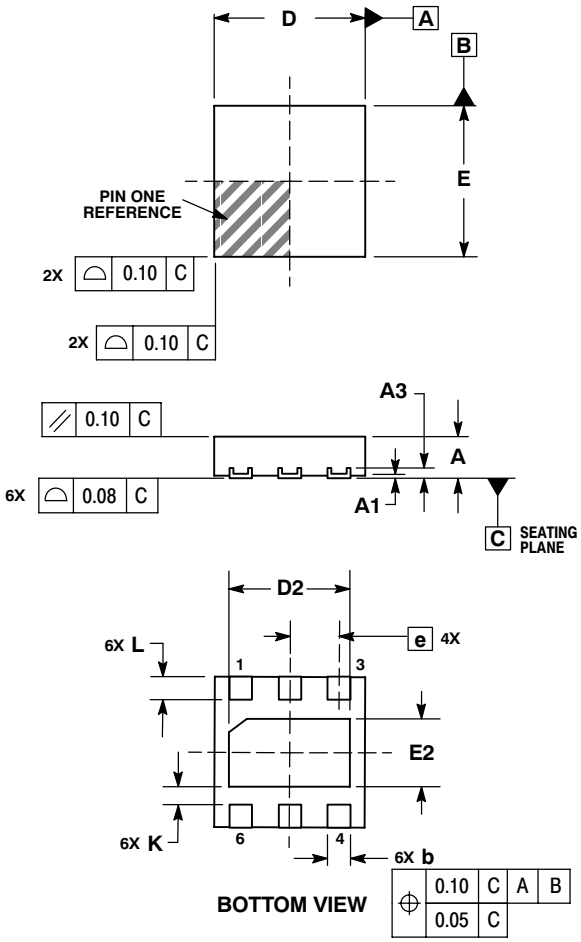
Figure 19.

PCB Recommendations

The NCP360 integrates a 500 mA rated PMOS FET, and the PCB rules must be respected to properly evacuate the heat out of the silicon. The UDFN PAD1 must be connected to ground plane to increase the heat transfer if necessary from an application standpoint. Of course, in any case, this pad shall be not connected to any other potential.

PACKAGE DIMENSIONS

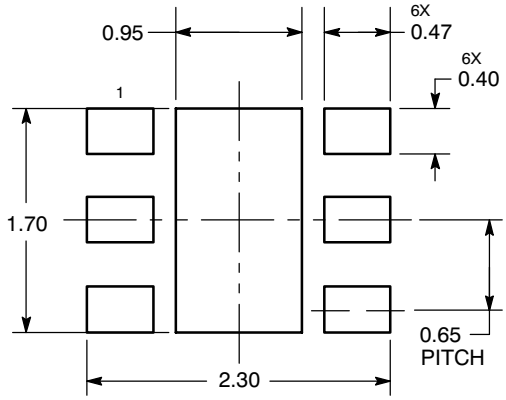
UDFN6 2x2, 0.65P
CASE 517AB-01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
K	0.20	---
L	0.25	0.35

SOLDERING FOOTPRINT*

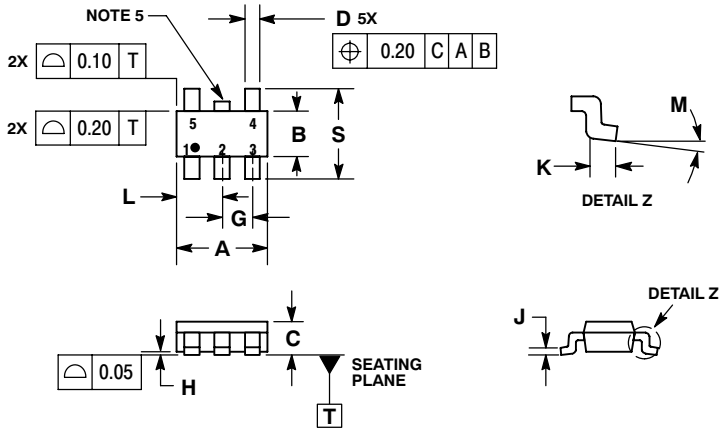


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

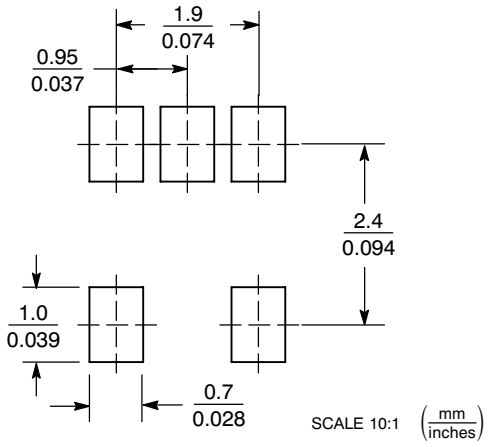
TSOP-5
CASE 483-02
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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