TYPES 3N211, 3N212, 3N213
N-CHANNEL DUAL-GATE DEPLETION-TYPE INSULATED-GATE FIELD-EFFECT TRANSISTORS

BULLETIN NO. DL-S 7312009, MARCH 1973

DEPLETION-TYPE MOS SILICON TRANSISTORS

- Monolithic Gate-Protection Diodes
- Low C_{rss} . . . 0.05 pF Max
- High $|y_{fs}|$ . . . 30,000 μmhos Typ for 3N211 and 3N212

description

The 3N211, 3N212, and 3N213 are N-channel, depletion-type, dual-gate, metal-oxide-semiconductor transistors. They are protected from excessive input voltages by integrated back-to-back diodes between gates and source, thus eliminating precautionary handling procedures required by unprotected MOS transistors.

The 3N211 is intended for use in VHF pre-amplifiers where linear, low-noise amplification is required. Its extremely low feedback capacitance permits high stable gain without the use of neutralization.

The 3N212 is intended for use as a VHF mixer and is well suited for TV tuners. Its use as a mixer minimizes cross-modulation distortion and provides low-noise operation.

The 3N213 is designed for application in tuned high-frequency amplifiers such as TV IF strips. Its extremely low feedback capacitance permits high stage gain and stability without the necessity for neutralization.

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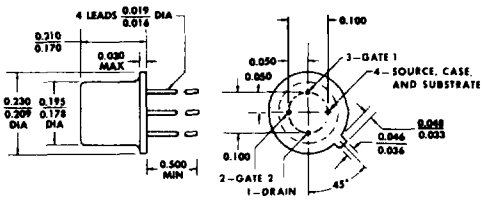
*mechanical data

THE SUBSTRATE AND SOURCE ARE IN ELECTRICAL CONTACT WITH THE CASE



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

ALL JEDEC TO-72 DIMENSIONS AND NOTES ARE APPLICABLE

*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

	3N211 3N212	3N213
Drain–Gate-One Voltage	35 V	40 V
Drain–Gate-Two Voltage	35 V	40 V
Drain-Source Voltage	27 V	35 V
Forward Gate-One-Terminal Current (See Note 1)	←10 mA→	
Forward Gate-Two-Terminal Current (See Note 1)	←10 mA→	
Reverse Gate-One-Terminal Current	←−10 mA→	
Reverse Gate-Two-Terminal Current	←−10 mA→	
Continuous Drain Current	←50 mA→	
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	←360 mW→	
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	←1.2 W→	
Storage Temperature Range	−65°C to 200°C	
Lead Temperature 1/16 Inch from Case for 10 Seconds	←300°C→	

NOTES: 1. Forward gate-terminal current is the current into a gate terminal with a forward gate-source voltage applied. This voltage is of such polarity that an increase in its magnitude causes the channel resistance to decrease.
2. Derate linearly to 175°C free-air temperature at the rate of 2.4 mW/°C.
3. Derate linearly to 175°C case temperature at the rate of 8 mW/°C.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

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*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	3N211		3N212		3N213		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)DS}$	Drain-Source Breakdown Voltage	I_D = 10 μA, V_{G1S} = V_{G2S} = −4 V, t = 5 s	27		27		35		V
$v_{(BR)DS}$	Instantaneous Drain-Source Breakdown Voltage	I_D = 10 μA, V_{G1S} = V_{G2S} = −4 V	25		25		30		V
$V_{(BR)G1SSF}$	Gate-One–Source Forward Breakdown Voltage	I_{G1} = 10 mA, V_{G2S} = V_{DS} = 0, See Note 4	6		6		6		V
$V_{(BR)G1SSR}$	Gate-One–Source Reverse Breakdown Voltage	I_{G1} = −10 mA, V_{G2S} = V_{DS} = 0, See Note 4	−6		−6		−6		V
$V_{(BR)G2SSF}$	Gate-Two–Source Forward Breakdown Voltage	I_{G2} = 10 mA, V_{G1S} = V_{DS} = 0, See Note 4	6		6		6		V
$V_{(BR)G2SSR}$	Gate-Two–Source Reverse Breakdown Voltage	I_{G2} = −10 mA, V_{G1S} = V_{DS} = 0, See Note 4	−6		−6		−6		V
I_{G1SSF}	Gate-One-Terminal Forward Current	V_{G1S} = 5 V, V_{G2S} = V_{DS} = 0		10		10		10	nA
I_{G1SSR}	Gate-One-Terminal Reverse Current	V_{G1S} = −5 V, V_{G2S} = V_{DS} = 0		−10		−10		−10	nA
		V_{G1S} = −5 V, V_{G2S} = V_{DS} = 0, T_A = 150°C		−10		−10		−10	μA
I_{G2SSF}	Gate-Two-Terminal Forward Current	V_{G2S} = 5 V, V_{G1S} = V_{DS} = 0		10		10		10	nA
I_{G2SSR}	Gate-Two-Terminal Reverse Current	V_{G2S} = −5 V, V_{G1S} = V_{DS} = 0		−10		−10		−10	nA
		V_{G2S} = −5 V, V_{G1S} = V_{DS} = 0, T_A = 150°C		−10		−10		−10	μA
I_{DS}	Zero-Gate-One-Voltage Drain Current	V_{DS} = 15 V, V_{G1S} = 0, V_{G2S} = 4 V, See Note 5	6	40	6	40	6	40	mA
$V_{G1S(off)}$	Gate-One–Source Cutoff Voltage	V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 20 μA	−0.5	−5.5	−0.5	−4	−0.5	−5.5	V
$V_{G2S(off)}$	Gate-Two–Source Cutoff Voltage	V_{DS} = 15 V, V_{G1S} = 0, I_D = 20 μA	−0.2	−2.5	−0.2	−4	−0.2	−4	V
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	V_{DS} = 15 V, V_{G1S} = 0, V_{G2S} = 4 V, f = 1 kHz, See Note 6	17	40	17	40	15	35	mmho
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance	V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 1 mA, f = 1 MHz	0.005	0.05	0.005	0.05	0.005	0.05	pF

NOTES: 4. All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage-limiting network is functioning properly.
5. This parameter must be measured using pulse techniques. t_w = 300 μs, duty cycle ⩽ 2%.
6. This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating. The signal is applied to gate 1 with gate 2 at a-c ground.

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*3N211 operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		3N211			UNIT
				MIN	TYP	MAX	
F	Common-Source Spot Noise Figure	V_{DD} = 24 V,	V_{GG} = 6 V,			4	dB
G_{ps}	Small-Signal Common-Source Insertion Power Gain	f = 45 MHz,	See Figure 5	29		37	dB
B	Bandwidth			3.5		6	MHz
$V_{GG(GC)}$	Gain-Control Gate-Supply voltage	V_{DD} = 24 V,	ΔG_{ps} = −30 dB†			+1	V
		f = 45 MHz,	See Figure 5			−1	
F	Common-Source Spot Noise Figure	V_{DD} = 18 V,	V_{GG} = 7 V,			3.5	dB
G_{ps}	Small-Signal Common-Source Insertion Power Gain	f = 200 MHz,	See Figure 6	24		35	dB
B	Bandwidth			5		12	MHz
$V_{GG(GC)}$	Gain-Control Gate-Supply Voltage	V_{DD} = 18 V,	ΔG_{ps} = −30 dB‡,	0		−2	V
		f = 200 MHz,	See Figure 6				
F	Common-Source Spot Noise Figure	V_{DS} = 15 V,	V_{G2S} = 4 V,		5		dB
G_{ps}	Small-Signal Common-Source Insertion Power Gain	I_D = 15 mA,	f = 450 MHz,		21		dB
		See Figures 7 and 9					

†ΔG_{ps} at 45 MHz is defined as the change in G_{ps} from the value at V_{GG} = 6 volts.

‡ΔG_{ps} at 200 MHz is defined as the change in G_{ps} from the value at V_{GG} = 7 volts.

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*3N212 operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDTIONS		3N212		UNIT
				MIN	MAX	
$G_{ps(conv)}$	Small-Signal Conversion Power Gain	V_{DD} = 18 V,	f_{LO} = 245 MHz§,	21	28	dB
B	Bandwidth	f_{RF} = 200 MHz,	See Figure 8	4	7	MHz

§Amplitude at input from local oscillator is adjusted for maximum $G_{ps(conv)}$.

*3N213 operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		3N213		UNIT
				MIN	MAX	
F	Common-Source Spot Noise Figure	V_{DD} = 24 V,	V_{GG} = 6 V,		4	dB
G_{ps}	Small-Signal Common-Source Insertion Power Gain	f = 45 MHz,	See Figure 5	27	35	dB
B	Bandwidth			3.5	6	MHz
$V_{GG(GC)}$	Gain-Control Gate-Supply Voltage	V_{DD} = 24 V,	ΔG_{ps} = −30 dB†,		+1	V
		f = 45 MHz,	See Figure 5		−1	

†ΔG_{ps} at 45 MHz is defined as the change in G_{ps} from the value at V_{GG} = 6 volts.

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TYPICAL CHARACTERISTICS AT T_A = 25°C

3N211
SMALL-SIGNAL COMMON-SOURCE
INSERTION POWER GAIN
vs
GAIN-CONTROL GATE-SUPPLY VOLTAGE

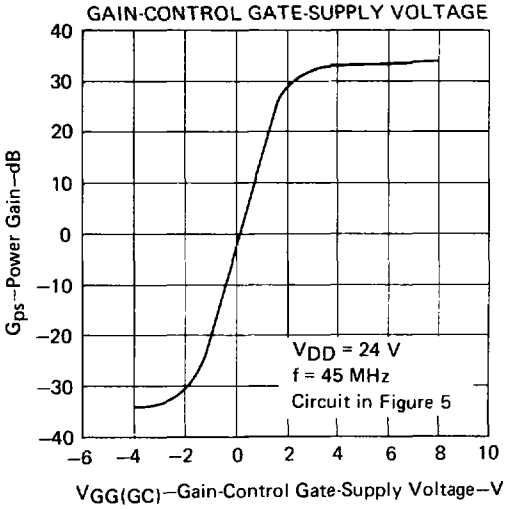

FIGURE 1

3N211
RELATIVE SMALL-SIGNAL POWER GAIN
vs
GAIN-CONTROL GATE-SUPPLY VOLTAGE

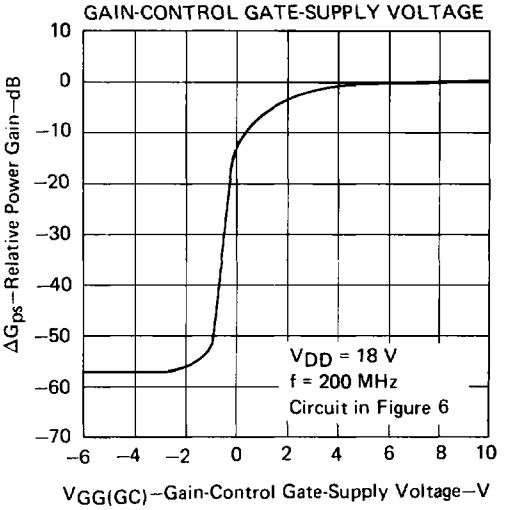

FIGURE 2

3N211
COMMON-SOURCE SPOT NOISE FIGURE
vs
GAIN-CONTROL GATE-SUPPLY VOLTAGE

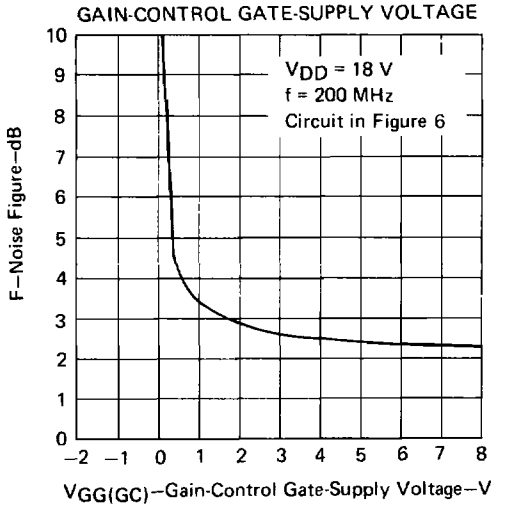

FIGURE 3

3N211
OPTIMUM SPOT NOISE FIGURE
vs
FREQUENCY

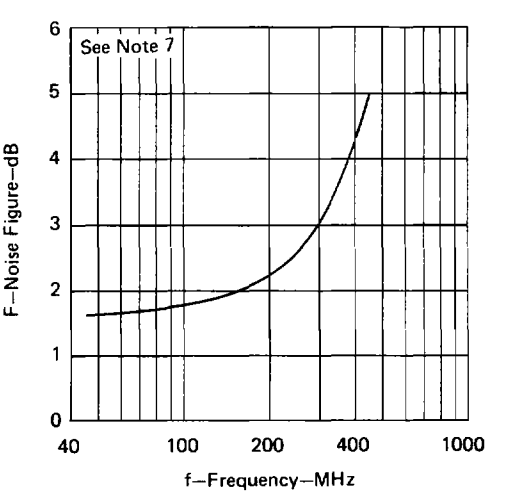

FIGURE 4

NOTE 7: Test conditions at 45 MHz, 200 MHz, and 450 MHz are the conditions given in the table of operating characteristics for 3N211.

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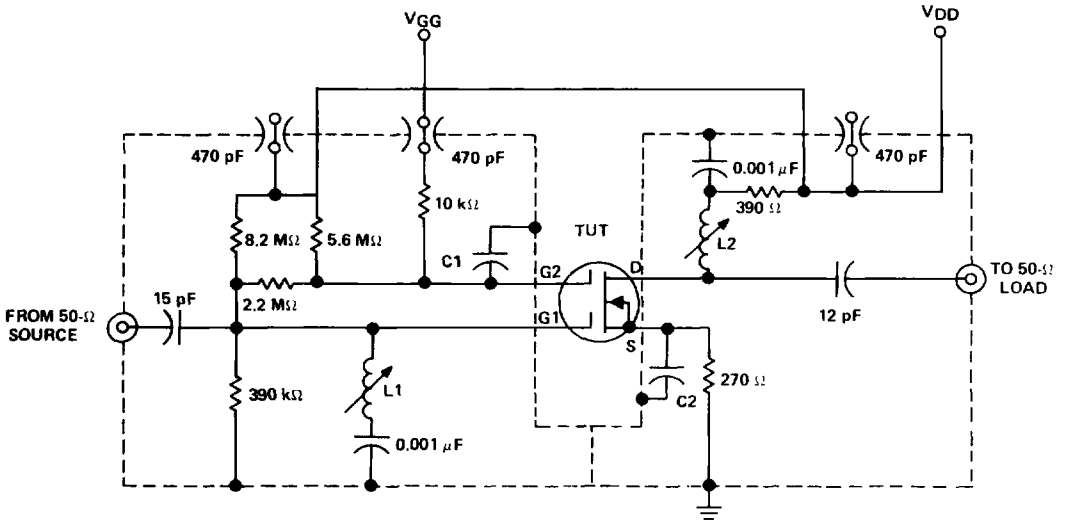
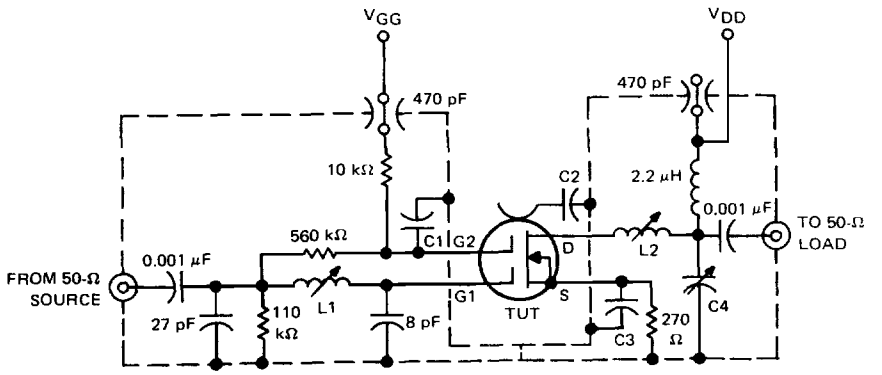
PARAMETER MEASUREMENT INFORMATION



CIRCUIT COMPONENT INFORMATION

C1: Leadless disc ceramic, 0.001 μF
C2 Leadless disc ceramic, 0 01 μF
L1 8T # 28, 5/32-inch-dia form, type "J" slug
L2. 9T # 28, 5/32-inch-dia form, type "J" slug

FIGURE 5—45-MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT FOR 3N211 AND 3N213*



CIRCUIT COMPONENT INFORMATION

C1, C2, & C3: Leadless disc ceramic, 0.001 μF
C4: ARCO 462, 5-80 pF, or equivalent
L1: 3T #18, 3/16-inch-dia aluminum slug
L2: 8T #20, 3/16-inch-dia aluminum slug

FIGURE 6—200-MHz POWER GAIN, GAIN-CONTROL VOLTAGE, AND NOISE FIGURE TEST CIRCUIT FOR 3N211*

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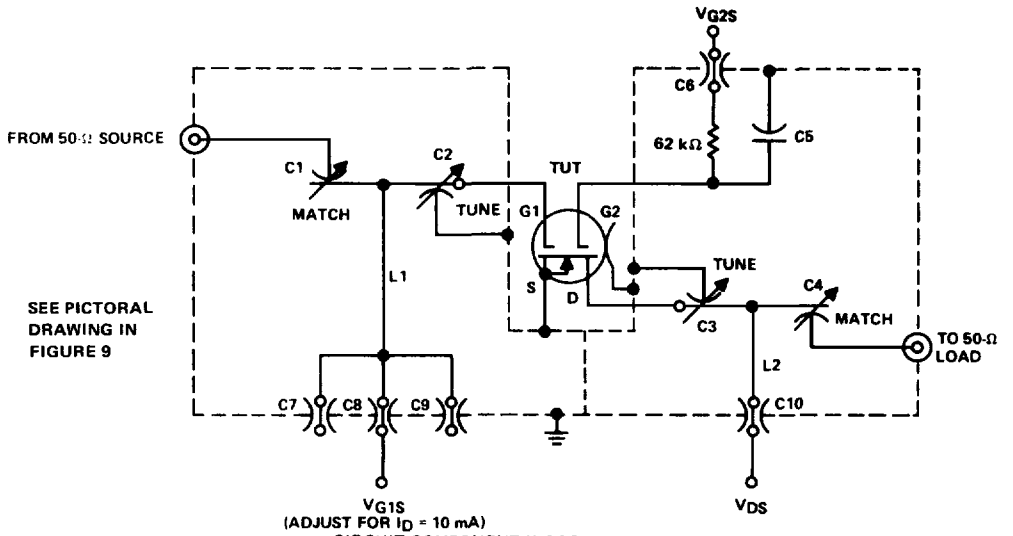
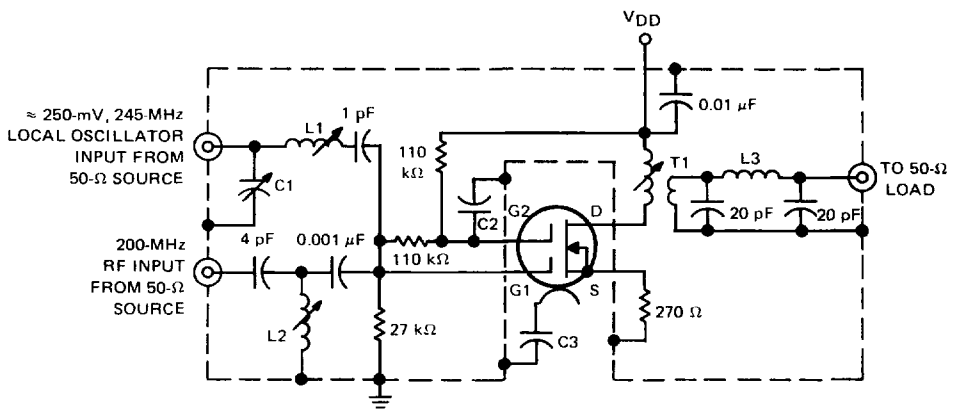
PARAMETER MEASUREMENT INFORMATION



CIRCUIT COMPONENT INFORMATION

C1 thru C4: See Figure 9, Note D
C5: 0.001 μF leadless disc capacitor
C6 thru C10: Allen-Bradley FSAU 0.001 μF feed-through capacitors
L1 & L2: See Figure 9

FIGURE 7—450-MHz POWER GAIN AND NOISE TEST CIRCUIT FOR 3N211



L1: 7T #34, 1/4-inch dia., aluminum slug
L2: 3T #20, 1/4-inch dia., aluminum slug
L3: 7T #24, 1/4-inch dia., air core

C1: Arco type 462, 5-80 pF
C2: 0.001 μF leadless disc
C3: 0.01 μF leadless disc

T1: Pri: 25T #30, close wound on 1/4-inch-dia form, type "J" slug
Sec: 4T #30, centered over primary

FIGURE 8—200-MHz-to-45-MHz CIRCUIT FOR CONVERSION POWER GAIN FOR 3N212*

*JEDEC registered data

NOTES:
A. All dimensions are in inches.
B. The removable top of test fixture is not shown.
C. For clarity, the 62 kΩ resistor, the source and gate-2 socket pins, and insulating stand-off terminals (ISOT) soldered into the fold of L1 and L2 respectively for mechanical support, are not shown in view A.
D. C1 and C2 (C3 and C4) consist of shim brass and the "C" portion of L1 (L2) separated by air and the mylar tape covering the "C" portion of L1 (L2).

NOTE:
E. The four views surrounding the center view are as they would appear before the metal is bent up to form the sides.

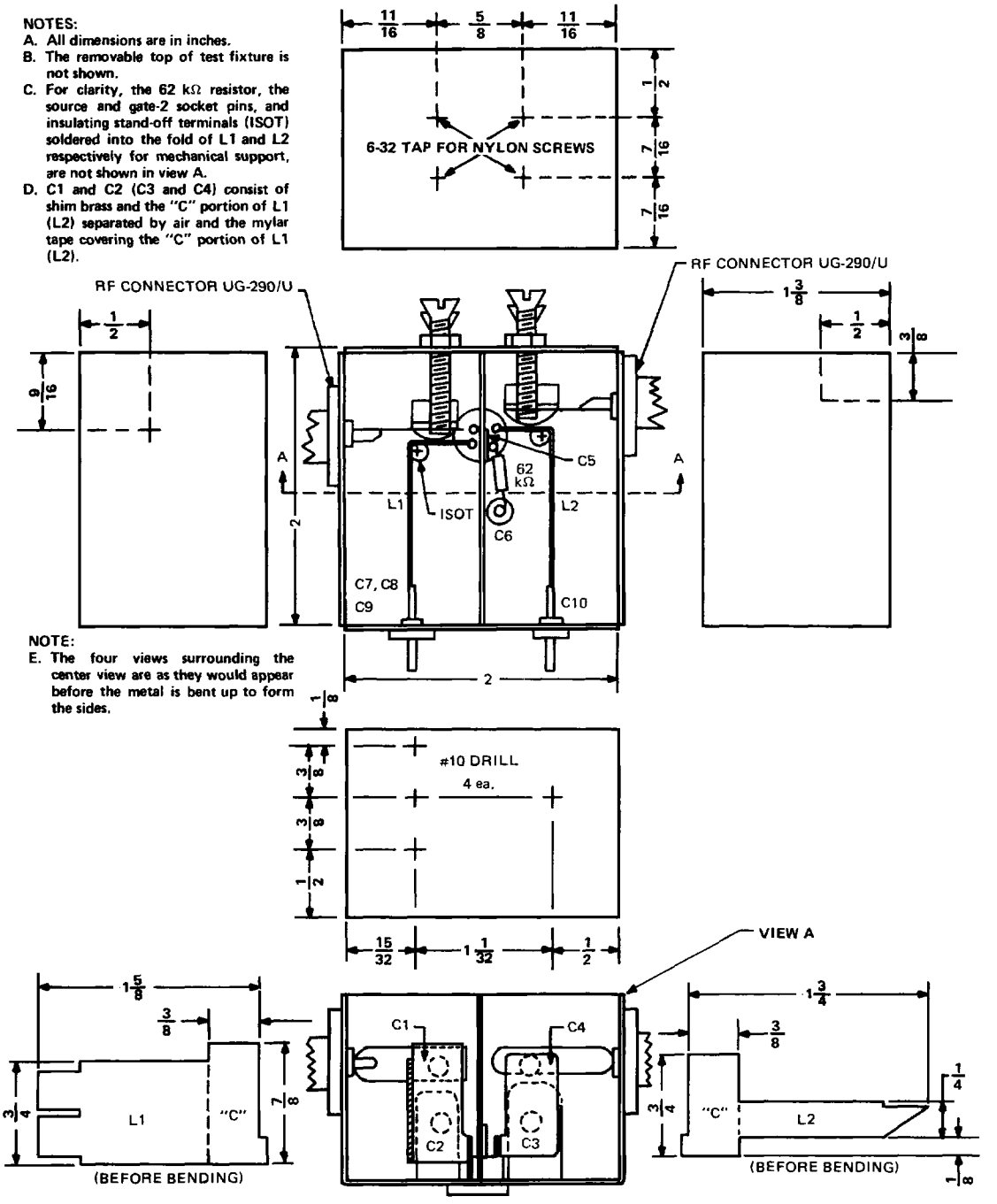


FIGURE 9—450-MHz POWER GAIN AND NOISE TEST FIXTURE

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