HADC77200

8-BIT, 150 MSPS FLASH A/D CONVERTER

FEATURES

- **150 MSPS CONVERSION RATE**
- 1/2 LSB Linearity
- Preamplifier Comparator Design
- Typical Power Dissipation < 2.2 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Medical Electronics: Ultrasound, CAT Instrumentation

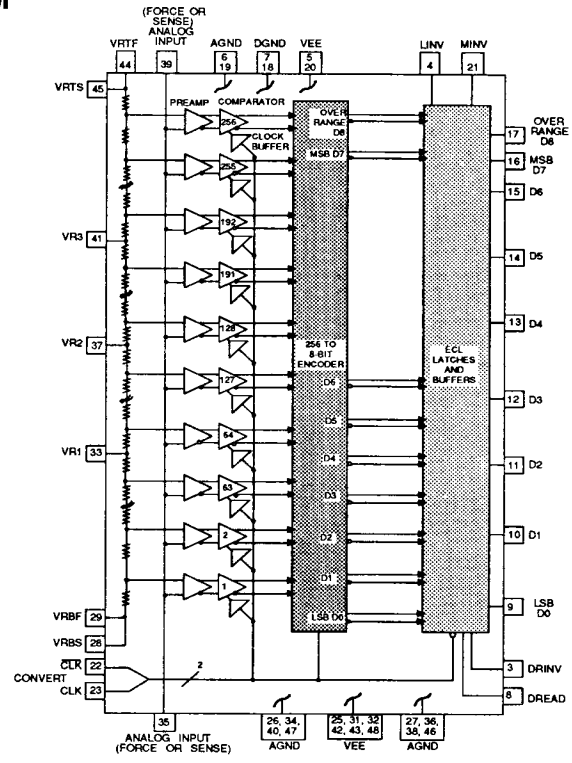
GENERAL DESCRIPTION

The HADC77200 is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components into 8-bit digital words at a 150 MSPS update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth. A single standard -5.2 Volt power supply is required for operation of the HADC77200, with nominal power dissipation of 2.2 Watts.

The part is packaged in a 48 or 42 Lead Ceramic Side-brazed DIP. The 42 Lead DIP is pin compatible with the CX20116. The HADC77200 in the 48 or 46 lead packages includes five external reference ladder TAPS to gain better control over linearity; an overrange bit for use in higher resolution systems; and a data ready output pin for ease in interfacing to high-speed memory. Careful attention to design and layout has provided a device with low noise floor, stable input characteristics, and low data error rate. The HADC77200 is available in Industrial and Military Temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages Output
Negative Supply Voltage (V_{EE} TO GND) ..-7.0 to +0.5 V
Ground Voltage Differential.....-0.5 to +0.5V

Input Voltage
Analog Input Voltage.....+0.5 to V_{EE} V
Reference Input Voltage.....+0.5 to V_{EE} V
Digital Input Voltage.....+0.5 to V_{EE} V
Reference Current VRT to VRB.....25 mA
Tap Reference Current.....-6 to +6 mA

Output
Digital Output Current.....0 to -25 mA

Temperature
Operating Temperature, ambient.....-65 to +150°C
junction.....+150°C
Lead Temperature, (soldering 10 seconds).....+300°C
Storage Temperature.....-65 to +150°C

Notes:
1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
TRANSFER CHARACTERISTICS										
Integral Linearity , 77200A		II			±1/2		±1/2		±1/2	LSB
Differential Linearity , 77200A		II			±1/2		±1/2		±1/2	LSB
Integral Linearity, 77200B		II			±3/4		±3/4		±3/4	LSB
Differential Linearity, 77200B (No missing codes)		II			±3/4		±3/4		±3/4	LSB
Offset Error VRT		II	-30		30	-30	30	-30	30	mV
Offset Error VRB		II	-30		30	-30	30	-30	30	mV
ANALOG INPUT CHARACTERISTICS										
Input Voltage Range		II	-2.0		0.0	-2.0	0.0	-2.0	0.0	VOLTS
Input Capacitance	Over full input range	V		45						pF
Input Resistance		V		4						kΩ
Input Current		II		300	500		450		650	µA
Clock Synchronous Input Currents		V		40						µA

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
POWER SUPPLIES										
Supply Current		II		420	505		525		505	mA
Power Dissipation		II		2.18	2.63		2.73		2.63	watts
REFERENCE										
Ladder Resistance		II	100		300	100	300	80	300	Ω
Reference Bandwidth		V		50						MHz
DIGITAL LOGIC										
Output High Voltage	50Ω to -2V	II	-0.98	-0.90	-0.82	-0.89	-0.70	-1.08	-0.91	VOLTS
Output Low Voltage	50Ω to -2V	II	-1.95	-1.80	-1.65	-1.95	-1.65	-1.95	-1.69	VOLTS
Input High Voltage (MINV, LINV)		II	-1.13		-0.81	-1.07	-0.67	-1.27	-0.87	VOLTS
Input Low Voltage (MINV, LINV)		II	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	VOLTS

V_{EE} = -5.2V, R_{Source} = 10Ω, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
CONVERSION TIMING, See Figure 1A										
Maximum Sample Rate		IV	125	150		125		125		MSPS
Clock Low Width, TPW0		I	5	3		4		4		ns
Clock High Width, TPW1		I	5	3		4		4		
Output Delay, TD	Differential Clock	I	3	4.2	5					ns
Output Delay Tempco	Differential Clock	V		15						ps/°C
Data Ready Delay	Differential Clock	I	3	4	5					ns
Output Rise Time 20% to 80%	50Ω to -2V	I	1.3	1.9	2.4					ns
Output Fall Time 20% to 80%	50Ω to -2V	I	1.1	1.5	2.2					ns

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 100MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
ANALOG INPUTS										
Large Signal Bandwidth	Vin = F.S.	V		100						MHz
Small Signal Bandwidth	Vin = 500mV PP	V		175						MHz
Aperture Jitter		V		12						ps RMS
Aperture Delay	Differential Clock	I	0.3	1.8	2.3					ns
Aperture Delay Tempco	Differential Clock	V		4						ps/°C
Aperture Time		V		<100						ps
Acquisition Time	F.S. to ±1/2 LSB	V		5						ns
Input Slew Rate		V		800						V/µs

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 100MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
SIGNAL QUALITY f_{clock} = 100MHz										
Total Dynamic Error	Vin = FS @ 1MHz	I	45	48						dB
Total Dynamic Error	Vin = FS @ 25MHz	I	36.7	38						dB
Total Dynamic Error	Vin = FS @ 50MHz	I	31	33						dB
Signal to noise ratio	Vin = FS @ 1MHz	I	46.5	49						dB
Signal to noise ratio	Vin = FS @ 25MHz	I	42.5	46						dB
Signal to noise ratio	Vin = FS @ 50MHz	I	34	38						dB
Total Harmonic Distortion	Vin = FS @ 1MHz	I	52	56						dBc
Total Harmonic Distortion	Vin = FS @ 25MHz	I	38	39						dBc
Total Harmonic Distortion	Vin = FS @ 50MHz	I	32	34						dBc
Differential Gain	NTSC 40IRE mod. ramp,Fc = 125MSPS	V		1.0						%
Differential Phase		V		.5						DEG

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 100MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
TRANSFER CHARACTERISTICS										
Integral Linearity, 77200A		I			±1/4 ±1/2		±1/2		±1/2	LSB
Differential Linearity, 77200A		I			±1/4 ±1/2		±1/2		±1/2	LSB
Offset Error VRT		I	-30		30	-30	30	-30	30	mV
Offset Error VRB		I	-30		30	-30	30	-30	30	mV
ANALOG INPUT CHARACTERISTICS										
Input Voltage Range	VRT = 0.5V VRB = -2.5V	I	-2.5		+0.5	-2.5	+0.5	-2.5	+0.5	VOLTS
Input Capacitance	Over full input range	IV		45						pF
Input Resistance		V		4						kΩ
Input Current		I		300	500		400		750	µA
Clock Synchronous Input Currents		V		40						µA
POWER SUPPLIES										
Supply Current		I		420	505		535		505	mA
REFERENCE										
Ladder Resistance		I	100		300	130	300	60	300	Ω
Reference Bandwidth		V		50						MHz

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 100MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
DIGITAL LOGIC										
Output High Voltage	50Ω to -2V	I	-0.98	-0.90	-0.82	-0.85	-0.66	-1.10	-0.95	VOLTS
Output Low Voltage	50Ω to -2V	I	-1.95	1.80	-1.65	-1.95	-1.65	-2.0	-1.70	VOLTS
Input High Voltage (MINV, LINV)		I	-1.13		-0.81	-1.07	-0.67	-1.27	-0.87	VOLTS
Input Low Voltage (MINV, LINV)		I	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	VOLTS

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
CONVERSION TIMING (See Figure1A)										
Maximum Sample Rate		I	100	150		100		100		MSPS
Clock Low Width, TPW0		I	5	3		5		5		ns
Clock High Width, TPW1		I	5	3		5		5		ns
Data Ready Delay, TD		I	3	4	5	3.8	7	3.5	4.5	ns
Output Delay, TD	Differential Clock	I	3	3.4	5	4	7	3	4.5	ns
Output Rise Time (20% to 80%)	50Ω to -2V	I	1.3	1.9	2.4	1.3	4	0.5	2.2	ns
Output Fall Time (20% to 80%)	50Ω to -2V	I	1.1	1.5	2.2	1.1	4	0.5	2.2	ns
ANALOG INPUTS										
Aperture Jitter		V		12						ps RMS
Aperture Delay	Differential Clock	I	0.3	1.2	2.3	0.3	2.8	0.3	2.0	ns
Aperture Time		V		<100						ps
Settle-to-Hold Time		V		5						ns
Aperture Delay Tempco	Differential Clock	V		4						ps/°C

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 100MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
SIGNAL QUALITY f_{clock} = 100MHz										
Total Dynamic Error	Vin = FS @ 1MHz	I		45	48	44.2		44.2		dB
Total Dynamic Error	Vin = FS @ 25MHz	I		36.7	38	36.2		36.2		dB
Total Dynamic Error	Vin = FS @ 50MHz	I		31	33	29.2		29.2		dB
Signal to noise ratio	Vin = FS @ 1MHz	I		46.5	49	45		45		dB
Signal to noise ratio	Vin = FS @ 25MHz	I		42.5	46	41		41		dB
Signal to noise ratio	Vin = FS @ 50MHz	I		34	38	32.5		32.5		dB
Total Harmonic Distortion	Vin = FS @ 1MHz	I		52	56	50.5		52		dBc
Total Harmonic Distortion	Vin = FS @ 25MHz	I		38	39	36.5		38		dBc
Total Harmonic Distortion	Vin = FS @ 50MHz	I		32	34	30.5		32		dBc

TEST LEVEL CODES

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperatures.
II	100% production tested at Ta = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

GENERAL DESCRIPTION

The HADC77200 is the fastest monolithic 8-bit parallel flash A/D converter available today. The minimum conversion rate is 150 MSPS and the analog bandwidth is in excess of 70 MHZ. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This reduces clock transient kickback to the input and reference ladder. The preamplfiers also add a gain of six to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces meta- stable states that can cause errors at the output.

An additional advantage of the HADC77200 over similar devices is a better integral linearity specification over the part's entire usable range.
The specification is improved from 1/2 LSB to 1/4 LSB. The center reference ladder tap is optional as needed to futher decrease this specification.

The HADC77200 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. Furthermore, the HADC77200 has an on-board power supply bypass of 1500pF to reduce external component needs, and the output drive capability of the device can provide full ECL swings into 50Ω loads.

TYPICAL INTERFACE CIRCUIT

The HADC77200 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows:

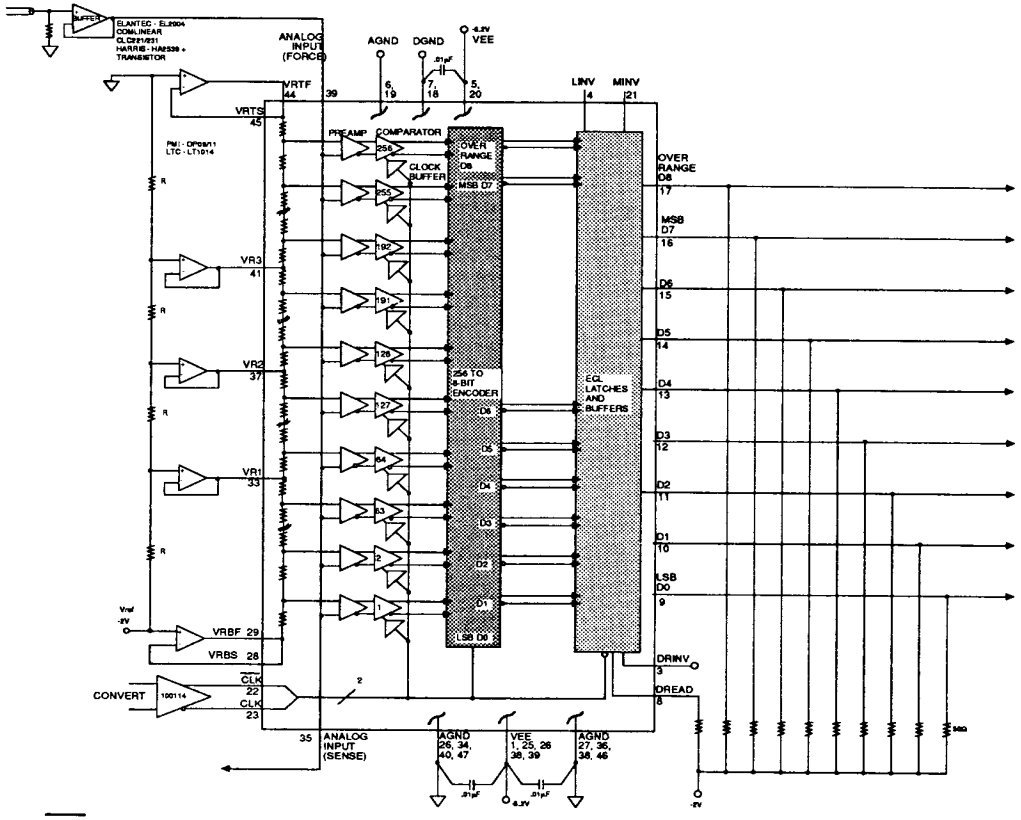
VEE, AGND, DGND

VEE is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01µF ceramic capacitor. A 1µF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in Figure 1.

VIN (Analog Input)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force". This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The HADC77200 is superior to similar devices due to a preamplifier stage before the comparators. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836 transistor. Very high performance can be achieved by using a Comlinear CLC221/231.

FIGURE 1 HADC77200 TYPICAL INTERFACE CIRCUIT



CLK, $\overline{CLK}$ (Clock Inputs)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{CLK}$ is internally biased to -1.3V (see clock input circuit on page 12). It may be left open but a .01µF bypass capacitor from $\overline{CLK}$ to AGND is recommended. The duty cycle of the clock is not important as long as minimum pulse width is maintained.

MINV, LINV (Output Logic Control)

These are digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table 1. Both MINV and LINV are in the logic "low" (0) state when they are left open. The "high" state can be obtained by tying to AGND through a diode or 3.9kΩ resistor.

D0 to D7 (Digital Outputs)

The digital outputs can drive 50Ω to ECL levels when pulled down to -2V. When pulled down to -5.2V the outputs can drive 130Ω to 1KΩ loads.

VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS (Reference Inputs)

These are five external reference voltage taps from -2V (VRB) to AGND (VRT) which can be used to control integral linearity over temperature. The TAPS can be driven by Op amps as shown in Figure 1. These voltage level inputs can be bypassed to AGND for futher noise suppression if so desired. VRB and VRT have "force" and "sense" pins for monitoring the top and bottom voltage references.

DREAD (Data Ready), DRINV (Data Ready Inverse)

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the HADC77200's decoders and latches. This function is useful for interfacing with high speed memory. Using the data ready output to latch the output data ensures minimum setup and hold times. DRINV is a data ready inverse control pin. Timing is shown in Figure 1A.

D8 (Overrange)

This is an overrange function. When the HADC77200 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the HADC77200 into higher resolution systems.

N/C

All "Not Connected" pins should be tied to AGND.

TABLE 1 - OUTPUT CODING

	MINV LINV	0 0	0 1	1 0	1 1
	0V	111...11	100...00	011...11	000...00
	.	111...10	100...01	011...10	000...01
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
V_{IN}	.	100...00	111...11	000...00	011...11
	.	011...11	000...00	111...11	100...00
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
	.	000...01	011...10	100...01	111...10
	-2V	000...00	011...11	100...00	111...11

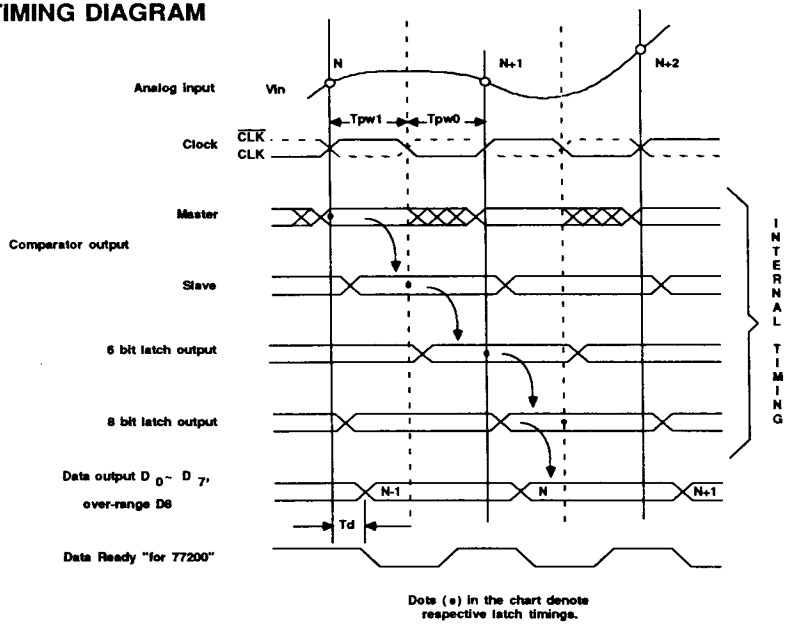
1: V_{IH}, V_{OH}

0: V_{IL}, V_{OL}

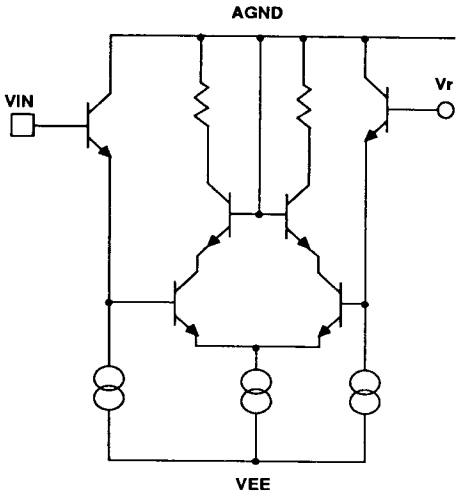
OPERATION

The HADC77200 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram on page 1. This voltage is applied to the positive input of each preamplifier and comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT(0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from four columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions and they consist of a set of eight XOR gates. Finally, eight ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

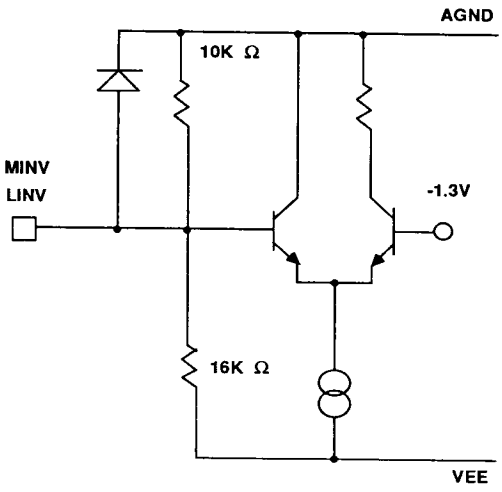
FIGURE 1A - TIMING DIAGRAM



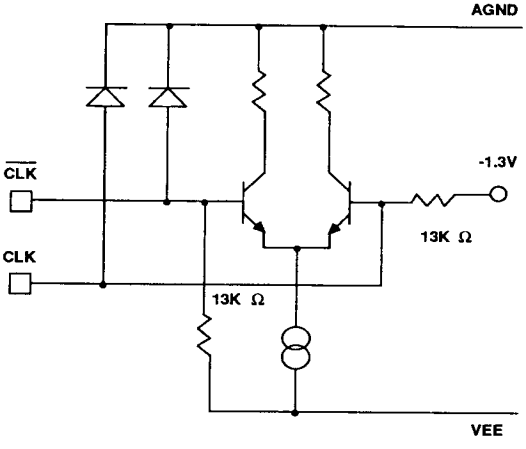
INPUT CIRCUIT



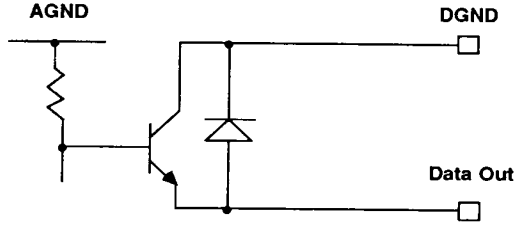
DRINV, MINV, LINV INPUT CIRCUIT



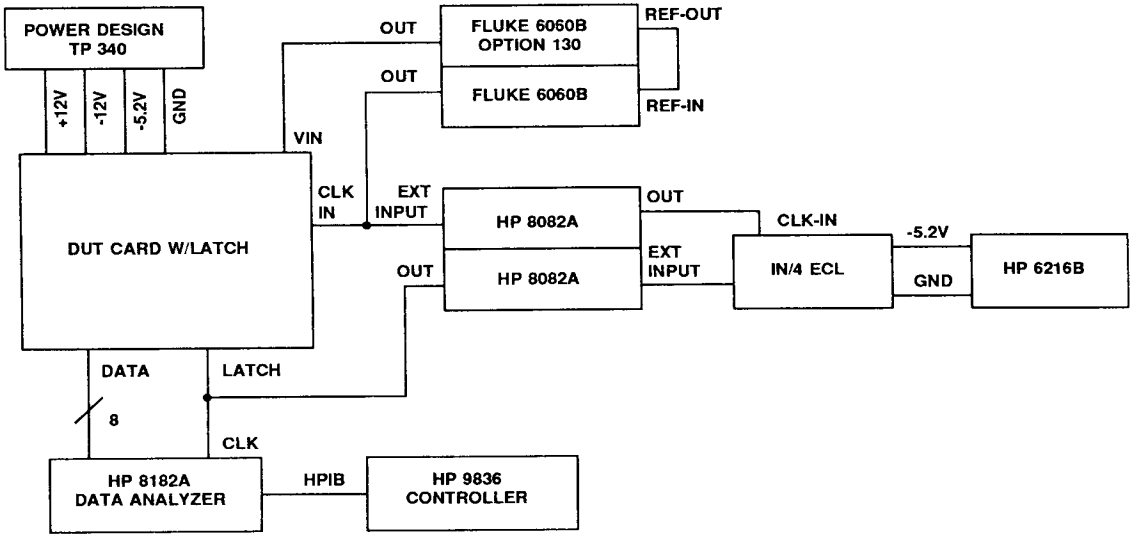
CLOCK INPUT



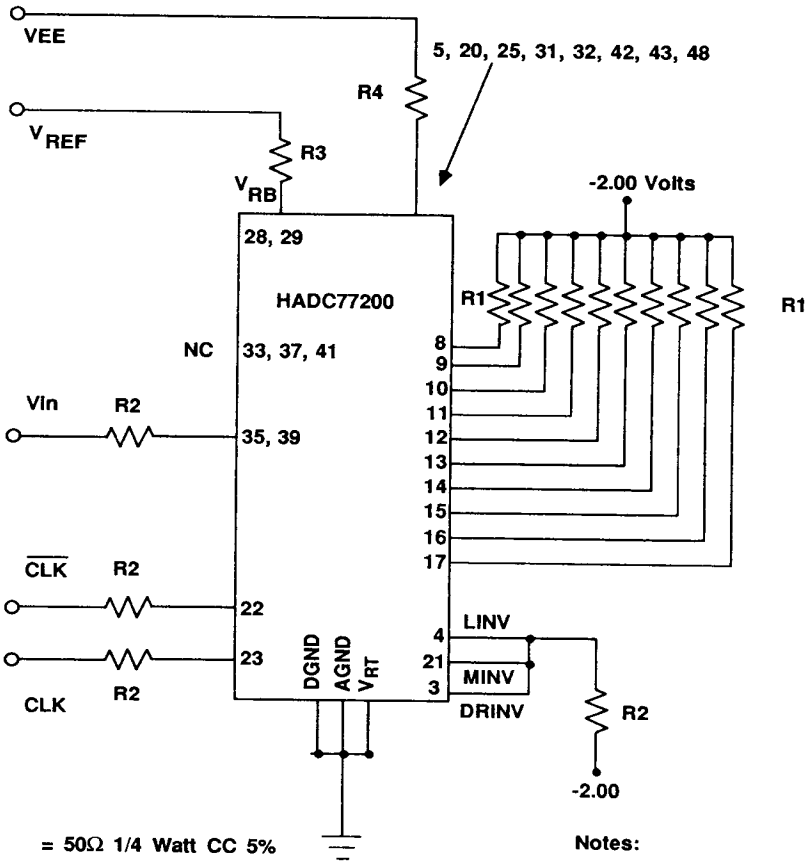
OUTPUT CIRCUIT D0 THROUGH D8, DREAD



DYNAMIC EVALUATION



BURN-IN CIRCUIT T_{CASE} = 125°C



R1 = 50Ω 1/4 Watt CC 5%

R2 = 1KΩ 1/4 Watt CC 5%

R3 = 6.5Ω 1/4 Watt CC 5%

R4 = 3.25Ω 1/2 Watt CC 5%

V_{REF} = -2.00 Volts

V_{EE} = -6.6 Volts

Notes:

1. Pin numbers refer to dip packages

DEFINITION OF TERMS

SPECIFICATIONS

A/D CONVERTER ERROR SUMMARY

Honeywell SPT realizes that the transfer function for an A/D converter is very dependent upon the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 2B) while a static dc input level may appear close to the ideal (Figure 2A). That is why we are including many dynamic tests as well as the the industry standard dc specifications.

EFFECTIVE BITS (SNR)

This is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from measured rms error for the ideal sinewave and the measured actual rms error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual rms error}}{\text{ideal rms error}}$$

Furthermore, signal-to-noise ratio (SNR) can be related to effective bits by the following formula:

$$\text{SNR(dB)} = 1.8 + 6.02 \times \text{N(eff bits)}$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D tranfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q = $FSR/2^N$ where FSR = full scale range and N = 8. Non-ideal quantization bands represent differential nonlinearity errors (See Figures 2A and 2B).

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 2B shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC77200's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 2B points out two missed codes in the transfer function.

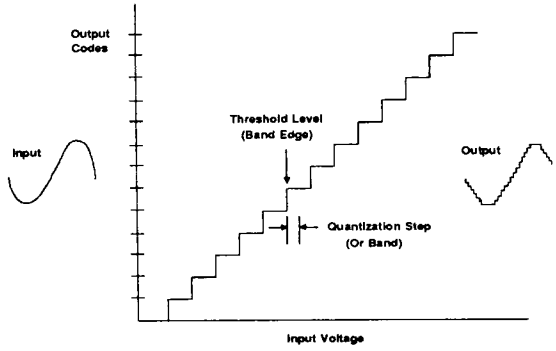


Figure 2A Static Input Conditions

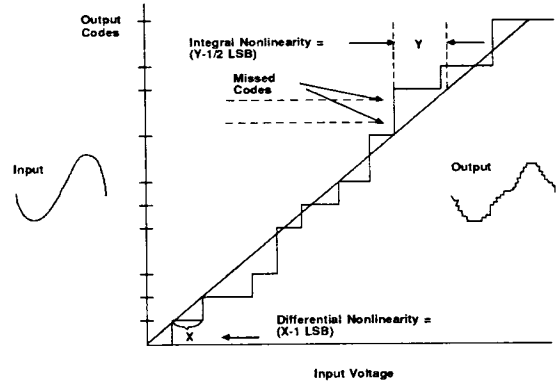


Figure 2B Dynamic Conditions

SPECIFICATIONS CONTINUED

INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 3A). Integral nonlinearity does not include any gain and offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 2B shows an integral nonlinearity error of 2 LSB. The HADC77200's integral nonlinearity can be improved by using the external reference ladder taps as shown in Figure 1. The resulting effect on the linearity is shown in Figure 3B.

APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point. See Figure 3C .

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sinewave can be calculated for time or voltage by the equation:

$$dV/V = 2\pi f t_a$$

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track and hold can be determined. The graph in Figure 4 summarizes required aperture time for 8-bit resolution high speed converters using sinusoidal frequencies.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10MHz, then from Figure 4 it can be determined that to assure less than 8-bits of error due to aperture alone, the A/D converter must have an aperture time of less than 70ps. Most data sheets do not state aperture time so usually a sample and hold is used. Unfortunately, the sample and holds generally available today are not faster than 70ps.

Aperture time and delay are very difficult to measure, however these values are needed to make intelligent design decisions. Honeywell SPT supplies these values for the HADC77200 based on both computer design simulations and verified by characterization of samples.

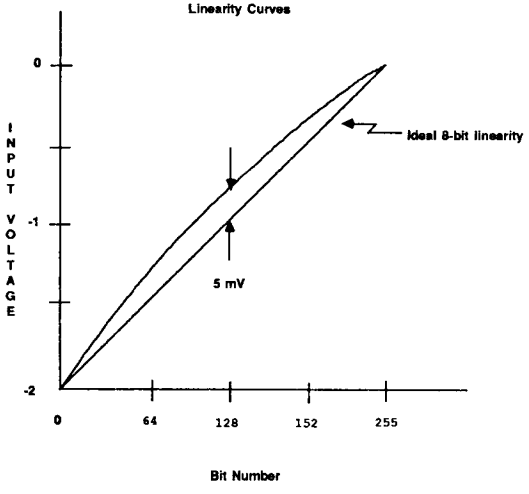


FIGURE 3A Linearity Curve with no TAP adjustment

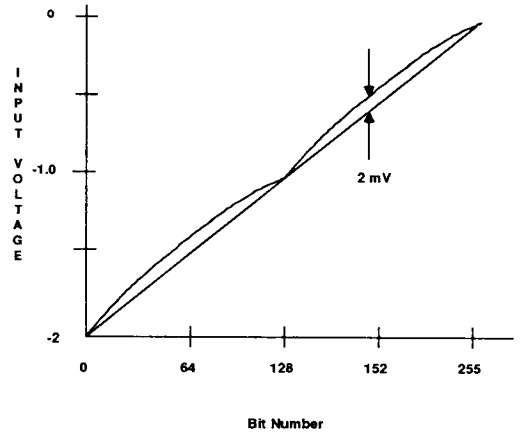


FIGURE 3B Linearity Curve with TAPS Forced to Within .5mV of Ideal

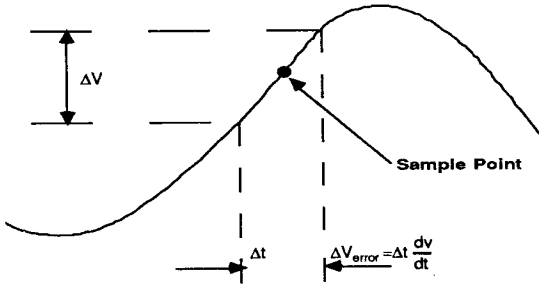


FIGURE 3C Aperture Uncertainty

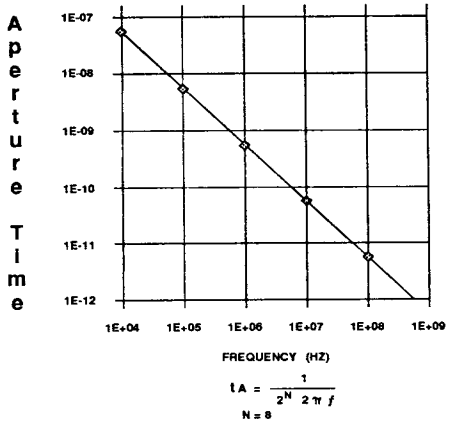
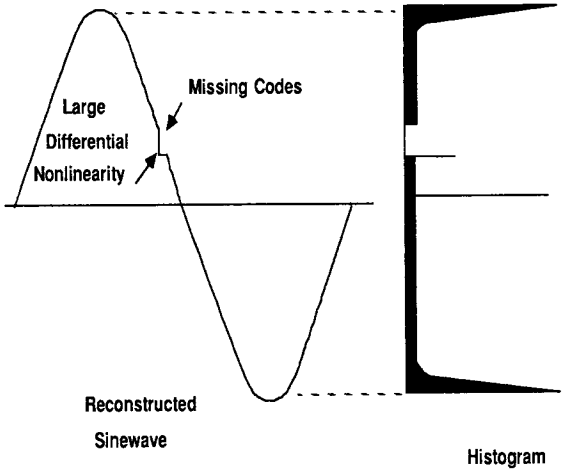


FIGURE 4 Aperture Time - Sinewaves



In the histogram test, A/D transfer function step widths larger than ideal show up as "spikes" in the histogram. Codes missing from the transfer function show up as "bins" with zero counts.

FIGURE 5 Histogram Testing

CHARACTERISTIC TESTING

TESTING

All of the following tests can be performed using Hewlett-Packard equipment as referred to in H.P. Product Note 5180A-2. Test methods available to measure the previous specifications are explained as follows and listed in Table 2.

HISTOGRAM TESTING

In histogram testing, a full scale sinewave of specified frequency is input to the HADC77200. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A/D converter. Several hundred thousand samples of the signal are taken and processed into a histogram. At the end of the sampling, the histogram is plotted with possible output codes along the x-axis and frequency of occurance along the y-axis. Above each possible output code (the x-axis is from 0 to 256), a point is plotted whose height is proportional to the total number of times that code occurs. For a sinewave input, a perfect A/D converter would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi(A^2 - V^2)^{-1/2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurance at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. A step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts (See Figure 5).

FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is another useful tool for evaluating A/D converter dynamic performance. Implemented using a Fast Fourier Transform algorithm, the DFT converts a finite time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the A/D converter's dynamic transfer function may be measured. Harmonics of the input sinewave, caused by the integral nonlinearity, are aliased

SPECIFICATION TESTING CONTINUED:

into the baseband spectrum and can be readily identified and measured. Additional effects can be measured as shown in Table 2.

SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the HADC77200. Using least squared error minimization techniques, an idealized sinewave fit to the data is calulated by software. The sinewave is in the form:

$$A\sin(2\pi ft+\theta)+DC$$

where A,f,θ,DC are the parameters which are selected for a best fit to the data. The idealized best fit sine-wave, $A_0\sin(2\pi f_0 t+\theta_0)+DC_0$ is then subtracted from the digitized time record.

The rms errors are then calculated and the effective bits specification is found.

BEAT FREQUENCY TEST

Beat frequency testing is a qualitative test for A/D converter dynamic performance and may be used to quickly judge whether or not there are any gross problems with the HADC77200. In this technique, a full scale sinewave input signal is offset slightly in frequency from the A/D converters sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the A/D's output ideally would change by 1 LSB at the point of maximum slope. Thus the A/D sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency, Δ f, is observed. Differential nonlinear-ities show up as nonuniform horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

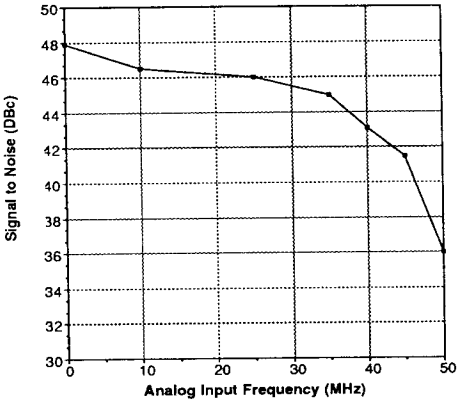
TABLE 2
TESTS

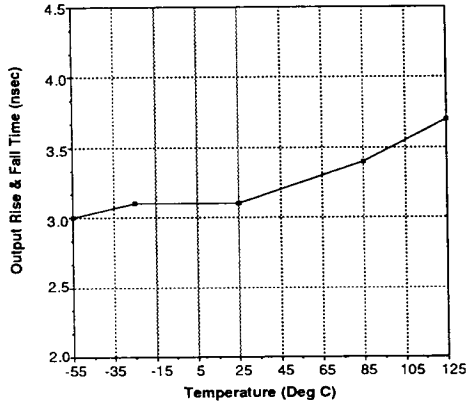
The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

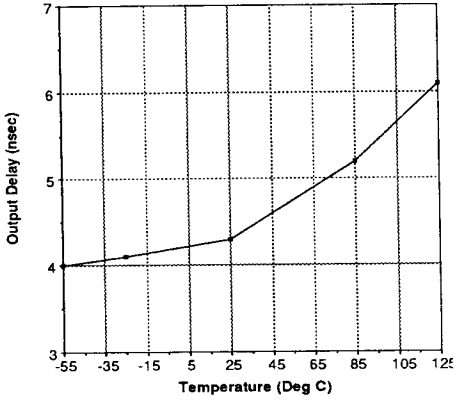
(Table from H. P. Product Note 5180A-2)

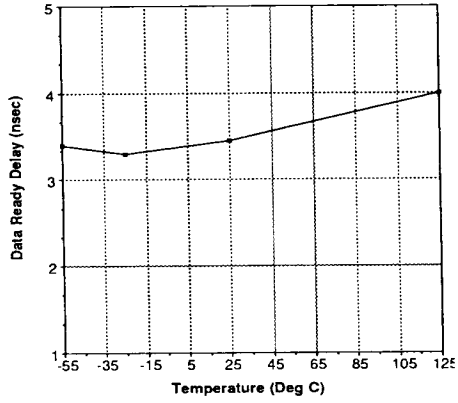
ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes-shows up as spikes	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Missing Codes	Yes-shows up as bins with 0 counts	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Integral Nonlinearity	Yes (could be measured directly with highly linear ramp waveform)	Yes-shows up as harmonics of fundamental aliased into baseband	Yes-part of RMS error	Yes
Aperature Uncertainty	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Noise	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Bandwidth Errors	No	No	No	Yes-used to measure analog bandwidth.
Gain Errors	Yes-shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes-shows up in offset of distribution average.	No	No	No

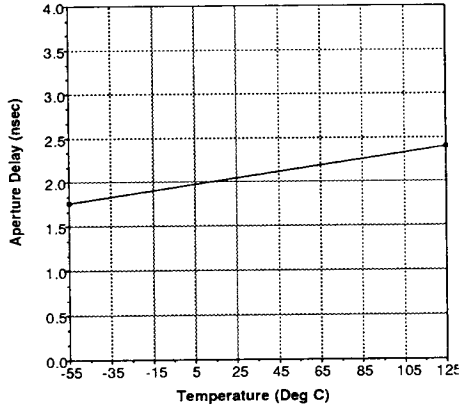
CHARACTERIZATION GRAPHS

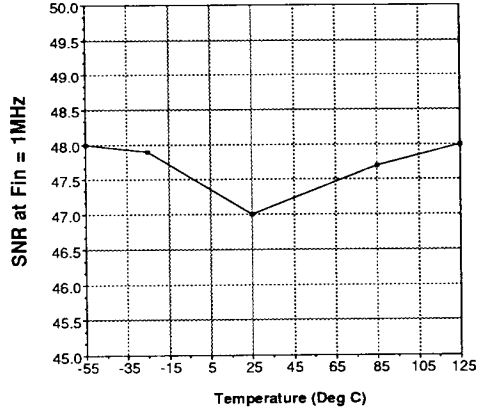




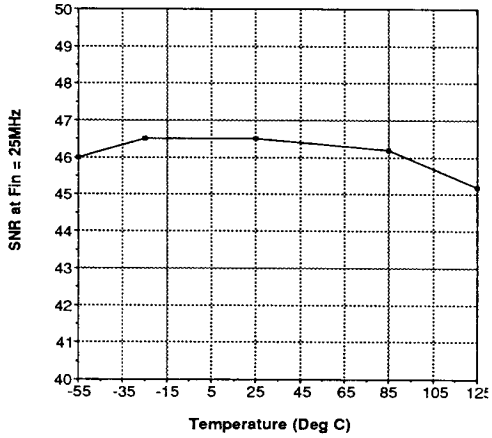


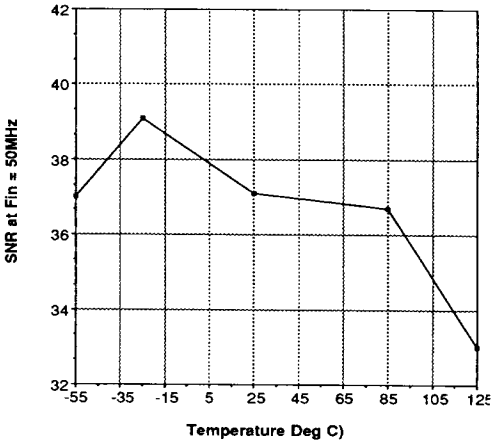




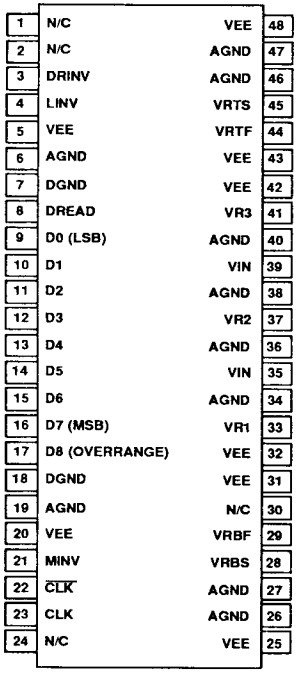


CHARACTERIZATION GRAPHS (con't.)





PIN ASSIGNMENT HADC77200



NAME	FUNCTION
VEE	Negative Supply Nominally -5.2V
LINV	D0 through D6 Output Inversion Control Pin
DREAD	Data Ready Output
DGND	Digital Ground
AGND	Analog Ground
D0	Digital Data Output Pin 1 (LSB)
D1- D6	Digital Data Output Pin 2 through Pin 6
D7	Digital Data Output Pin 7 (MSB)
D8	Overrange Output
MINV	D7 Output Inversion Control Pin

NAME	FUNCTION
CLK	ECL Clock Input Pin
$\overline{\text{CLK}}$	ECL Clock Input Pin
DRINV	Data Ready Inverse
VRBS	Reference Voltage Bottom, Sense, Nominally -2.0V
VRBF	Reference Voltage Bottom, Force, Nominally -2.0V
VIN	Analog Input, connected to the input signal or used as Sense
VR1	Reference Voltage Tap 1
VR2	Reference Voltage Tap 2
VR3	Reference Voltage Tap 3
VRTS	Reference Voltage Top, Sense, Nominally -2.0V
VRTF	Reference Voltage Top, Force, Nominally -2.0V

48 LEAD CERAMIC SIDEBRAZED DIP

**For Ordering Information See Section 1.*