ML610Q474/ML610Q475/ML610Q476

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

This LSI is a high performance CMOS 8-bit microcontroller equipped with an 8-bit CPU nX-U8/100 and integrated with peripheral functions such as the UART, melody driver, Analog compartor, and LCD driver.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by 3-stage pipe line architecture parallel processing. Additionally, it adopts the low-/high-speed dual clock system, standby mode, and process that prohibits leak current at high temperatures, and is most suitable for battery-driven applications.
MTP version can rewrite programs on-board, which can contribute to reduction in product development TAT. The flash memory incorporated into this MTP version implements the mask ROM-equivalent low-voltage operation (1.25V or higher) and low-power consumption (typically 4.5uA at low-speed operation), enabling volume production by the MTP version.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit length instruction
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    30.5 μs (@ 32.768 kHz system clock)
    2 μs (@ 500 kHz system clock)
    0.5 μs (@ 2 MHz system clock)

- Internal memory
  - Internal 16KByte flash memory (8K x 16 bits) (including unusable 1K Byte TEST area)
  - Internal 1KByte RAM (1024 x 8 bits)

- Interrupt controller
  - 1 non-maskable interrupt source:
    Internal source: 1 (Watchdog Timer)
  - 22 maskable interrupt sources:
    Internal source: 12 (Timer0, Timer1, Timer 2, Timer 3, Timer C, Timer D, UART0, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz, Analog Comparator)
    External source: 10 (P00, P01, P02, P03, P50, P51, P52, P53, P54, P56)
    (One interrupt request is generated from P50 to P54, P56 interrupt sources.)

- Time base counter
  - Low-speed time base counter x 1 channel
    Frequency compensation (Compensation range: Approx. -488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter x 1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, 8s)

- Timers
  - 8 bits x 6 channels [also available is 16-bit x 3 configuration (using Timers 0-1, 2-3, or C-D)]
  - Clock frequency measurement function mode (16-bit configuration using Timers 2 and 3 x 1 channel only)
  - The timer C and timer D are controlled by the external trigger.
  - The timer C and timer D are used for the one-shot timer mode.

- Capture
  - Time base capture x 2 channels (4096 Hz to 32 Hz)

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- Analog Comparator
  - Operating voltage: V_{DD}=1.8V～3.6V
  - Common mode input voltage: 0.2V～VDD－0.2V
  - Input offset voltage: 30mV(max)
  - Interrupt allow edge selection and sampling selection
  - The RC discharged type A/D convertor is configured with the timers C and D.
  - The temperature measurement function using built-in temperature sensor.
    Temperature measurement range: -20°C to +70°C
  - The reference voltage can be switched between CMPP0, CMPM0, temperature sensor and the internal 0.7V voltage source.

- General-purpose ports
  - Input-only port: 4 channels (including secondary functions)
  - Output-only port
    ML610Q474: 10 channels (including secondary functions)
    ML610Q475: 6 channels (including secondary functions)
    ML610Q476: 2 channels (including secondary functions)
  - Input/output port: 10 channels (including secondary functions)

- LCD driver
  - Number of segments
    ML610Q474: Up to 135 dots (select among 27 segments x 5 commons, 28 segments x 4 commons, 29 segments x 3 commons, and 30 segments x 2 commons)
    ML610Q475: Up to 155 dots (select among 31 segments x 5 commons, 32 segments x 4 commons, 33 segments x 3 commons, and 34 segments x 2 commons)
    ML610Q476: Up to 175 dots (select among 35 segments x 5 commons, 36 segments x 4 commons, 37 segments x 3 commons, and 38 segments x 2 commons)
  - 1/1 to 1/5 duty
  - 1/2 or 1/3 bias (built-in bias generation circuit)
  - Frame frequency selectable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow
  - Reset by the low-speed oscillation stop detection (Available by a mask option)

- Clock
  - Low-speed clock (Operation of this LSI is not guaranteed under a condition with no supply of low-speed crystal oscillation clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock
    Built-in RC oscillation (500 kHz, 2 MHz)

- Power management
  - HALT mode: Suspends the instruction execution by CPU (peripheral circuits are in operating states)
  - STOP mode: Stops the low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - High-speed clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block control function: Completely stops the operation of any function block circuit that is not used (resets registers and stops clock)
  - When LSCLK is selected for system clock, the power consumption can be reduced by using halver circuit.

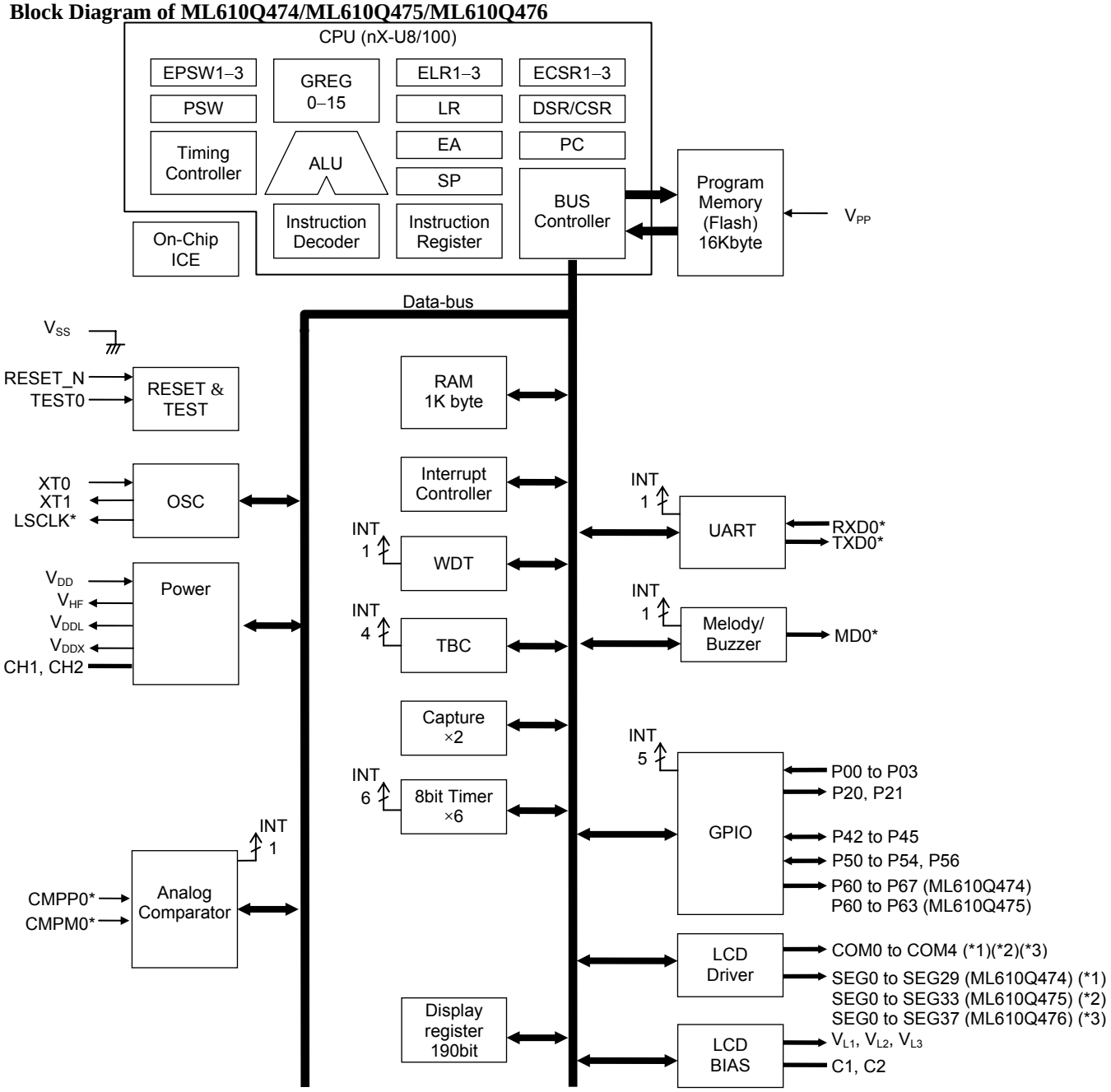
- Shipment
  – Chip (Die)
    ML610Q474-xxxWA
    ML610Q475-xxxWA
    ML610Q476-xxxWA
  – 80-pin plastic TQFP
    ML610Q474-xxxTBZ0ARL
    ML610Q475-xxxTBZ0ARL
    ML610Q476-xxxTBZ0ARL

  xxx: ROM code number (xxx of the blank product is NNN)
  Q: MTP version
  WA: Chip (Die)
  TBZ0ARL: TQFP

- Guaranteed Operation Range
  – Operating temperature: -20°C to +70°C
  – Operating voltage: V_{DD} = 1.25V to 3.6V (2.4V to 3.6V used halver circuit)

BLOCK DIAGRAM

Block Diagram of ML610Q474/ML610Q475/ML610Q476



* Secondary function or Tertiary function

(*1) Select among 27 segments x 5 commons, 28 segments x 4 commons, 29 segments x 3 commons, and 30 segments x 2 commons with the register

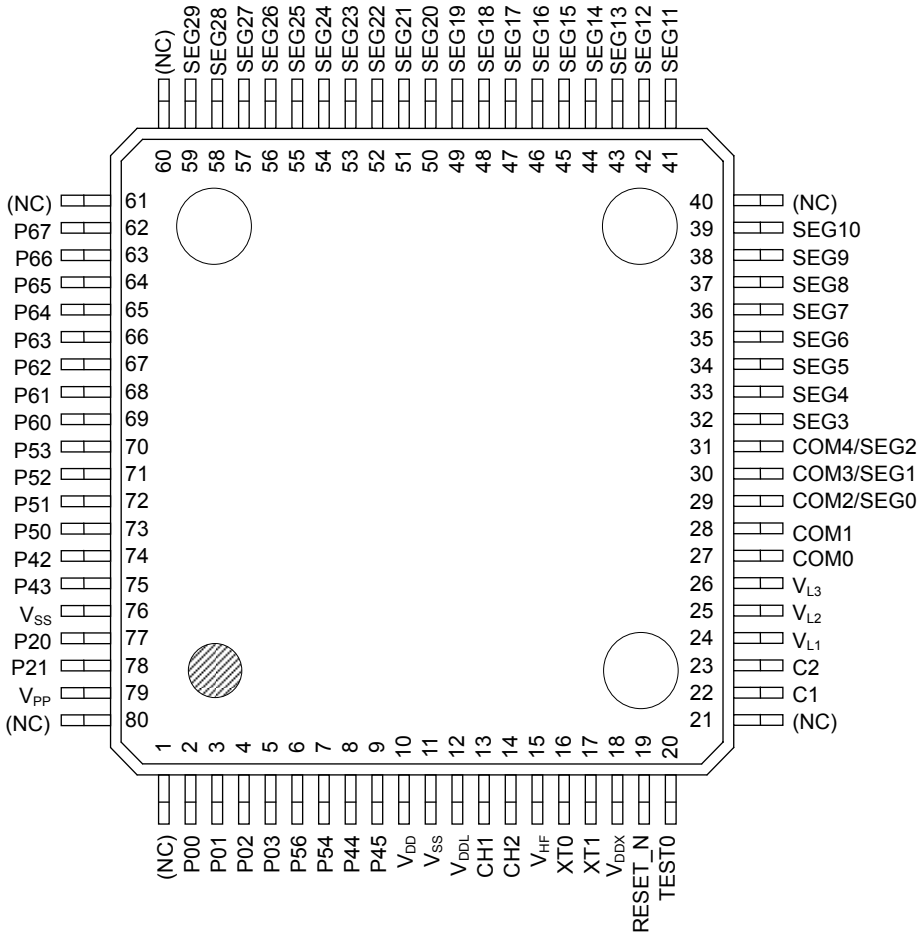
(*2) Select among 31 segments x 5 commons, 32 segments x 4 commons, 33 segments x 3 commons, and 34 segments x 2 commons with the register

(*3) Select among 35 segments x 5 commons, 36 segments x 4 commons, 37 segments x 3 commons, and 38 segments x 2 commons with the register

Figure 1 ML610Q474/ML610Q475/ML610Q476 Block Diagram

PACKAGE PIN/CHIP PAD LAYOUT

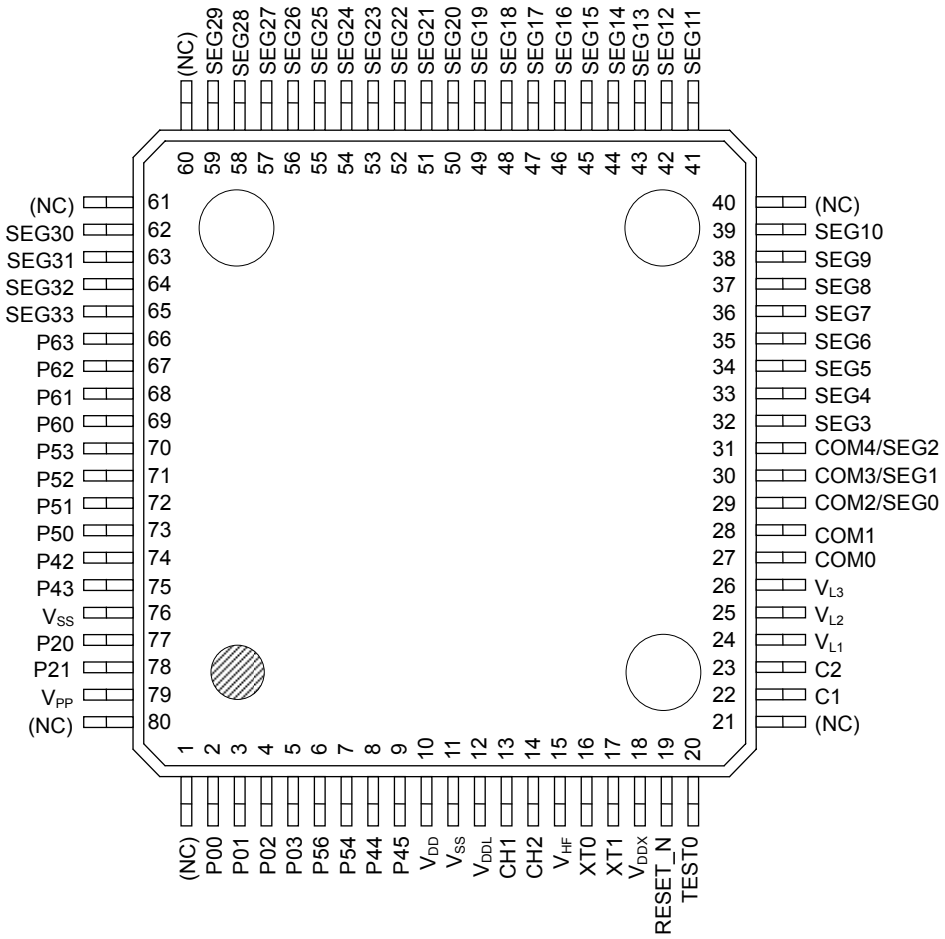
ML610Q474 80pin TQFP Package Pin Layout



(NC): No Connection

Figure 2 ML610Q474 80pin TQFP Package Pin Layout

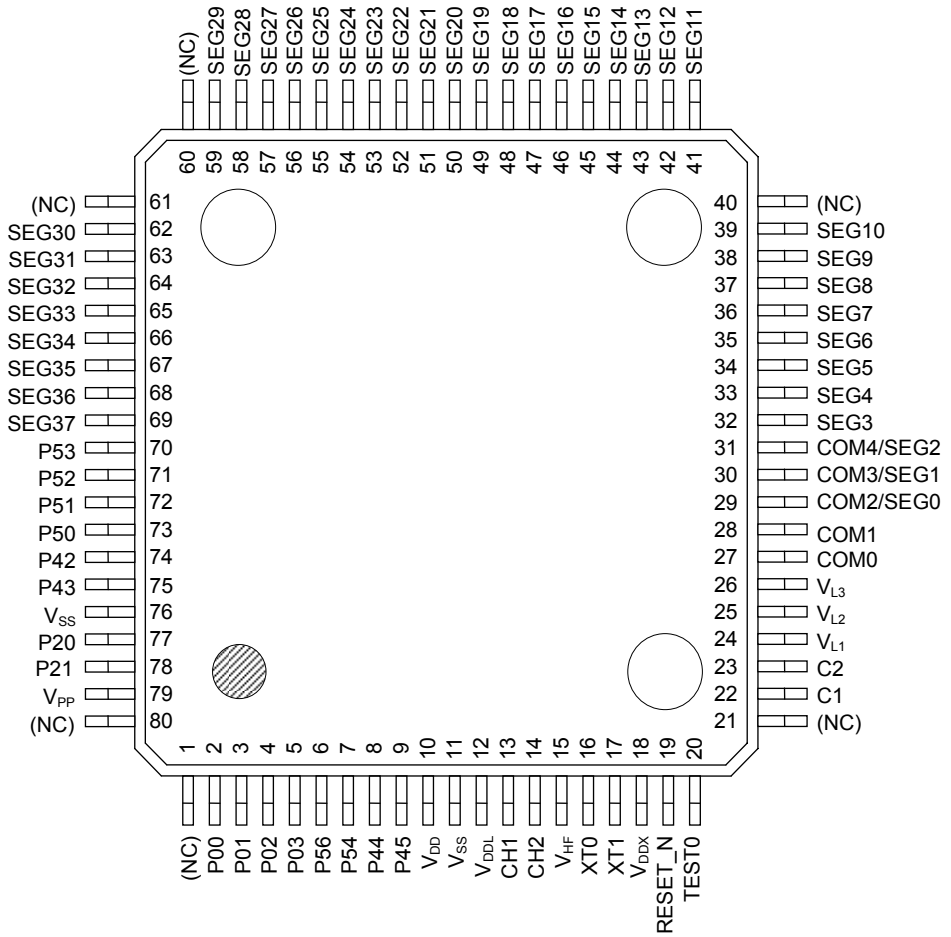
ML610Q475 80pin TQFP Package Pin Layout



(NC): No Connection

Figure 3 ML610Q475 80pin TQFP Package Pin Layout

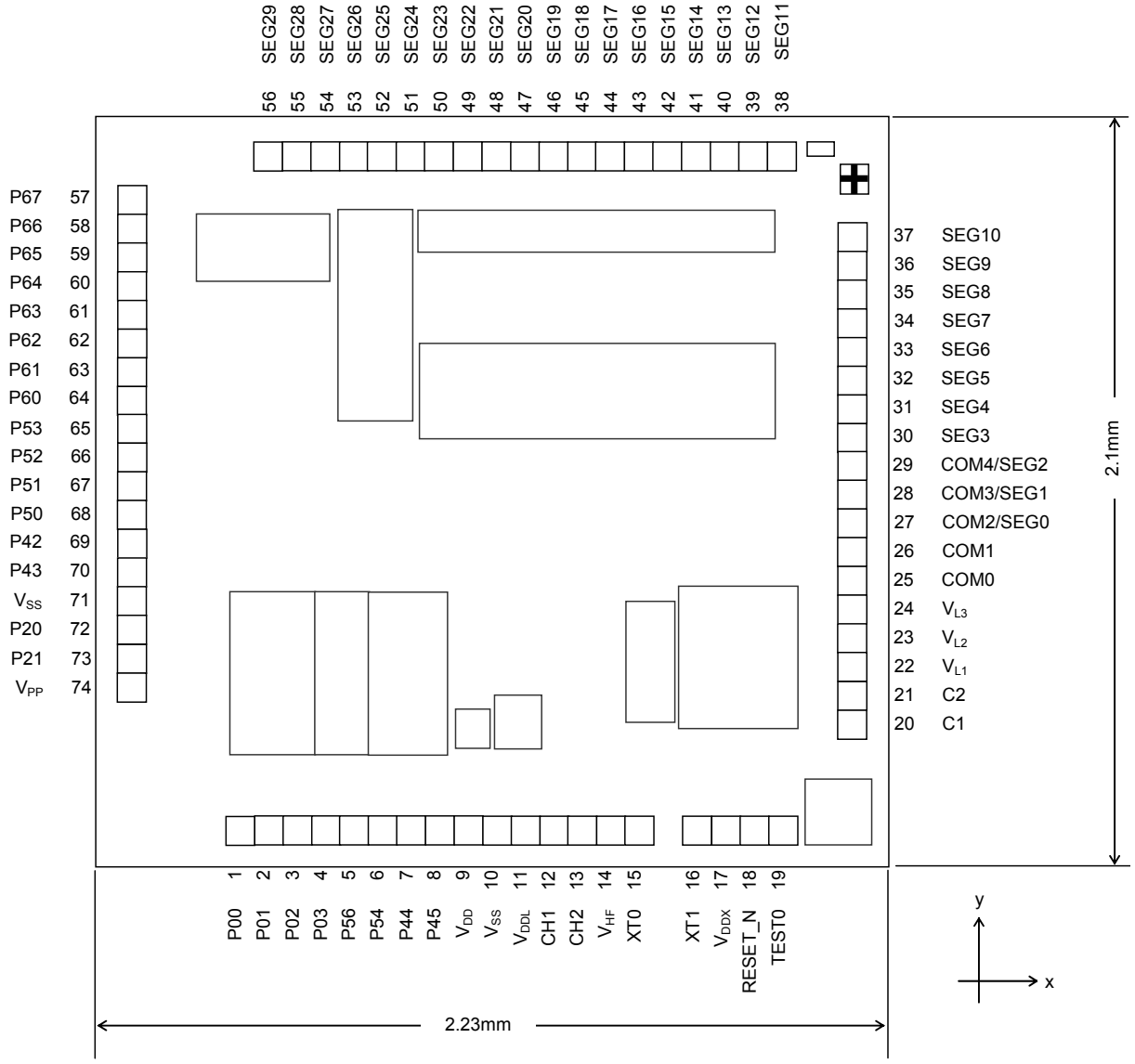
ML610Q476 80pin TQFP Pin Layout



(NC): No Connection

Figure 4 ML610Q476 80pin TQFP Package Pin Layout

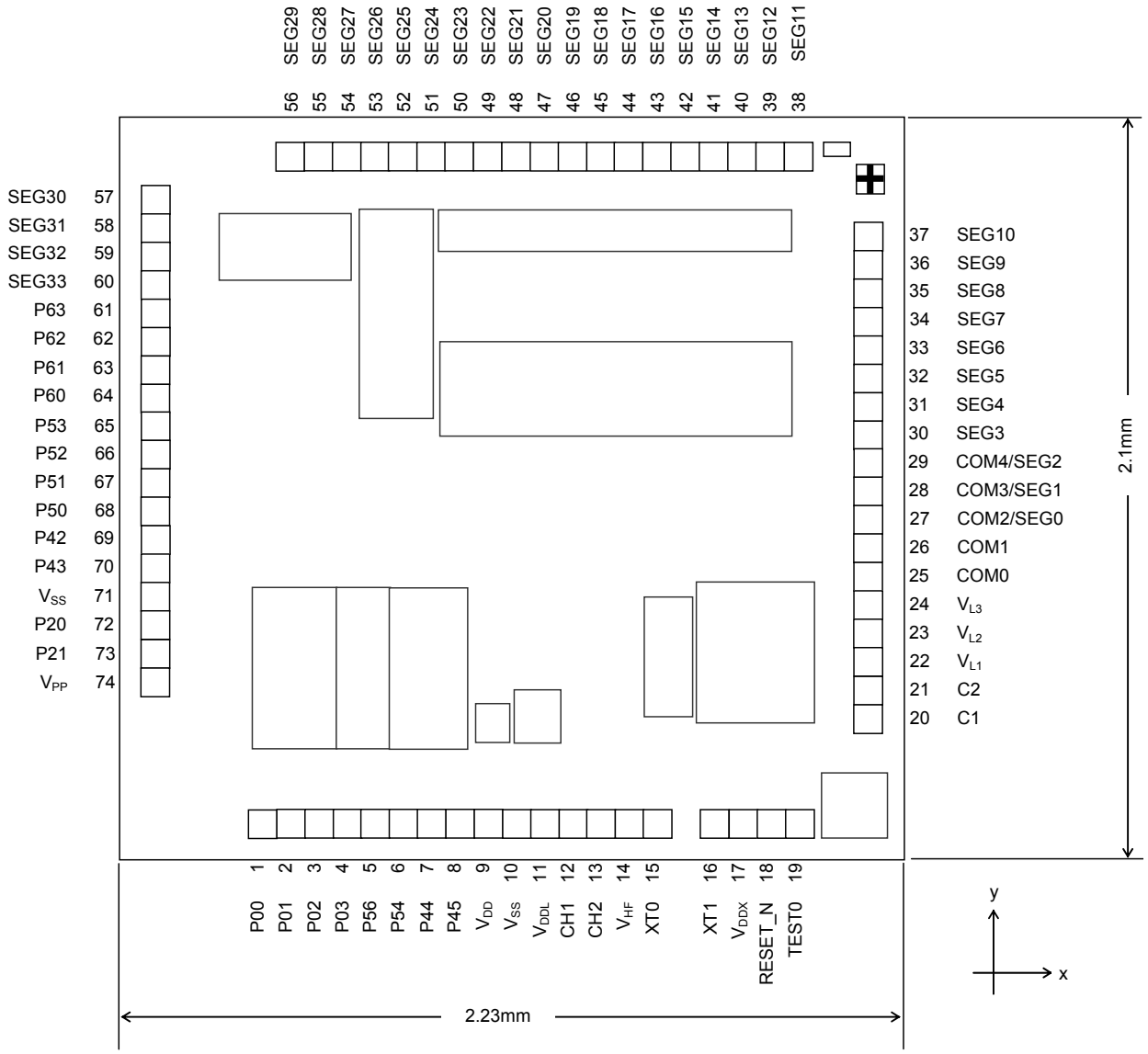
ML610Q474 Chip Pad Layout & Dimension



Chip size: 2.23mm ×2.10mm
PAD count: 74 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: VSS level.

Figure 5 ML610Q474 Chip Pin Layout & Dimension

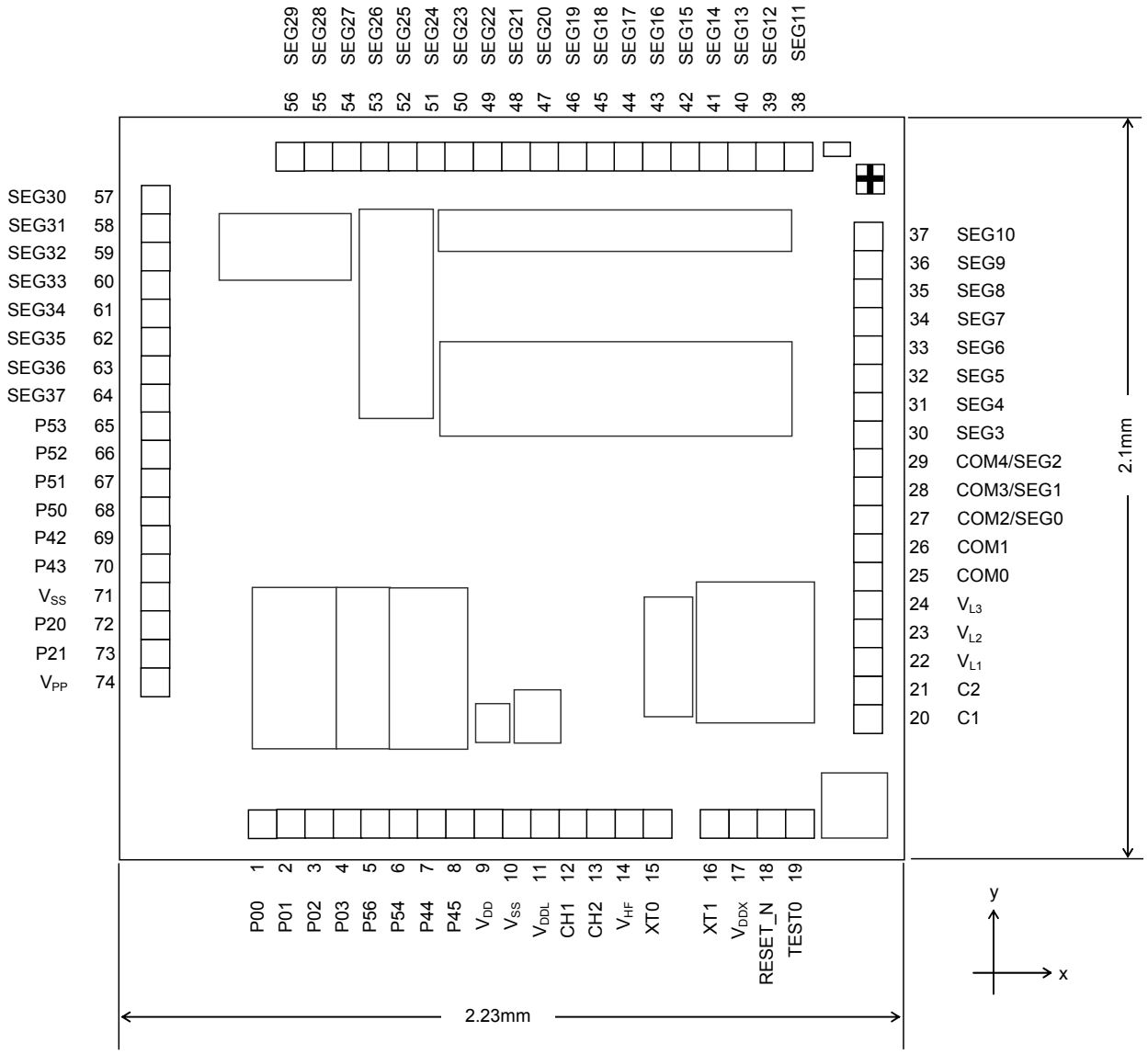
ML610Q475 Chip Pad Layout & Dimension



Chip size: 2.23mm ×2.10mm
PAD count: 74 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

Figure 6 ML610Q475 Chip Pin Layout & Dimension

ML610Q476 Chip Pad Layout & Dimension



Chip size: 2.23mm ×2.10mm
PAD count: 74 pins
Minimum PAD pitch: 80 μm
PAD aperture: 70 μm×70 μm
Chip thickness: 350 μm
Voltage of the rear side of chip: V_{SS} level.

Figure 7 ML610Q476 Chip Pin Layout & Dimension

PAD COORDINATES

ML610Q474/ML610Q475/ML610Q476 Pad Coordinates

Table 1 ML610Q474/ML610Q475/ML610Q476 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	ML610Q474/5/6		PAD No.	Pad Name	ML610Q474/5/6	
		X (μm)	Y (μm)			X (μm)	Y (μm)
1	P00	-705	-944	44	SEG17	330	944
2	P01	-625	-944	45	SEG18	250	944
3	P02	-545	-944	46	SEG19	170	944
4	P03	-465	-944	47	SEG20	90	944
5	P56	-385	-944	48	SEG21	10	944
6	P54	-305	-944	49	SEG22	-70	944
7	P44	-225	-944	50	SEG23	-150	944
8	P45	-145	-944	51	SEG24	-230	944
9	V_{DD}	-65	-944	52	SEG25	-310	944
10	V_{SS}	15	-944	53	SEG26	-390	944
11	V_{DDL}	95	-944	54	SEG27	-470	944
12	CH1	175	-944	55	SEG28	-550	944
13	CH2	255	-944	56	SEG29	-630	944
14	V_{HF}	335	-944	57	P67(*1) SEG30(*2) (*3)	-1009	835
15	XT0	415	-944				
16	XT1	575	-944	58	P66(*1) SEG31(*2) (*3)	-1009	755
17	V_{DDX}	655	-944				
18	RESET_N	735	-944	59	P65(*1) SEG32(*2) (*3)	-1009	675
19	TEST0	815	-944				
20	C1	1009	-650	60	P64(*1) SEG33(*2) (*3)	-1009	595
21	C2	1009	-570				
22	V_{L1}	1009	-490	61	P63(*1) (*2) SEG34(*3)	-1009	515
23	V_{L2}	1009	-410				
24	V_{L3}	1009	-330	62	P62(*1) (*2) SEG35(*3)	-1009	435
25	COM0	1009	-240				
26	COM1	1009	-160	63	P61(*1) (*2) SEG36(*3)	-1009	355
27	COM2/SEG0	1009	-80				
28	COM3/SEG1	1009	0	64	P60(*1) (*2) SEG37(*3)	-1009	275
29	COM4/SEG2	1009	80				
30	SEG3	1009	160	65	P53	-1009	175
31	SEG4	1009	240	66	P52	-1009	95
32	SEG5	1009	320	67	P51	-1009	15
33	SEG6	1009	400	68	P50	-1009	-65
34	SEG7	1009	480	69	P42	-1009	-145
35	SEG8	1009	560	70	P43	-1009	-225
36	SEG9	1009	640	71	V_{SS}	-1009	-305
37	SEG10	1009	720	72	P20	-1009	-385
38	SEG11	810	944	73	P21	-1009	-465
39	SEG12	730	944	74	V_{PP}	-1009	-545
40	SEG13	650	944				
41	SEG14	570	944				
42	SEG15	490	944				
43	SEG16	410	944				

(*1) Pad for ML610Q474 . (*2) Pad for ML610Q475. (*3) Pad for ML610Q476.

PIN LIST

PIN No.	PAD No.	Primary function			Secondary function		
		Pin name	I/O	Function	Pin name	I/O	Function
11, 76	10,71	Vss	—	Negative power supply pin	—	—	—
10	9	V_{DD}	—	Positive power supply pin	—	—	—
15	14	V_{HF}	—	Power supply pin for halver circuit (internally generated)	—	—	—
12	11	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—
18	17	V_{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—
79	74	V_{PP}	—	Power supply pin for Flash ROM	—	—	—
24	22	V_{L1}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)(*2)	—	—	—
25	23	V_{L2}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)(*2)	—	—	—
26	24	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—
22	20	C1	—	Capacitor connection pin for LCD bias generation	—	—	—
23	21	C2	—	Capacitor connection pin for LCD bias generation	—	—	—
13	12	CH1	—	Capacitor connection pin for halver circuit	—	—	—
14	13	CH2	—	Capacitor connection pin for halver circuit	—	—	—
20	19	TEST0	I/O	Test pin	—	—	—
19	18	RESET_N	I	Reset input pin	—	—	—
16	15	XT0	I	Low-speed clock oscillation pin	—	—	—
17	16	XT1	O	Low-speed clock oscillation pin	—	—	—
2	1	P00/EXI0/ CAP0/TPRUN0	I	Input port, External interrupt, Capture 0 input Timer C/Timer D external trigger input	—	—	—
3	2	P01/EXI1/ CAP1/TPRUN1	I	Input port, External interrupt, Capture 1 input Timer C/Timer D external trigger input	—	—	—
4	3	P02/EXI2/ RXD0/TPRUN2	I	Input port, External interrupt, UART0 received data Timer C/TimerD external trigger input	—	—	—
5	4	P03/EXI3/ TPRUN3	I	Input port, External interrupt Timer C/Timer D external trigger input	—	—	—
77	72	P20/LED0	O	Output port	LSCLK	O	Low-speed clock output
78	73	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output
74	69	P42	I/O	Input/output port	RXD0	I	UART data input
75	70	P43	I/O	Input/output port	TXD0	O	UART data output
8	7	P44/T02DCK/ TCDRUN	I/O	Input/output port, Timer 0/Timer 2/Timer C external clock input Timer C/Timer D external trigger Input	—	—	—
9	8	P45/T13DCK/ TCDRUN	I/O	Input/output port, Timer 1/Timer 3/Timer D external clock input Timer C/Timer D external trigger input	—	—	—
73	68	P50/EXI8	I/O	Input/output port, External interrupt	MD0	O	Melody 0 output
72	67	P51/EXI8	I/O	Input/output port, External interrupt	—	—	—
71	66	P52/EXI8	I/O	Input/output port, External interrupt	—	—	—
70	65	P53/EXI8	I/O	Input/output port, External interrupt	—	—	—

PIN No.	PAD No.	Primary function			Secondary function		
		Pin name	I/O	Function	Pin name	I/O	Function
7	6	P54/EXI8/ CMPP0	I/O	Input/output port, External interrupt Analog comparator noninverting input0 pin	—	—	—
6	5	P56/EXI8/ CMPM0	I/O	Input/output port, External interrupt Analog comparator inverting input0 pin	—	—	—

PIN No.	PAD No.	Primary function			Secondary function		
		Pin name	I/O	Function	Pin name	I/O	Function
27	25	COM0	O	LCD common pin	—	—	—
28	26	COM1	O	LCD common pin	—	—	—
29	27	COM2/SEG0	O	LCD common/segment pin	—	—	—
30	28	COM3/SEG1	O	LCD common/segment pin	—	—	—
31	29	COM4/SEG2	O	LCD common/segment pin	—	—	—
32	30	SEG3	O	LCD segment pin	—	—	—
33	31	SEG4	O	LCD segment pin	—	—	—
34	32	SEG5	O	LCD segment pin	—	—	—
35	33	SEG6	O	LCD segment pin	—	—	—
36	34	SEG7	O	LCD segment pin	—	—	—
37	35	SEG8	O	LCD segment pin	—	—	—
38	36	SEG9	O	LCD segment pin	—	—	—
39	37	SEG10	O	LCD segment pin	—	—	—
41	38	SEG11	O	LCD segment pin	—	—	—
42	39	SEG12	O	LCD segment pin	—	—	—
43	40	SEG13	O	LCD segment pin	—	—	—
44	41	SEG14	O	LCD segment pin	—	—	—
45	42	SEG15	O	LCD segment pin	—	—	—
46	43	SEG16	O	LCD segment pin	—	—	—
47	44	SEG17	O	LCD segment pin	—	—	—
48	45	SEG18	O	LCD segment pin	—	—	—
49	46	SEG19	O	LCD segment pin	—	—	—
50	47	SEG20	O	LCD segment pin	—	—	—
51	48	SEG21	O	LCD segment pin	—	—	—
52	49	SEG22	O	LCD segment pin	—	—	—
53	50	SEG23	O	LCD segment pin	—	—	—
54	51	SEG24	O	LCD segment pin	—	—	—
55	52	SEG25	O	LCD segment pin	—	—	—
56	53	SEG26	O	LCD segment pin	—	—	—
57	54	SEG27	O	LCD segment pin	—	—	—
58	55	SEG28	O	LCD segment pin	—	—	—
59	56	SEG29	O	LCD segment pin	—	—	—
62	57	P67(*2)	O	Output port	—	—	—
		SEG30(*3) (*4)	O	LCD segment pin	—	—	—
63	58	P66(*2)	O	Output port	—	—	—
		SEG31(*3) (*4)	O	LCD segment pin	—	—	—
64	59	P65(*2)	O	Output port	—	—	—
		SEG32(*3) (*4)	O	LCD segment pin	—	—	—
65	60	P64(*2)	O	Output port	—	—	—
		SEG33(*3) (*4)	O	LCD segment pin	—	—	—
66	61	P63(*2) (*3)	O	Output port	—	—	—
		SEG34(*4)	O	LCD segment pin	—	—	—
67	62	P62(*2) (*3)	O	Output port	—	—	—
		SEG35(*4)	O	LCD segment pin	—	—	—
68	63	P61(*2) (*3)	O	Output port	—	—	—
		SEG36(*4)	O	LCD segment pin	—	—	—
69	64	P60(*2) (*3)	O	Output port	—	—	—
		SEG37(*4)	O	LCD segment pin	—	—	—

(*3) Pad for ML610Q474 . (*4) Pad for ML610Q475. (*5) Pad for ML610Q476.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal resonator is connected to this pin. Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS}. (see appendix C measuring circuit 1)	—	—
XT1	O		—	—
LSCLK	O	Low-speed clock output. Assigned to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00 to P03	I	General-purpose input port.	Primary	Positive
General-purpose output port				
P20, P21	O	General-purpose output port. This cannot be used as the general output port when used as the secondary function.	Primary	Positive
General-purpose input/output port				
P42 to P45	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary or tertiary function.	Primary	Positive
P50 to P54, P56	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive
P60 to P63	O	General-purpose output port. Incorporated only into ML610Q474/ML610Q475, and not into ML610Q476.	Primary	Positive
P64 to P67	O	General-purpose output port. Incorporated only into ML610Q474, and not into ML610Q475/ ML610Q476.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
External interrupt				
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00 to P03 pins.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. Assigned to the primary function of the P50 to P54, P56 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T02CK	I	External clock input pin used for both Timer 0 and Timer 2. This pin is used as the primary function of the P44 pin.	Primary	—
T13CK	I	External clock input pin used for both Timer 1 and Timer 3. This pin is used as the primary function of the P45 pin.	Primary	—
TCDRUN	I	External trigger input pin used for Timer C or Timer D. This pin is used as the primary function of the P44 pin or the P45 pin.	Primary	—
TPRUN0	I	External trigger input pin used for Timer C or Timer D. This pin is used as the primary function of the P00 pin.	Primary	—
TPRUN1	I	External trigger input pin used for Timer C or Timer D. This pin is used as the primary function of the P01 pin.	Primary	—
TPRUN2	I	External trigger input pin used for Timer C or Timer D. This pin is used as the primary function of the P02 pin.	Primary	—
TPRUN3	I	External trigger input pin used for Timer C or Timer D. This pin is used as the primary function of the P03 pin.	Primary	—
LED drive				
LED0, LED1	O	N-channel open drain output pins to drive LED. This pin is used as the primary function of the P20 and the P21 pins.	Primary	Positive /negative
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P50 pin.	Secondary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary	Logic
Analog Comparator				
CMPP0	I	Analog comparator noninverting input0 pin. This pin is used as the secondary function of the P54.	Primary	—
CMPM0	I	Analog comparator inverting input0 pin. This pin is used as the secondary function of the P56.	Primary	—
LCD drive signal				
COM0 to COM4	O	Common output pins. COM2, COM3, and COM4 can be switched to SEG0, SEG1, and SEG2, respectively, through the register setting. To change the setting, switch between COM4 and SEG2 for one pin and switch between COM3, COM4 and SEG1, SEG2 for two pins.	—	—
SEG0 to SEG29	O	Segment output pin. The SEG0, SEG1, and SEG2 pins are for switching the register setting with the COM2, COM3, and COM4.	—	—
SEG30 to SEG33	O	Segment output pin. Incorporated into ML610Q475/ML610Q476, not into ML610Q474.	—	—
SEG34 to SEG37	O	Segment output pin. Incorporated into ML610Q476, not into ML610Q474/ML610Q475.		
LCD driver power supply				
V_{L1}	—	Power supply pin for LCD bias (internally generated) or power supply connection pin. Depending on LCD Bias setting and V_{DD} voltage level, V_{DD} or V_{DDL} or capacitor is connected. For details of the connection method, see Chapter 20, "LCD Drivers".	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitor C_{12} (see Appendix C measuring circuit 1) is connected between C1 and C2.	—	—
C2	—		—	—

Pin name	I/O	Description	Primary/ Secondary	Logic
Test				
TEST0	I/O	Pin for testing. A pull-down resistor is internally connected.	—	Positive
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{HF}	—	Positive power supply pin (internally generated) for Halver. Capacitor C_{HF} (see measuring circuit 1) should be connected between this pin and V_{SS}.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors C_L (see measuring circuit 1) are connected between this pin and V_{SS}.	—	—
V_{DDX}	—	Positive power supply pin (internally generated) for low-speed oscillation. Capacitor C_X (see measuring circuit 1) should be connected between this pin and V_{SS}.	—	—
CH1	—	Capacitor connection pin for halver circuit. Capacitor C_{H12} (see Appendix C measuring circuit 1) are connected between CH1 and CH2.	—	—
CH2	—		—	—
V_{PP}	—	Power supply pin for programming Flash ROM. A pull-down resistor is internally connected.	—	—

TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

Table 2 Termination of Unused Pins

Pin	Recommended pin handling
VPP	Open
VL1	Open
VL2	Open
VL3	Open
C1, C2	Open
RESET_N	Open
TEST0	Open
P00 to P03	VDD or VSS
P20, P21	Open
P42 to P45	Open
P50 to P54, P56	Open
P60 to P67	Open
COM0 to COM4	Open
SEG0 to SEG37	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS}= 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta=25°C	-0.3 to +4.6	V
Power supply voltage 2	V_{PP}	Ta=25°C	-0.3 to +9.5	V
Power supply voltage 3	V_{DDL}	Ta=25°C	-0.3 to +3.6	V
Power supply voltage 4	V_{L1}	Ta=25°C	-0.3 to +2.0	V
Power supply voltage 5	V_{L2}	Ta=25°C	-0.3 to +4.0	V
Power supply voltage 6	V_{L3}	Ta=25°C	-0.3 to +6.0	V
Input voltage	V_{IN}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port 3 to 6, Ta=25°C	-12 to +11	mA
Output current 2	I_{OUT2}	Port 2, Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	0.9	W
Storage temperature	T_{STG}	—	-55 to +150	°C

Recommended Operating conditions

(V_{SS}= 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	-20 to +70	°C
Operating voltage	V_{DD}	f_{OP}=30k to 625kHz	1.25 to 3.6	V
		f_{OP}=30k to 2.5MHz	1.8 to 3.6	
		f_{OP}=30k to 36kHz, Used Halver	2.4 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD}=1.25 to 3.6V	30k to 625k	Hz
		V_{DD}=1.8 to 3.6V	30k to 2.5M	
		V_{DD}=2.4 to 3.6V, Used Halver	30k to 36k	
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitance	C_{DL}	—	3 to 18	pF
	C_{GL}	—	3 to 18	
V_{DDL} pin external capacitance	C_L	—	0.47±30%	µF
V_{DDX} pin external capacitance	C_X	—	0.1±30%	µF
V_{HF} pin external capacitance	C_{HF}	—	0.1±30%	µF
$V_{L1, 2, or 3}$ pin external capacitance	$C_{a,b,c}$	—	0.1±30%	µF
Pin-to-pin (C1 to C2) external capacitance	C_{12}	—	0.47±30%	µF
Pin-to-pin (CH1 to CH2) external capacitance	C_{H12}	—	0.1±30%	µF

Operating conditions of FlashROM

(VSS= 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase	2.75 to 3.6	V
	V_{DDL}	At write/erase*1	2.5 to 2.75	
	V_{PP}	At write/erase	7.7 to 8.3	
Rewrite count	C_{EP}	—	80	cycles
Data retention	Y_{DR}	—	10	years

*1: When writing to and erasing on the flash Memory, the voltage in the specified range needs to be supplied to the V_{DDL} pin. The V_{PP} pin has an internal pull-down resistor.

Operation conditions of Comparator

(VDD=1.8 to 3.6V, VSS=0V, Ta=-20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Common-mode input voltage	CMV_{IN}	—	0.2	—	V_{DD} – 0.2	V	1
Analog Comparator Input offset voltage	V_{CMPOF}	Ta=25°C	-30	—	30	mV	
Analog Comparator Response time	T_{CMP}	Ta=25°C, Overdrive=100mV	—	—	1	µs	
Analog Comparator supply current	I_{CMP}	Ta=25°C	—	25	45	µA	
Analog Comparator wakeup time	T_{CMPW}	—	—	—	5	ms	
Temperature sensor output voltage through x2	V_{TMP}	Ta = +25°C	—	1355	—	mV	
Temperature sensor output voltage through x2 (Temperature property)	ΔV_{TMP}	Ta = -20 to +25°C	—	-3.585	—	mV/°C	
		Ta = 25 to 70°C	—	-3.718	—		
0.7V voltage source output voltage through x2	V_{REF}	Ta=25°C	1.386	1.400	1.414	V	
0.7V voltage source temperature deviation	ΔV_{REF}	—	—	0	—	%/°C	
0.7V voltage source supply current	I_{REF}	Ta=25°C	—	20	40	µA	
0.7V voltage source wakeup time	T_{REFW}	—	—	—	1	ms	
1/2 VDD voltage source	VDD2	—	VDD/2x 0.96	VDD/2	VDD/2x 1.04	V	
1/4 VDD voltage source	VDD4	—	VDD/4x 0.945	VDD/4	VDD/4x 1.055	V	

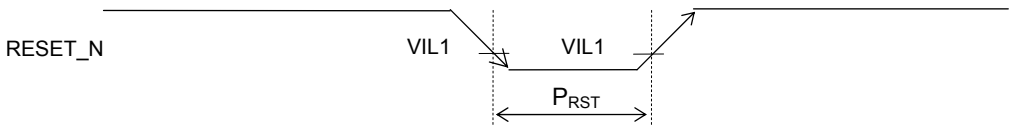
DC Characteristics (1/5)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C unless otherwise specified)

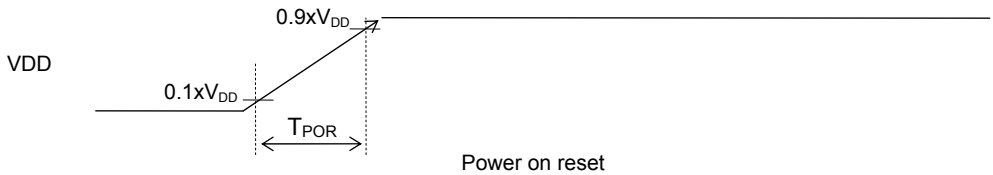
Parameter	Symbol	Condition		Rating			Unit	Measurement circuit
				Min.	Typ.	Max.		
500kHz/2MHz RC oscillation frequency	f_{RC}	V_{DD}=1.25 to 3.6V	Ta=25°C	Typ. -10%	500	Typ. +10%	kHz	
			*2	Typ. -25%	500	Typ. +25%	kHz	
		V_{DD}=1.8 to 3.6V	Ta=25°C	Typ. -10%	2.0	Typ. +10%	MHz	
			*3	Typ. -25%	2.0	Typ. +25%	MHz	
Low-speed crystal oscillation start time*1	T_{XTL}	—		—	0.6	2	s	1
500kHz/2MHz RC oscillation start time	T_{RC}	—		—	—	3	µs	
Reset pulse width	P_{RST}	—		200	—	—	µs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset generated power rise time	T_{POR}	—		—	—	10	ms	
LCD bias voltage generation time*3	T_{BIAS}	—		—	—	100	ms	

*1: 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=12pF).
*2: Recommended operating temperature (Ta=-20 to 70°C)
*3: 1/3bias, VL2=VDD.

RESET

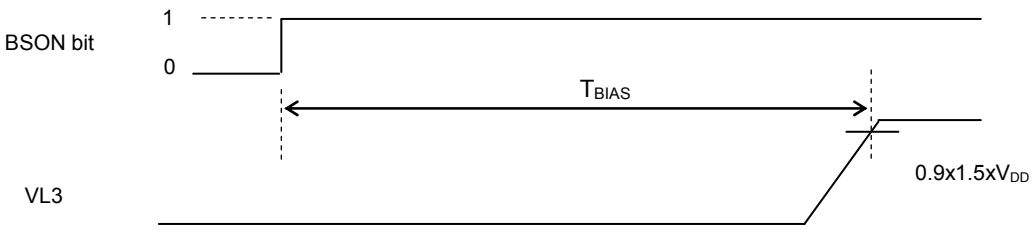


RESET_N pin reset



Power on reset

T_{BIAS}



DC Characteristics (2/5)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
V_{DDL} voltage	V_{DDL}	fop=30k to 36kHz, Used Halver	—	1.15	—	V	1
		fop=30k to 625kHz	—	1.2	—		
		fop=1.5M to 2.5MHz	—	1.5	—		
V_{DDL} temperature deviation *1	ΔV_{DDL}	V_{DD}=3.0V	—	-1	—	mV/°C	
V_{DDL} voltage dependency *1	ΔV_{DDL}	—	—	5	20	mV/V	

*1: The maximum V_{DDL} voltage becomes the V_{DD} voltage level when the V_{DDL} voltage determined by the temperature and voltage deviations mathematically exceeds the V_{DD} voltage.

DC Characteristics (3/5)

(VDD=3.0V, VSS=0V, Ta=-20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Rating			Unit	Measurement circuit
				Min.	Typ.	Max.		
Supply current 1	IDD1	CPU: In STOP state. Low-speed/High-speed oscillation: stopped.	Ta=25°C	—	0.32	0.8	µA	1
			*5	—	—	8		
Supply current 2	IDD2	CPU: In HALT state. (LTBC, WDT: Operating)*3*4. High-speed 500kHz/2MHz oscillation: Stopped. LCD/BIAS circuits: Stopped Used halver	Ta=25°C	—	0.25	0.5	µA	
			*5	—	—	4		
Supply current 3-1	IDD3-1	CPU: In 32.768kHz operating state.*1*3 High-speed 500kHz/2MHz oscillation: Stopped, LCD/BIAS circuits: Operating *2 Not used halver	Ta=25°C	—	4.5	8	µA	
			*5	—	—	15		
Supply current 3-2	IDD3-2	CPU: In 32.768kHz operating state.*1*3 High-speed 500kHz/2MHz oscillation: Stopped, LCD/BIAS circuits: Operating *2 Used halver	Ta=25°C	—	2.5	4	µA	
			*5	—	—	7.5		
Supply current 4-1	IDD4-1	CPU: In 500kHz RC operating state. LCD/BIAS circuits: Operating.*2 Not used halver	Ta=25°C	—	75	100	µA	
			*5	—	—	120		
Supply current 4-2	IDD4-2	CPU: In 2MHz RC operating state. LCD/BIAS circuits: Operating.*2 Not used halver	Ta=25°C	—	300	350	µA	
			*5	—	—	400		

*1: When the CPU operating rate is 100% (no HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : 32.768KHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF)
*4 : Significant bits of BLKCON0 to BLKCON4 registers are all "1" except DLCD bit on BLKCON4.
*5 : Recommended operating temperature (Ta=-20 to 70°C)
*6: LCD stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

DC Characteristics (4/5)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20, P21 (N-channel open drain output mode is not selected)) (P42 to P45) (P50 to P54, P56) (P60 to P63) *2 (P60 to P67) *1	VOH1	IOH1=-0.5mA, V_{DD}=1.8 to 3.6V	V_{DD} -0.5	—	—	V	2
		IOH1=-0.03mA, V_{DD}=1.25 to 3.6V	V_{DD} -0.3	—	—		
	VOL1	IOL1=+0.5mA, V_{DD}=1.8 to 3.6V	—	—	0.5		
		IOL1=+0.1mA, V_{DD}=1.25 to 3.6V	—	—	0.3		
Output voltage 2 (P20, P21 (N-channel open drain output mode is selected))	VOL2	IOL2=+5mA, V_{DD}=1.8 to 3.6V	—	—	0.5		
Output voltage 3 (COM0 to 4) (SEG0 to 29) *1 (SEG0 to 33) *2 (SEG0 to 37) *3	VOH3	IOH3=-0.05mA, VL1=1.2V	V_{L3} -0.2	—	—		
	VOML3	IOML3=+0.05mA, VL1=1.2V	—	—	V_{L2} +0.2		
	VOML3S	IOML3S=-0.05mA, VL1=1.2V	V_{L2} -0.2	—	—		
	VOLM3	IOLM3=+0.05mA, VL1=1.2V	—	—	V_{L1} +0.2		
	VOLM3S	IOLM3S=-0.05mA, VL1=1.2V	V_{L1} -0.2	—	—		
	VOL3	IOL3=+0.05mA, VL1=1.2V	—	—	0.2		
Output leakage (P20, P21) (P42 to P45) (P50 to P54, P56) (P60 to P63) *2 (P60 to P67) *1	IOOH	VOH=V_{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL=V_{SS} (in high-impedance state)	-1	—	—		
Input current 1 (RESET_N, TEST1_N)	IIH1	VIH1=V_{DD}	—	—	1	μA	4
	IIL1	VIL1=V_{SS}	-600	-300	-2		
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	2	300	600		
	IIL2	VIL2=V_{SS}	-1	—	—		
Input current 3 (P00 to P03) (P42 to P45) (P50 to P54, P56)	IIH3	VIH3=V_{DD}, V_{DD}=1.8 to 3.6V (when pulled-down)	2	30	200		
		VIH3=V_{DD}, V_{DD}=1.25 to 3.6V (when pulled-down)	0.01	30	200		
	IIL3	VIL3=V_{SS}, V_{DD}=1.8 to 3.6V (when pulled-up)	-200	-30	-2		
		VIL3=V_{SS}, V_{DD}=1.25 to 3.6V (when pulled-up)	-200	-30	-0.01		
	IIH3Z	VIH3=V_{DD} (in high-impedance state)	—	—	1		
	IIL3Z	VIL3=V_{SS} (in high-impedance state)	-1	—	—		

*1: Characteristics for ML610Q474.
*2: Characteristics for ML610Q475.
*3: Characteristics for ML610Q476.

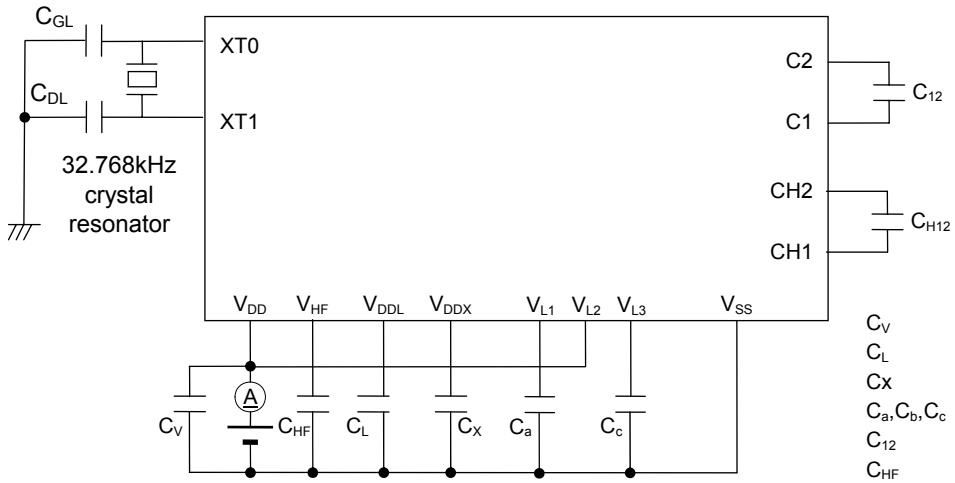
DC Characteristics (5/5)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0) (P00 to P03) (P42 to P45) (P50 to P54, P56)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	5
	VIL1	V_{DD}=1.25 to 3.6V	0	—	0.2 ×V_{DD}		
Input pin capacitance (P00 to P03) (P42 to P45) (P50 to P54, P56)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	—	—	5	pF	—

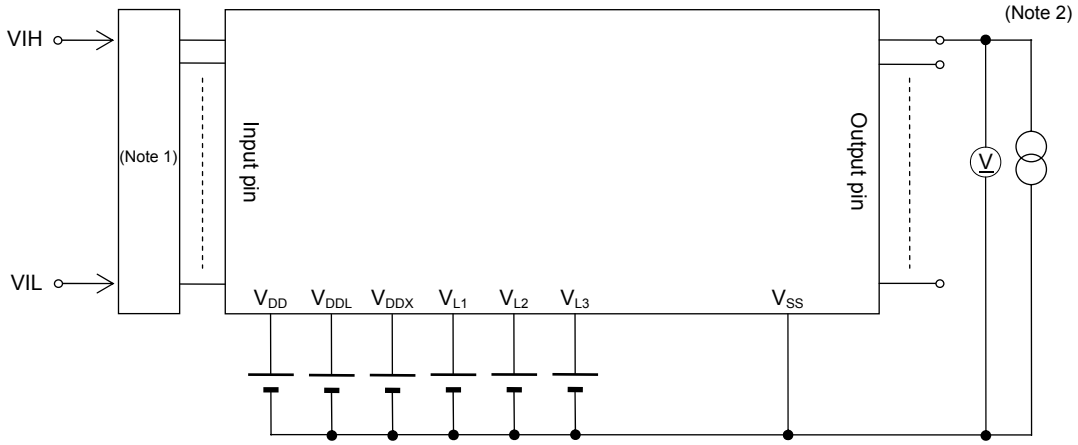
Measuring Circuits

Measuring Circuit 1



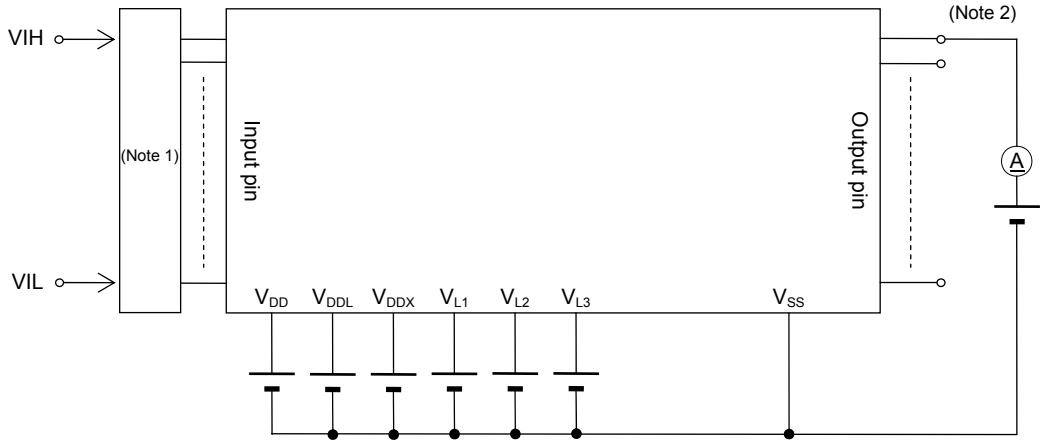
C_V : 1µF
C_L : 0.47uF
Cx : 0.15µF
C_a,C_b,C_c : 0.1µF
C_{12} : 0.47µF
C_{HF} : 0.1µF
C_{H12} : 0.1µF
32.768kHz crystal resonator
: DT-26 (Load capacitance 6pF)
(Made by KDS:DAISHINKU CORP.)
C_{GL}, C_{DL} : 6pF

Measuring Circuit 2



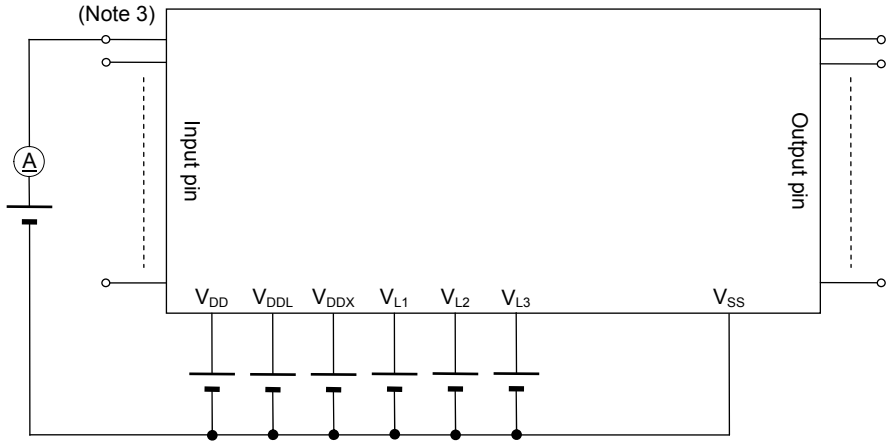
(Note 1) Input logic circuit to determine the specified measuring conditions.
(Note 2) Repeats for the specified output pin

Measuring Circuit 3



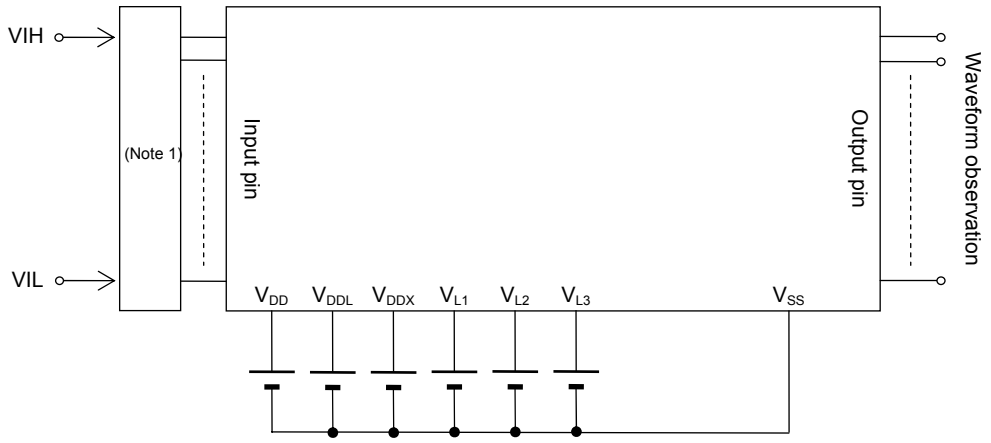
(Note 1) Input logic circuit to determine the specified measuring conditions.
(Note 2) Repeats for the specified output pin

Measuring Circuit 4



(Note 3) Repeats for the specified input pin

Measuring Circuit 5

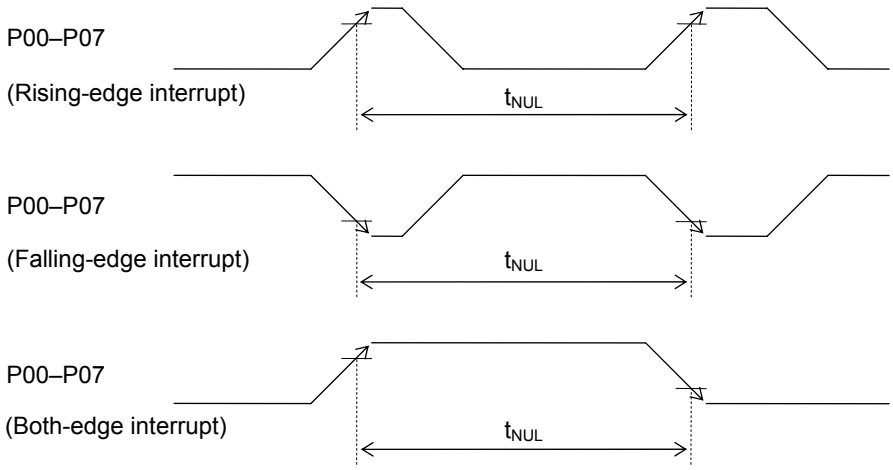


(Note 1) Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

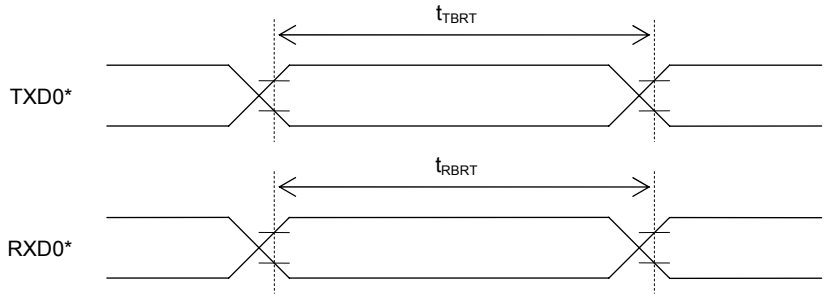


AC Characteristics (UART)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*1	—	s
Receive baud rate	t_{RBRT}	—	BRT*1 -3%	BRT*1	BRT*1 +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA0BRTL,H) and the UART mode register 0 (UA0MOD0).

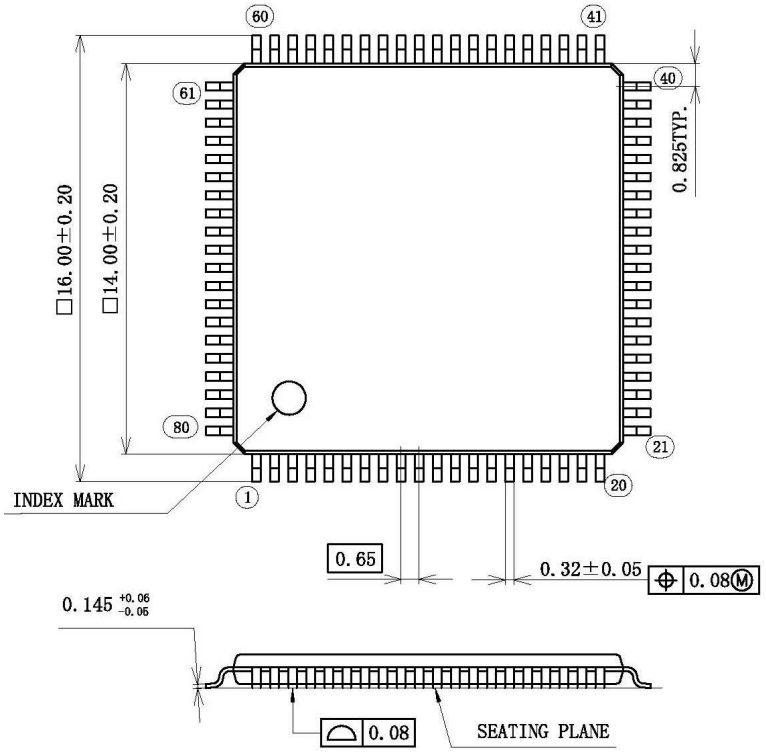


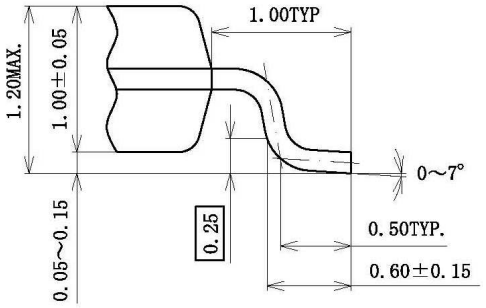
*: Indicates the secondary function of the port.

PACKAGE DIMENSIONS

(Unit: mm)

P-TQFP80-1414-0.65-TK6





LAPIS Semiconductor Co.,Ltd.

Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Sn
Solder thickness	More than 5μm
Package weight (g)	0.55typ.
Rev. No./Last Revised	1 / Dec.15,2011

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVESION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q476-01	Jan.11,2013	–	–	Final edition 1

NOTES

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