March 1990
Edition 4.0

FUJITSU

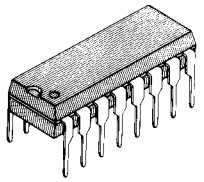
DATA SHEET

MB6041/6042/6045/6046
PCM CODEC

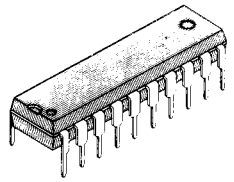
SINGLE CHIP CODEC WITH FILTERS

The Fujitsu CMOS MB 6040 Series consists of both μ-law and A-law single-chip codec/filter IC's for either synchronous-only or sync/async operation. These monolithic single-channel voice frequency codecs incorporate both transmit and receive circuitry that is used for PCM (pulse coded modulation) systems.

- Transmit High-pass and Low-pass Filters
- Receive Low-pass Filter with SinX/X Correction
- Receive Push-pull Power Amplifiers: MB 6045, MB 6046
- Anti-aliasing Filter
- Conforms to CCITT and AT & T Specifications
- Synchronous and Asynchronous Operation
- Serial Data Rates of 64kHz to 3.152 MHz
- PLL Circuit as Internal Clock Generator
- Internal Voltage Reference
- Internal Auto-zero Circuit
- TTL Compatible Digital Interface
- Input Gain Adjust Amplifier
- Pin selectable on-chip Analog Loopback
- μ-Law: MB 6041, MB 6045
  A-Law: MB 6042, MB 6046
- Package
  16-pin Plastic DIP package (Suffix: -P): MB 6041, MB 6042
  20-pin Plastic DIP package (Suffix: -P): MB 6045, MB 6046

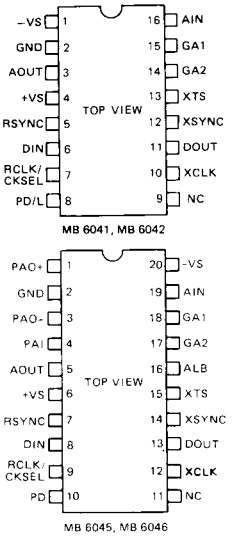


PLASTIC PACKAGE
DIP-16P-M03



PLASTIC PACKAGE
DIP-20P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Pin MB 6041 MB 6042	Pin MB 6045 MB 6046	Value Min	Value Max	Unit
Positive Supply Voltage	+VS	4	6	-0.3	7	V
Negative Supply Voltage	-VS	1	20	-7	0.3	V
Analog Input Voltage	V_{AIN}	16	19	-VS-0.3	+VS+0.3	V
Digital Input Voltage	V_{DIN1}	5, 6, 10, 12	7, 8, 10, 12, 14, 16	-0.3	+VS+0.3	V
Digital Input Voltage	V_{DIN2}	7,8	9	-VS-0.3	+VS+0.3	V
Storage Temperature	T_{STG}			-55	150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 6041, MB 6042 BLOCK DIAGRAM

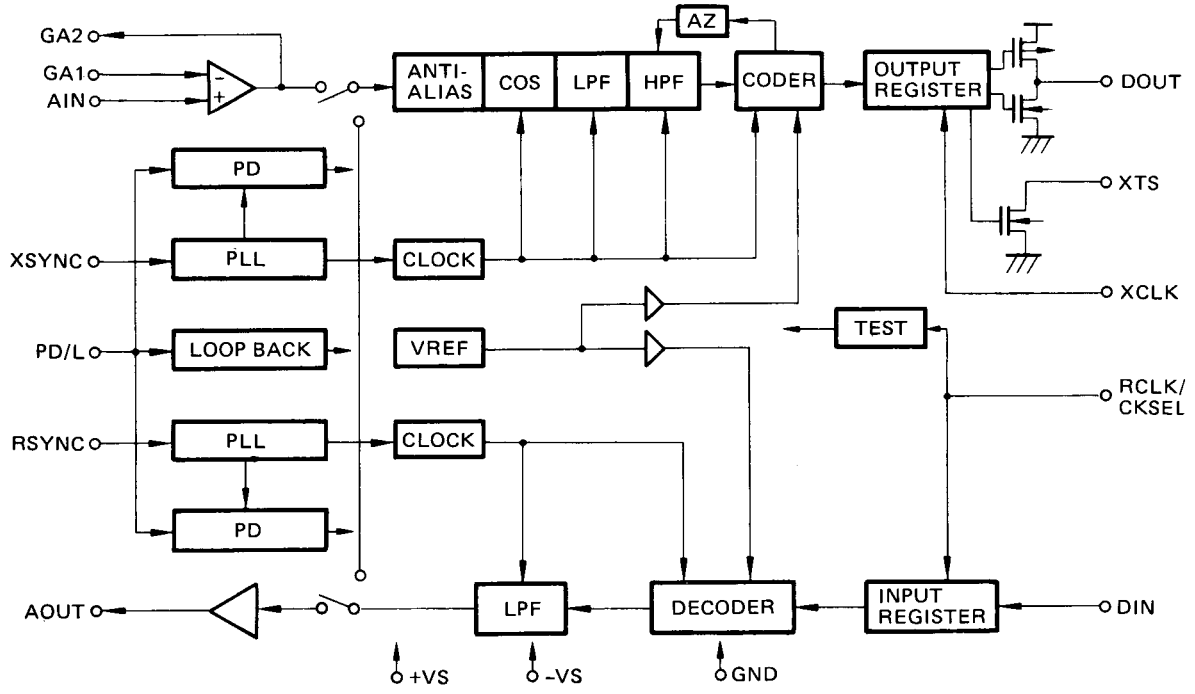
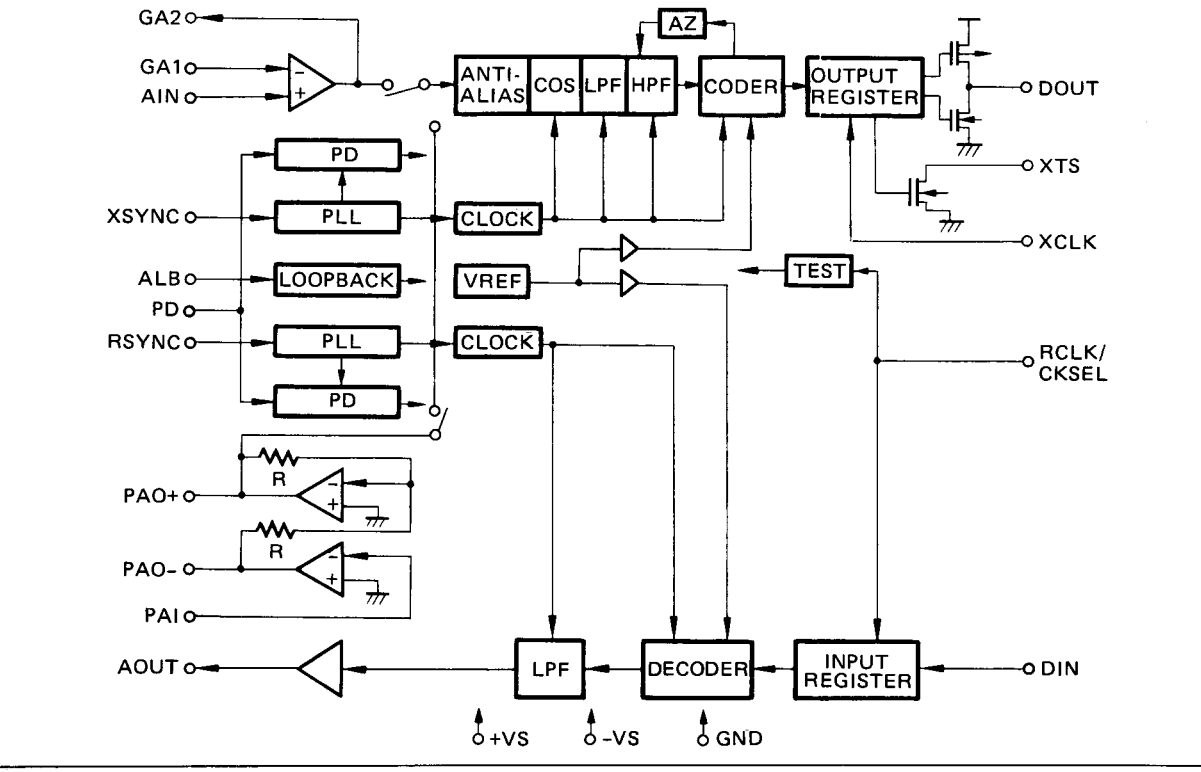


Fig. 2 – MB 6045, MB 6046 BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The simplified block diagram of the MB 6041 and MB 6042 is shown in Figure 1, and the block diagram for the MB 6045 and MB 6046 is shown in Figure 2. The transmit section (upper half) is composed of an input gain amplifier, an anti-aliasing filter (ANTI-ALIAS), a band-pass filter (COS, LPF and HPF), and a compressing coder (CODER). An auto-zero circuit (AZ) is also included in this section. The receive section (lower half) is composed of an expanding decoder (DECODER) and a low-pass filter (LPF).

TRANSMIT SECTION

Analog signals are input to an operational amplifier to provide gain adjustment. This amplifier is followed by a 2nd order analog anti-aliasing filter (ANTI-ALIAS). This filter provides attenuation of 40 dB (typical) at the 256 kHz effective clock frequency of the following switched capacitor cosine filter (COS). From the cosine filter, the signals enter a 5th order low-pass filter (LPF) clocked at 128 kHz, followed by a 3rd order high-pass filter (HPF) clocked at 8 kHz. The resulting band-pass characteristics meet both the D3/D4 specification and the CCITT G.712 recommendation. The output of the high-pass filter is then sampled by the coder (CODEC) a 8 kHz. This coder transforms the analog signals into 8-bit words using compressing law. The encoded PCM data is then output serially from the OUTPUT REGISTER at a frequency determined by the external clock, 64 kHz to 3.152 MHz. An auto-zero circuit (AZ) is utilized for the DC offset correction.

RECEIVE SECTION

The PCM data is shifted in by the receive (RCLK/CKSEL), which can vary from 64 kHz to 3.152 MHz. The decoder (DECODER) reconstructs the analog signals from the PCM data using expanding law. The decoder is followed by a 5th order low pass filter (LPF). This filter smooths the decoded signals and corrects them for the SinX/X attenuation due to the 8 kHz sampling and holding operation.

As for MB 6045 and MB 6046, two inverting mode power amplifiers are provided to firectly drive a match line interface transformer.

INTERNAL CLOCK

Two independent phase locked loops (PLL) generate internal clocks for the transmit and receive sections from the respective synchronization clocks (XSYNC and RSYNC).

ANALOG LOOPBACK MODE

(MB 6041, MB 6042)

The analog loopback mode allows all decoding and coding functions to be exercised without using the analog input (AIN) and analog output (AOUT). In this mode, a digital input signal is decoded and internally routed to the transmit filters.

The output is available from the digital output (DOUT). The analog output (AOUT) is forced to the ground (GND) level. The analog loopback mode is selected by connecting the PD/L input to the negative supply voltage (−VS).

(MB 6045, MB 6046)

The analog loopback mode allows all decoding and coding functions to be exercised without using the analog input (AIN) and analog output (AOUT). In this mode, a digital input signal is decoded and the PAO+ output of the receive power amplifier is internally routed to the transmit filters. The output is available from the digital output (DOUT). The analog output (AOUT) is forced to the ground (GND) level. The analog loopback mode is selected by connecting the ALB input to the TTL high level.

SYNCHRONOUS OPERATION

With a fixed level on the RCLK/CKSEL pin, the device operate in the a synchronous mode. In this mode, both the transmit and receive bits are synchronous to the XCLK. The XCLK may be from 64 kHz to 3.152 MHz.

ASYNCHRONOUS OPERATION

For asynchronous operation, XCLK and RCLK/CKSEL may operate from 64 kHz to 3.152 MHz for bit clock.

SHORT/LONG FRAME SYNC OPERATION

They can utilize either short frame sync pulse or a long frame sync pulse. When power is first applied, the device assumes a short frame sync mode. In this mode, both frame sync pulses, XSYNC and RSYNC, must be one bit clock period long. To use the long frame sync mode, both the synchronization clocks must be three or more bit clock periods long.

POWER DOWN MODE

(MB 6041, MB 6042)

Two power down modes are provided. The transmit and receive sections independently go into power down operation in the absense of the respective synchronization clocks (XSYNC and RSYNC). If the external power down input

(PD/L) is connected to a TTL high level, both the transmit and receive section are powerd down regardless of the synchronization clocks. During power down operation, AOUT is forced to the level of GND, and DOUT goes into a high impedance state. When Power is first applied, the device is in powered down mode operation. If external pin conditions are not powered down mode (PD/L is not connected to TTL high level and synchronization clock is applied), the device goes into a normal operation after PLL circuit is locked.

(MB 6045, MB 6046)

Two power down modes are provided. The transmit and receive sections independently go into power down operation in the absense of the respective synchronization clocks (XSYNC and RSYNC). If the external power down input (PD) is connected to a TTL high level, both the transmit and receive sections are powerd down regardless of the synchronization clocks. During power down operation, the AOUT, PAO+, PAO- is forced to GND level and DOUT is put in high-impedance state. When power is first applied, the device is in powered down mode operation. If external pin conditions are not powered down mode (PD is not connected to TTL high level and synchronization clock is applied), the device goes into a normal operation after PLL circuit is locked.

TEST MODE

If RCLK/CKSEL pin is connected to – VS, test mode allows independent evaluation of the coder and decoder. In this mode, AIN is internally connected to the input of the coder and its output is available on the DOUT pin. Also, the output of the decoder is made available in on pin AOUT.

PIN DESCRIPTION

MB 6041, MB 6042		MB 6045, MB 6046		Description
Pin Name	Pin No.	Pin Name	Pin No.	
-VS	1	–	–	Negative Voltage Supply, -5 V ±5%
–	–	PAO+	1	Non-inverting Power Amplifier Output This pin is the non-inverted output of the receive power amplifier.
GND	2	GND	2	Ground All signals are referenced to this pin.
AOUT	3	–	–	Analog Output This pin outputs the decoded and filtered analog signals. It can drive a load impedance of 600 Ω or greater, and 50 pF or less. This output is forced to GND level in the analog loopback mode and power down mode.
–	–	PAO-	3	Inverting Power Amplifier Output This pin is the inverted output of the receive power amplifier.
+VS	4	–	–	Positive Voltage Supply, +5 V ±5%
–	–	PAI	4	Power Amplifier Input This pin is the inverting input to the receive power amplifier. If this pin is connected to -VS, both of the receive power amplifiers are powered down.
RSYNC	5	–	–	Receive Synchronization Clock This TTL compatible input defines the beginning of the receive timeslot on the receive PCM highway. It must be synchronized with RCLK. The clock rate is typically 8 kHz. Its high pulse width must be one bit clock period long corresponds to short frame sync operation and three or more bit clock period long corresponds to long frame sync operation, respectively.
–	–	AOUT	5	Analog Output This pin outputs the decoded and filtered analog signals. It can drive a load impedance of 10 kΩ or greater, and 50 pF or less. This output is put in the ground in the analog loopback mode and the power down mode.
DIN	6	–	–	Digital Input This is a TTL compatible input to the decoder and accepts an eight-bit data word into the shift register on the falling edge of RCLK/CKSEL.
–	–	+VS	6	Positive Voltage Supply, +5 V ±5%
RCLK/ CKSEL	7	–	–	Receive Clock This TTL compatible input defines the bit rate on the receive PCM highway. The device can operate with clock rates of 64 kHz to 3.152 MHz. The digital PCM codes are accepted on the falling edge of the clock. With a fixed level of 0 V or +VS (or left open), the device operate in synchronous mode. If this pin is connected to -VS, test mode is selected.
–	–	RSYNC	7	Receive Synchronization Clock This TTL compatible input defines the beginning of the receive timeslot on the receive PCM highway. It must be synchronized with RCLK. The clock rate is typically 8 kHz. Its high pulse width must be one bit clock period long corresponding to the short frame sync operation and three or more bits clock period long corresponding to the long frame sync operation, respectively.

PIN DESCRIPTION(Cont'd)

MB 6041, MB 6042		MB 6045, MB 6046		Description
Pin Name	Pin No.	Pin Name	Pin No.	
PD/L	8	–	–	Power Down/Analog Loopback This three level input is provided for the selection of power down mode or analog loopback mode. If this pin is at the TTL low level or clock mode input (64 kHz min.), the normal operation is selected. If this pin is at the TTL high level, the device is powered down regardless of the synchronization clocks. If this pin is connected to -VS, the analog loopback mode is selected.
–	–	DIN	8	Digital Input This is a TTL compatible input to the decoder and accepts an eight-bit data word into the shift register on the falling edge of RCLK/CKSEL.
NC	9	–	–	No internal connection
–	–	RCLK/ CKSEL	9	Receive Clock This TTL compatible input defines the bit rate on the receive PCM highway. The device can operate with clock rates of 64 kHz to 3.152 MHz. The digital PCM codes are accepted on the falling edge of the clock. With a fixed level of 0 V or +VS (or left open), the device operates in synchronous mode, where the XCLK is used for both the transmit and receive operations. If this pin is connected to -VS, test mode is selected.
XCLK	10	–	–	Transmit Clock This TTL compatible input defines the bit rate on the transmit PCM highway. The device can operate with bit rates of 64 kHz to 3.152 MHz. The digital PCM codes are shifted out of the digital output (DOUT) pin on the rising edge of the XCLK. In synchronous operation, XCLK is used as the bit clock for the transmit and receive sections.
–	–	PD	10	Power Down This TTL compatible input is provided for the selection of power down mode. If this pin is at the TTL low level or clock mode input (64 kHz min.), the normal operation is selected. If this pin is at the TTL high level, the device is powered down regardless of the synchronization clocks.
DOUT	11	–	–	Digital Output This is a TTL compatible three-state output. PCM digital codes are shifted out of the device on the rising edges of XCLK in a serial format. This output goes into high-impedance state when eight bits are shifted out of the output shift register.
–	–	NC	11	No internal connection
XSYNC	12	–	–	Transmit Synchronization Clock This TTL compatible input defines the beginning of the transmit timeslot on the transmit PCM highway. It must be synchronized with XCLK. The clock rate is typically 8 kHz. Its high pulse width must be one bit clock period long corresponds to short frame sync operation and three or more bit clock periods long frame sync operation, respectively.

PIN DESCRIPTION (Cont'd)

MB 6041, MB 6042		MB 6045, MB 6046		Description
Pin Name	Pin No.	Pin Name	Pin No.	
–	–	XCLK	12	Transmit Clock This TTL compatible input defines the bit rate on the transmit PCM highway. The device can operate with bit rate of 64 kHz to 3.152 MHz. The digital PCM codes are shifted out of the digital output (DOUT) pin on the rising edge of the XCLK. In synchronous operation, XCLK is used as the bit clock for the transmit and receive sections.
XTS	13	–	–	Transmit Timeslot Strobe This is a TTL compatible open-drain output which pulse is low level during PCM transmit timeslots.
–	–	DOUT	13	Digital Output This is a TTL compatible three-state output. PCM digital codes are shifted out of the device on the rising edges of XCLK in a serial format. This output goes into high-impedance state when eight bits are shifted out of the output shift register.
GA2 GA1	14 15	–	–	Gain Adjust 2 Gain Adjust 1 These pins are provided for adjusting the gain of transmit section. GA1 and GA2 are the inverting input and output of amplifier, respectively. GA2 can drive a load impedance of 10 kΩ or more and 50 pF or less.
–	–	XSYNC	14	Transmit Synchronization Clock This TTL compatible input defines the beginning of the transmit timeslot on the transmit PCM highway. It must be synchronized with XCLK. The clock rate is typically 8 kHz. Its high pulse width must be one bit clock period long corresponds to short frame sync operation and three or more bits clock period long corresponding to the long frame sync operation, respectively.
–	–	XTS	15	Transmit Timeslot Strobe This is a TTL compatible open-drain output which pulses the low level during PCM transmit timeslots.
AIN	16	–	–	Analog Input This is an input pin for analog signals to be filtered and coded.
–	–	ALB	16	Analog Loopback This TTL compatible input is provided for the selection of the analog loopback mode. If this pin is at the TTL low level, the normal operation is selected. If this pin is at the TTL high level, the analog loopback mode is selected.
–	–	GA2 GA1	17 18	Gain Adjust 2 Gain Adjust 1 These pins are provided for adjusting the gain of transmit section. GA1 and GA2 are the inverting input and output of amplifier, respectively. GA2 can drive a load impedance of 10 to 20 kΩ or 50 pF or less.
–	–	AIN	19	Analog Input This is an input pin for analog signals to be filtered and coded.
–	–	-VS	20	Negative Voltage Supply, -5 V ±5%

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin MB 6041 MB 6042	Pin MB 6045 MB 6046	Symbol	Value			Unit
				Min	Typ	Max	
Positive Supply Voltage	4	6	+VS	+4.75	+5.0	+5.25	V
Negative Supply Voltage	1	20	-VS	-5.25	-5.0	-4.75	V
Operating Temperature			T_{OP}	0	25	70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Pin MB 6041/42	Pin MB6045/46	Symbol	Value			Unit
					Min	Typ	Max	
Positive Supply Current	Operating	4		$+I_{VS}$		8.0	12.0	mA
			6			10.0	14.0	
Negative Supply Current	Operating	1		$-I_{VS}$	-10.0	-5.0		mA
			20		-12.0	-8.0		
Positive Supply Current Power Down Mode	XSYNC=RSYNC=VIL or PD/L=VIH	4	6	$+I_{VSST}$		1.0	2.0	mA
Negative Supply Current Power Down Mode	XSYNC=RSYNC=VIL or PD/L=VIH	1	20	$-I_{VSST}$	-0.5	-0.1		mA
Digital Input High Voltage		5, 6, 7, 8, 10, 12	7, 8, 9, 10, 12, 14, 16	V_{IH}	2.0		+VS	V
Digital Input Low Voltage		5, 6, 7, 8, 10, 12	7, 8, 9, 10, 12, 14, 16	V_{IL}	0		0.8	V
Digital Input High Current		5, 6, 7, 8, 10, 12	7, 8, 9, 10, 12, 14, 16	I_{IH}	-10		10	μA
Digital Input Low Current		5, 6, 7, 8, 10, 12	7, 8, 9, 10, 12, 14, 16	I_{IL}	-10		10	μA
Digital Input Capacitance		5, 6, 7, 8, 10, 12	7, 8, 9, 10, 12, 14, 16	C_{DIN}			10	pF
Digital Output Low Voltage	I_{OL} = 3.2 mA	11, 13	13, 15	V_{OL}			0.4	V
Digital Output High Voltage	I_{OH} = -3.2 mA	11	13	V_{OH}	2.4			V
Digital Output Leakage Current		11	13	I_{LO}	-10		10	μA

DC CHARACTERISTICS(Cont'd)

Parameter	Conditions	Pin MB 6041/42	Pin MB6045/46	Symbol	Value			Unit
					Min	Typ	Max	
Digital Output Capacitance		11	13	C_{DOUT}			12	pF
Analog Input Offset Voltage		16	19	A_{INOFF}	-200	0	200	mV
Analog Input Resistance		16	19	R_{AIN}	10			MΩ
Analog Input Capacitance		16	19	C_{AIN}			10	pF
Analog Output Offset Voltage		3	5	A_{OUTOFF}	-150		150	mV
Analog Output Resistance		3	–	R_{AOUT}		1		Ω
Power Amplifier Output Resistance		–	1, 3	R_{PAO}		1		Ω
Transmit Gain Amplifier Load Resistance		14	17	R_{LGA2}	10			kΩ
Transmit Gain Amplifier Load Capacitance		14	17	C_{LGA2}			50	pF
Analog Output Load Resistance		3		R_{LAOUT}	0.6			kΩ
			5		10			
Analog Output Load Capacitance		3		C_{LAOUT}			500	pF
			5				50	
Power Amplifier Input Resistance		–	4	R_{PAI}	10			MΩ
Power Amplifier Load Capacitance	RL ≧ 1500 Ω	–	1, 3	C_{LPAO}			100	pF
	RL = 600 Ω						500	
	RL = 300 Ω						1000	
Power Amplifier Load Resistance		–	1, 3	R_{LPAO}	0.3			kΩ

AC CHARACTERISTICS(MB 6041, MB 6042)

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Pin	Symbol	Value			Unit
				Min	Typ	Max	
Digital Input Rise Time	0.8V → 2.0V	5, 6, 7, 8, 10, 12	t_r			50	ns
Digital Input Fall Time	2.0V → 0.8V	5, 6, 7, 8, 10, 12	t_f			50	ns
Shift Clock Frequency		7, 10	F_c	64		3152	kHz
Shift Clock High Width	V_{IH} = 2.0V	7, 10	t_{WCH}	160			ns
Shift Clock Low Width	V_{IL} = 0.8V	7, 10	t_{WCL}	160			ns
Synchronization Frequency		5, 12	F_s		8		kHz
Synchronization High Width	Long frame only V_{IH} = 2.0V	5, 12	t_{WSH}			117	μs
XSYNC to XCLK Delay	Long frame only	10, 12	t_{SXL}	80			ns
XCLK to XSYNC Delay	Long frame only	10, 12	t_{XSL}	0			ns
RSYNC to RCLK Delay	Long frame only	5, 7	t_{SRL}	80			ns
RCLK to RSYNC Delay	Long frame only	5, 7	t_{RSL}	70			ns
RCLK to DIN Delay		6, 7	t_{RD}	140			ns
DIN to RCLK Delay		6, 7	t_{DR}	50			ns
XCLK to DOUT Delay	Note 1 Bit 2 to 8 (Long frame) Bit 1 to 8 (Short frame)	10, 11	t_{XD}	0		180	ns
XCLK to DOUT Disable Time	Note 1	10, 11	t_{DZ}	50		165	ns
XCLK or XSYNC to DOUT Delay	Note 1 Long frame only Bit 1	10, 11, 12	t_{ZD}	20		165	ns
Hold time from 3rd XCLK to XSYNC	Long frame only	10, 12	t_{XHL}	100			ns
Hold time from 3rd RCLK to RSYNC	Long frame only	5, 7	t_{RHL}	130			ns

Note 1: DOUT Load Conditions: C_{DL} = 150 pF plus 2 LSTTL

AC CHARACTERISTICS(MB 6041, MB 6042)(Cont'd)

Parameter	Conditions	Pin	Symbol	Value			Unit
				Min	Typ	Max	
XCLK to XSYNC Delay	Short frame only	10, 12	t_{XSS}	0			ns
XSYNC to XCLK Delay	Short frame only	10, 12	t_{SXS}	50			ns
Hold time from XCLK to XSYNC	Short frame only	10, 12	t_{XHS}	100			ns
RCLK to RSYNC Delay	Short frame only	5, 7	t_{RSS}	0			ns
RSYNC to RCLK Delay	Short frame only	5, 7	t_{SRS}	50			ns
Hold time from RCLK to RSYNC	Short frame only	5, 7	t_{RHS}	100			ns
XCLK to XTS Low Delay	Note 1	10, 13	t_{XTSL}			140	ns
XCLK to XTS High Delay	Note 1	10, 13	t_{XTSH}	50		165	ns

Note 1: DOUT Load Conditions: C_{DL} = 150 pF plus 2 LSTTL

AC CHARACTERISTICS(MB 6045, MB 6046)

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Pin	Symbol	Value			Unit
				Min	Typ	Max	
Digital Input Rise Time	0.8V → 2.0V	7, 8, 9, 10, 12, 14, 16	t_r			50	ns
Digital Input Fall Time	2.0V → 0.8V	7, 8, 9, 10, 12, 14, 16	t_f			50	ns
Shift Clock Frequency		9, 12	F_c	64		3152	kHz
Shift Clock High Width	V_{IH} = 2.0V	9, 12	t_{WCH}	160			ns
Shift Clock Low Width	V_{IL} = 0.8V	9, 12	t_{WCL}	160			ns
Synchronization Frequency		7, 14	F_s		8		kHz
Synchronization High Width	Long frame only V_{IH} = 2.0V	7, 14	t_{WSH}			117	μs
XSYNC to XCLK Delay	Long frame only	12, 14	t_{SXL}	80			ns

AC CHARACTERISTICS(MB 6045, MB 6046)(Cont'd)

Parameter	Conditions	Pin	Symbol	Value			Unit
				Min	Typ	Max	
XCLK to XSYNC Delay	Long frame only	12, 14	t_{XSL}	0			ns
RSYNC to RCLK Delay	Long frame only	7, 9	t_{SRL}	80			ns
RCLK to RSYNC Delay	Long frame only	7, 9	t_{RSL}	70			ns
RCLK to DIN Delay		8, 9	t_{RD}	140			ns
DIN to RCLK Delay		8, 9	t_{DR}	50			ns
XCLK to DOUT Delay	Note 2 Bit 2 to 8 (Long frame) Bit 1 to 8 (Short frame)	12, 13	t_{XD}	0		180	ns
XCLK to DOUT Disable Time	Note 2	12, 13	t_{DZ}	50		165	ns
XCLK or XSYNC to DOUT Delay	Note 2 Long frame only Bit 1	12, 13, 14	t_{ZD}	20		165	ns
Hold time from 3rd XCLK to XSYNC	Long frame only	12, 14	t_{XHL}	100			ns
Hold time from 3rd RCLK to RSYNC	Long frame only	7, 9	t_{RHL}	130			ns
XCLK to XSYNC Delay	Short frame only	12, 14	t_{XSS}	0			ns
XSYNC to XCLK Delay	Short frame only	12, 14	t_{SXS}	50			ns
Hold time from XCLK to XSYNC	Short frame only	12, 14	t_{XHS}	100			ns
RCLK to RSYNC Delay	Short frame only	7, 9	t_{RSS}	0			ns
RSYNC to RCLK Delay	Short frame only	7, 9	t_{SRS}	50			ns
Hold time from RCLK to RSYNC	Short frame only	7, 9	t_{RHS}	100			ns
XCLK to XTS Low Delay	Note 2	12, 15	t_{XTSL}			140	ns
XCLK to XTS High Delay	Note 2	12, 15	t_{XTSH}	50		165	ns

Note 2: DOUT Load Conditions: C_{DL} = 150 pF plus 2 LSTTL

Fig. 3 — TIMING DIAGRAM (Long frame Sync Mode)

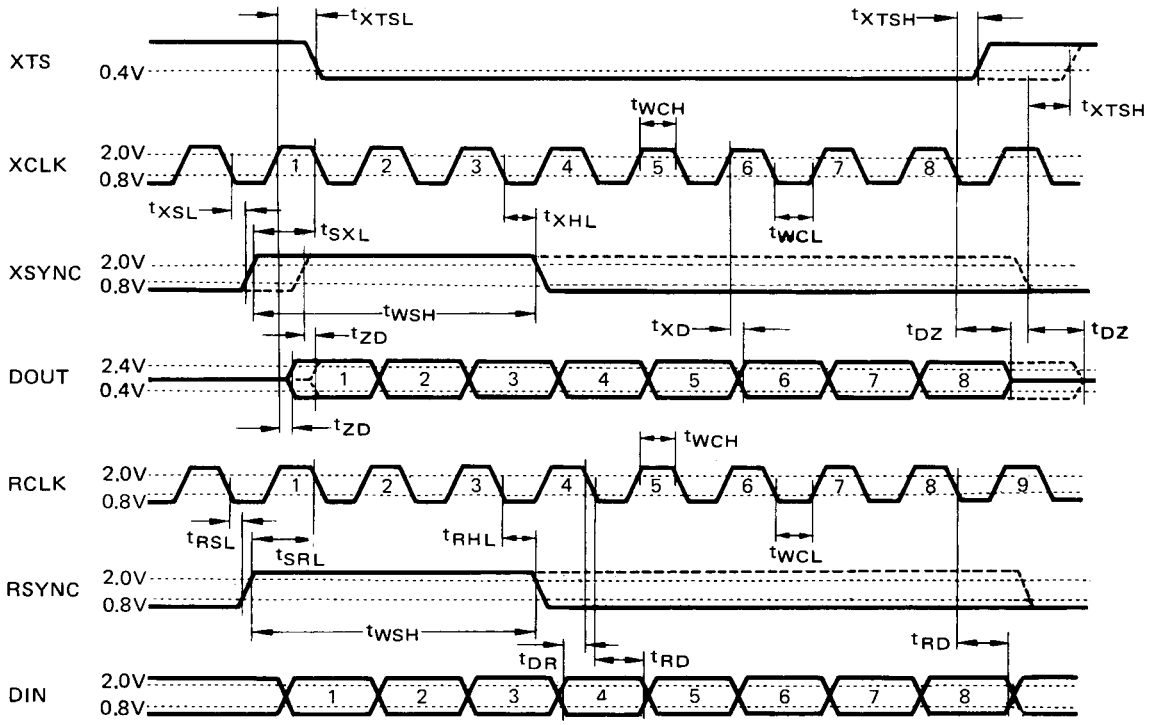
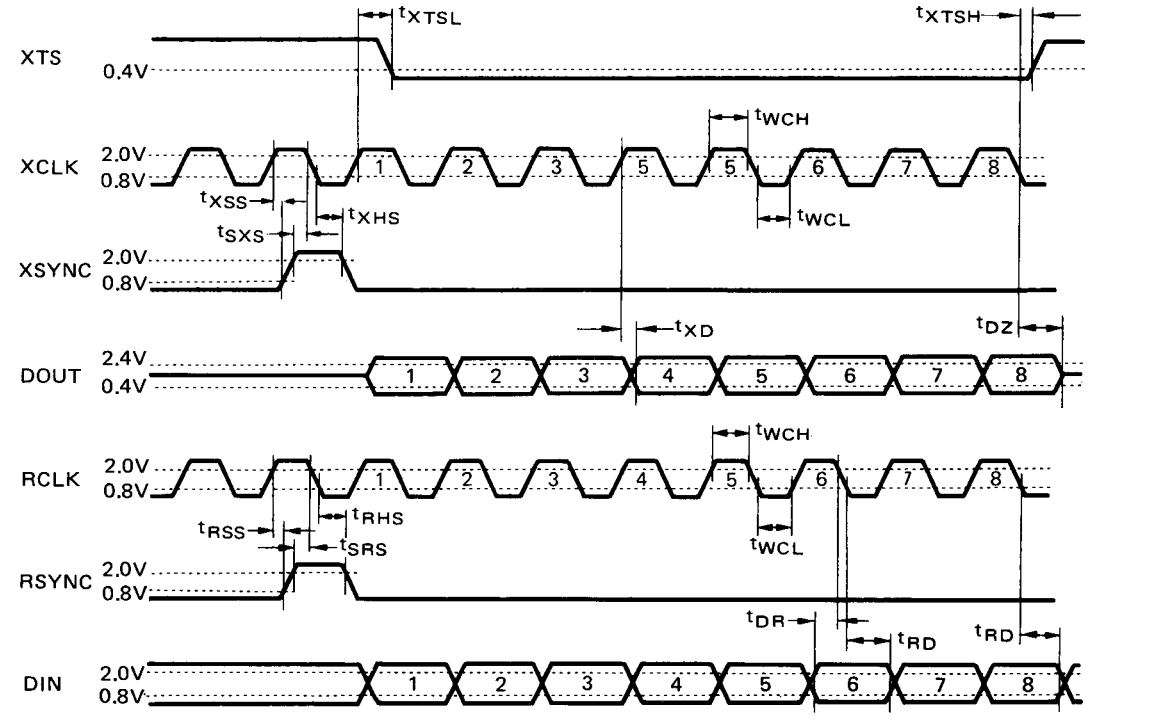


Fig. 4 — TIMING DIAGRAM (Short frame Sync Mode)



TRANSMISSION CHARACTERISTICS OF μ-LAW (MB 6041, MB 6045)

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions		Symbol	Value			Unit
				Min	Typ	Max	
Signal to Distortion (A to D)	1020Hz tone (C Message)	+3 to -30dBm0 -40dBm0 -45dBm0	SDX	36.0 31.0 26.0			dB dB dB
Signal to Distortion (D to A)	1020Hz tone (C Message)	+3 to -30dBm0 -40dBm0 -45dBm0	SDR	36.0 31.0 26.0			dB dB dB
Gain Tracking (A to D)	1020Hz tone	+3 to -40dBm0 -40 to -50dBm0 -50 to -55dBm0	GTX	-0.2 -0.4 -0.8		0.2 0.4 0.8	dB dB dB
Gain Tracking (D to A)	1020Hz tone	+3 to -40dBm0 -40 to -50dBm0 -50 to -55dBm0	GTR	-0.2 -0.4 -0.8		0.2 0.4 0.8	dB dB dB
Frequency Response (A to D)	0 – 60Hz 60 – 200Hz 200 – 300Hz 300 – 3000Hz 3000 – 3400Hz 3400 – 4600Hz 4.6 – 12 kHz Relative to 0dBm0, 820Hz		FRX	25.0 0.125 -0.1 -0.1 -0.1 Note 3 32.0		 1.8 0.15 0.8	dB dB dB dB dB dB dB
Frequency Response (D to A)	0 – 200Hz 200 – 300Hz 300 – 3000Hz 3000 – 3400Hz 3400 – 4600Hz 4.6 – 12KHz Relative to 0dBm0, 820Hz		FRR	-0.1 -0.1 -0.1 -0.1 Note 3 32.0		 0.5 0.15 0.8	dB dB dB dB dB dB
Idle Channel Noise (A to A)	C Message		ICNA		-80	-72.0	dBm0c
Idle Channel Noise (A to D)	C Message		ICNX		-83	-74.0	dBm0c
Idle Channel Noise (D to A)	C Message		ICNR		-83	-78.0	dBm0c
Crosstalk (A to A)	1020Hz, 0dBm0		CTA			-66	dB
Crosstalk (D to D)	1020Hz, 0dBm0		CTD			-70	dB
Absolute Level	Overload level 3.17dBm0		VABS		2.500		Vop
Analog Input Level	1020Hz, 0dBm0 ±VS = ±5.0V, T_A = 25°C		AIL		1.227		Vrms
Analog Output Level	1020Hz, 0dBm0 ±VS = ±5.0V, T_A = 25°C		AOL	1.206	1.227	1.248	Vrms

Note 3: $14.5\ (1 - \mathrm{Sin}\ \frac{\pi(4000 - f)}{1200})$

TRANSMISSION CHARACTERISTICS OF μ-LAW (MB 6041, MB6045) (Cont'd)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Gain Accuracy (A to D)	1020Hz, 0dBm0 ±VS = ±5.0V, T_A = 25°C Variation with Power Supply Variation with Temperature	GAX	-0.25 -0.15	0 0 ±0.02 ±0.001	+0.25 +0.15	dB dB dB dB/°C
Gain Accuracy (D to A)	1020Hz, 0dBm0 ±VS = ±5.0V, T_A = 25°C Variation with Power Supply Variation with Temperature	GAR	-0.25 -0.15	0 0 ±0.02 ±0.001	+0.25 +0.15	dB dB dB dB/°C
Propagation Delay (A to A)	FC ≧ 1544kHz	PDA			540	μs
Delay to Distortion (A to A)	500 – 600Hz 600 – 1000Hz 1000 – 2600Hz 2600 – 2800Hz 1020Hz, 0dBm0 Relative to Minimum Delay	DDA			1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	0 < f ≦ 50kHz Idle Channel Noise (C Message) +VS +50mVop AIN = GND	PSRRA+	25	30		dB
RSRR (-VS) (A to A)	0 < f ≦ 50kHz Idle Channel Noise (C Message) -VS +50mVop AIN = GND	PSRRA-	35	40		dB
Intermoduration (A to A)	AIN a. 0.47kHz, -10dBm0 b. 0.32kHz, -10dBm0 AOUT (2a–b)	IMA1			-38	dB
Intermoduration (A to A)	AIN a. 1.02kHz, -9dBm0 b. 0.05kHz, -23dBm0 AOUT (a–b)	IMA2			-52	dBm0

TRANSMISSION CHARACTERISTICS OF μ-LAW (MB 6041, MB 6045) (Cont'd)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Signal Frequency Noise (A to A)	0 – 4kHz 4kHz – 200kHz AIN = GND	SFNA			-70 -50	dBm0 dBm0
Discrimination (A to A)	AIN = 0dBm0 4.6kHz – 200kHz	DISA	30			dB
In Band Spurious (A to A)	2nd, 3rd Harmonic AIN = 0dBm0, 700 – 1100Hz	IBSA	43			dB

TRANSMISSION CHARACTERISTICS OF A-LAW (MB 6042, MB 6046)

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions		Symbol	Value			Unit
				Min	Typ	Max	
Signal to Distortion (A to D)	CCITT G.712 Method 2 1020Hz tone (P Message)	+3 to -30dBm0 -40dBm0 -45dBm0	SDX	36.0 31.0 26.0			dB dB dB
	CCITT G.712 Method 1	-3dBm0 -6 to -27dBm0 -34dBm0 -40dBm0 -55dBm0		30.0 36.0 34.0 29.5 14.5			dB dB dB dB dB
Signal to Distortion (D to A)	CCITT G.712 Method 2 1020Hz tone (P Message)	+3 to -30dBm0 -40dBm0 -45dBm0	SDR	36.0 31.0 26.0			dB dB dB
	CCITT G.712 Method 1	-3dBm0 -6 to -27dBm0 -34dBm0 -40dBm0 -55dBm0		30.0 36.0 34.0 29.5 14.5			dB dB dB dB dB
Gain Tracking (A to D)	CCITT G.712 Method 2 1020Hz tone	+3 to -40dBm0 -40 to -50dBm0 -50 to -55dBm0	GTX	-0.2 -0.4 -0.8		0.2 0.4 0.8	dB dB dB
	CCITT G.712 Method 1	-10 to -50dBm0 -50 to -55dBm0 -55 to -60dBm0		-0.25 -0.4 -0.8		0.25 0.4 0.8	dB dB dB
Gain Tracking (D to A)	CCITT G.712 Method 2 1020Hz tone	+3 to -40dBm0 -40 to -50dBm0 -50 to -55dBm0	GTR	-0.2 -0.4 -0.8		0.2 0.4 0.8	dB dB dB
	CCITT G.712 Method 1	-10 to -50dBm0 -50 to -55dBm0 -55 to -60dBm0		-0.25 -0.4 -0.8		0.25 0.4 0.8	dB dB dB

TRANSMISSION CHARACTERISTICS OF A-LAW (MB 6042, MB6046) (Cont'd)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Frequency Response (A to D)	0 – 60Hz 60 – 200Hz 200 – 300Hz 300 – 3000Hz 3000 – 3400Hz 3400 – 4600Hz 4.6 – 12KHz Relative to 0dBm0, 820Hz	FRX	25.0 0.125 -0.1 -0.1 -0.1 Note 4 32.0		 1.8 0.15 0.8	dB dB dB dB dB dB dB
Frequency Response (D to A)	0 – 200Hz 200 – 300Hz 300 – 3000Hz 3000 – 3400Hz 3400 – 4600Hz 4.6 – 12KHz Relative to 0dBm0, 820Hz	FRR	-0.1 -0.1 -0.1 -0.1 Note 4 32.0		 0.5 0.15 0.8	dB dB dB dB dB dB
Idle Channel Noise (A to A)	P Message	ICNA		-80	-72.0	dBm0p
Idle Channel Noise (A to D)	P Message	ICNX		-83	-74.0	dBm0p
Idle Channel Noise (D to A)	P Message	ICNR		-83	-78.0	dBm0p
Crosstalk (A to A)	1020Hz, 0dBm0	CTA			-66	dB
Crosstalk (D to D)	1020Hz, 0dBm0	CTD			-70	dB
Absolute Level	Overload level 3.14dBm0	VABS		2.500		Vop
Analog Input Level	1020Hz, 0dBm0 ±VS = ±5.0V, T_A = 25°C	AIL		1.231		Vrms
Analog Output Level	1020Hz, 0dBm0 ±VS = ±5.0V, T_A = 25°C	AOL	1.210	1.231	1.252	Vrms
Gain Accuracy (A to D)	1020Hz, 0dBm0 ±VS = ±5.0V, T_A = 25°C Variation with Power Supply Variation with Temperature	GAX	-0.25 -0.15	0 0 ±0.02 ±0.001	+0.25 +0.15	dB dB dB dB/°C
Gain Accuracy (D to A)	1020Hz, 0dBm0 ±VS = ±5.0V, T_A = 25°C Variation with Power Supply Variation with Temperature	GAR	-0.25 -0.15	0 0 ±0.02 ±0.001	+0.25 +0.15	dB dB dB dB/°C

Note 4: $14.5\ (1 - \mathrm{Sin}\ \frac{\pi(4000 - f)}{1200})$

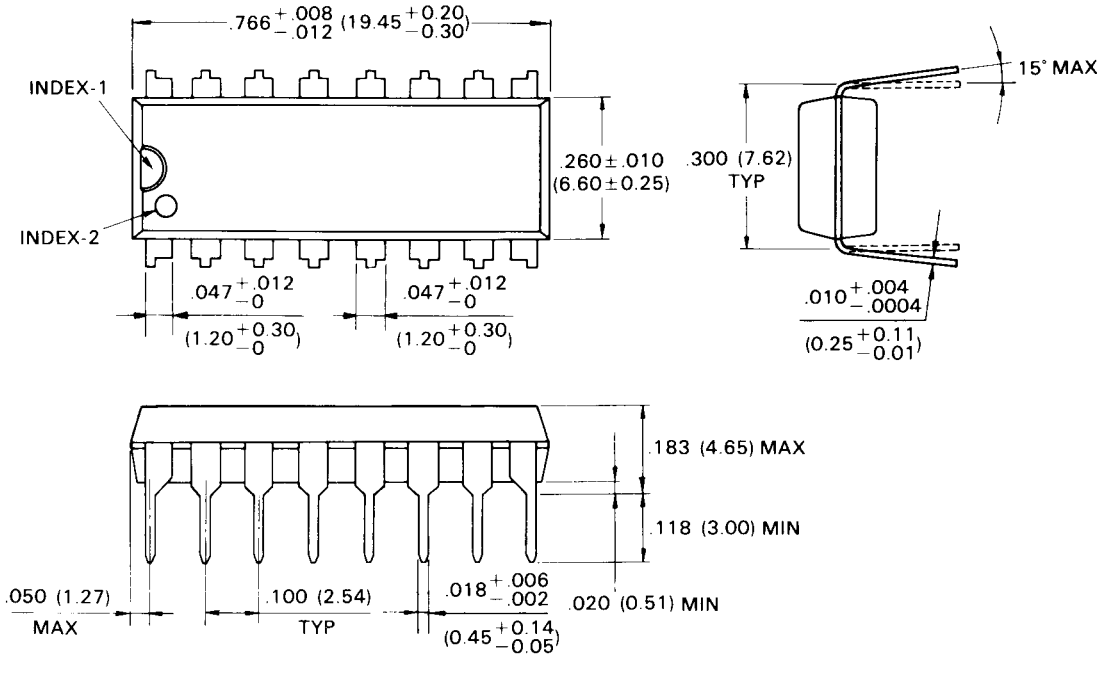
TRANSMISSION CHARACTERISTICS OF A-LAW (MB 6042, MB 6046) (Cont'd)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Propagation Delay (A to A)	FC ≧ 1544kHz	PDA			540	μs
Delay to Distortion (A to A)	500 – 600Hz 600 – 1000Hz 1000 – 2600Hz 2600 – 2800Hz 1020Hz, 0dBm0 Relative to Minimum Delay	DDA			1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	0 < f ≦ 50kHz Idle Channel Noise (P Message) +VS +50mVop AIN = GND	PSRRA+	25	30		dB
RSRR (-VS) (A to A)	0 < f ≦ 50kHz Idle Channel Noise (P Message) -VS +50mVop AIN = GND	PSRRA-	35	40		dB
Intermoduration (A to A)	AIN a. 0.47kHz, -10dBm0 b. 0.32kHz, -10dBm0 AOUT (2a–b)	IMA1			-38	dB
Intermoduration (A to A)	AIN a. 1.02kHz, -9dBm0 b. 0.05kHz, -23dBm0 AOUT (a–b)	IMA2			-52	dBm0
Single Frequency Noise (A to A)	0 – 4kHz 4kHz – 200kHz AIN = GND	SFNA			-70 -50	dBm0 dBm0
Discrimination (A to A)	AIN = 0dBm0 4.6kHz – 200kHz	DISA	30			dB
In Band Spurious (A to A)	2nd, 3rd Harmonic AIN = 0dBm0, 700 – 1100Hz	IBSA	43			dB

PACKAGE DIMENSIONS OF MB6041, MB6042

PLASTIC DIP (Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)

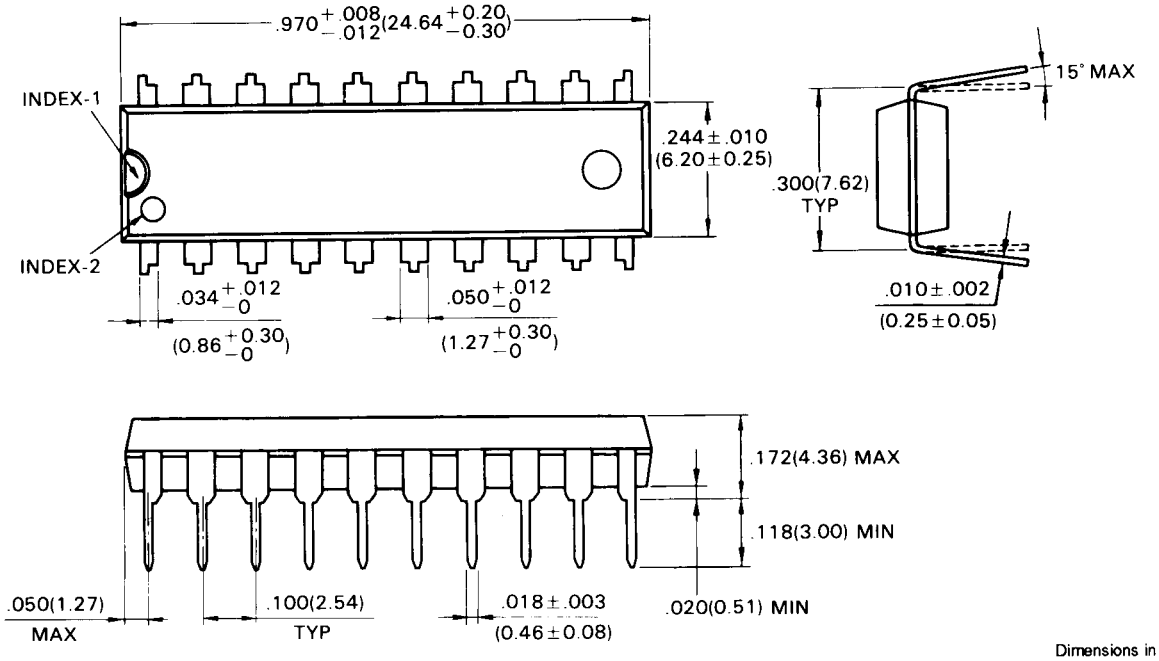


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS OF MB6045, MB6046

PLASTIC DIP (Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)



Dimensions in inches (millimeters)

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg., 6–1, Marunouchi 2–chome
Chiyoda–ku, Tokyo 100, Japan
Tel: (03) 216–3211
Telex: 781–2224361
FAX: (03) 216–9771

North and South America
FUJITSU MICROELECTRONICS, INC.
Integrated Circuits Division
3545 North First Street
San Jose, CA 95134–1804 USA
Tel: 408–922–9000
Telex: 910–338–0190
FAX: 408–432–9044

Europe
FUJITSU MIKROELEKTRONIK GmbH
Arabella Centre 9. OG
Lyoner Strasse 44–48
D–6000 Frankfurt 71
F.R. Germany
Tel: (069) 66320
Telex: 411963
FAX: (069) 6632122

Asia
FUJITSU MICROELECTRONICS ASIA PTE LIMITED
#06–04 to #06–07
Plaza By The Park
No. 51 Bras Basah Road
Singapore 0719
Tel: 336–1600
Telex: 55573
FAX: 336–1609