Chapter Six
Electrical Characteristics

Absolute Maximum Stress Ratings

Symbol	Parameter	Min	Max	Unit	Test Condition
T_{STG}	Storage Temperature	-55	150	°C	-
V_{DD}	Supply Voltage	-0.5	7.0	V	-
V_{IN}	Input Voltage	V_{SS}-0.5	V_{DD}+0.5	V	-
I_{LP}	Latch-up Current	-100	100	mA	$-2V < V_{PIN} < +8V$
ESD	Electrostatic Discharge	TBD	-	V	-

Note: Conditions that exceed the Absolute Maximum limits may destroy the device. Conditions that exceed the Operating limits may cause the device to function incorrectly.

Operating Conditions

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{DD}	Supply Voltage	4.5	5.5	V	-
I_{DD}	Supply Current	-	4	mA	Static*
I_{DD}	Supply Current	-	TBD	mA	Dynamic
T_A	Ambient Temperature	0	70	°C	-
U_{JA}	Thermal Resistance, junction/ambient				
	68-pin PLCC	-	39.97	°C/W	-
	80-pin PQFP	-	50.00	°C/W	-

* *Static means all inputs are deasserted, all outputs floating, and all bidirectional pins configured as inputs.*

DC Electrical Characteristics

Inputs: A3-A0, WR/, DIFFM

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
I_{IN}	Input Leakage Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Capacitance	-	10	pF	-

Inputs: CS/, RD/, DACK/,CLK, RESET

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
V_{H}	Hysteresis	200	700	mV	-
I_{IN}	Input Leakage Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Capacitance	-	10	pF	-

Inputs: ATNI/, ACKI/, BSYI/, REQI/, RSTI/, SELI/, MSGI/, CDI/, I_O/

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
V_{H}	Hysteresis	200	700	mV	-
I_{IL}	Input Leakage Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Capacitance	-	10	pF	-

Outputs: DREQ, IGS

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -4mA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
C_{OUT}	Capacitance	-	10	pF	-

Outputs: INT/

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
C_{OUT}	Capacitance	-	10	pF	-

Outputs: RESETO

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -8mA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
C_{OUT}	Capacitance	-	10	pF	-

Outputs: ACKO/, ATNO/, REQO/, BSYO/, RSTO/, SELO/, MSGO/, CDO/, I_OO/, SDOP/, SDO7/-SDO0/

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{OL}	Output Low Voltage	-	0.5	V	I_{OL} = 48 mA
I_{OZ}	High-Z State Leakage	-10	10	µA	$0 < V_{OUT} < V_{DD}$
S_{FT}	Signal Fall Time	4	-	ns	SCSI Termination
C_{OUT}	Capacitance	-	10	pF	-

Bidirectional Pins: DB7-DB0, DBP*

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
I_{IL}	Input Low Leakage	-600	-75	µA	V_{IN} = 0
I_{IH}	Input High Leakage	0	20	µA	V_{IN} = V_{DD}
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -4mA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4 mA
C_{IO}	Capacitance	-	10	pF	-

* *DBP applies to the 53CF90B only.*

Bidirectional Pins: SDIP/, SDI7/-SDI0/

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
V_{H}	Hysteresis	200	700	mV	-
I_{IN}	Input Current	0	10	µA	0 < V_{IN} < V_{DD}
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -4mA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 4 mA
C_{IO}	Capacitance	-	10	pF	-

Bidirectional Pins: TGS*

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	-
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	-
I_{IL}	Input Low Leakage	-600	-75	µA	V_{IN} = 0
I_{IH}	Input High Leakage	0	20	µA	V_{IN} = V_{DD}
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -8mA
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8 mA
C_{IO}	Capacitance	-	10	pF	-

* *In the 53CF90A, TGS is an output signal only.*

AC Electrical Characteristics

The AC characteristics described in this section apply over the operating voltage V_{DD} equal to 5 V ± 5%, and the temperature range 0 to 70 °C. Output timing is based on simulation under worst case conditions (4.75 v, 70 °C), and worst case processing, using the termination values listed below. All timings in this specification are taken from the 10% and 90% points with respect to the specified V_{OL} and V_{OH} of the waveforms.

Pin	Termination
DREQ, TGS, IGS, RESETO SDIP/, SDI7/-SDI0/	50 pF
INT/	50 pF, 1 KΩ pullup
DB7-DB0, DBP	85 pF
RSTO/, SELO/, BSYO/, ATNO/, MSGO/, CDO/, I_OO/, REQO/, ACKO/, SDOP/, SDO7/-SDO0/	200 pF, 110 Ω pullup, 165 Ω pulldown

System Interface Timing

Clock Input

Symbol	Parameter	Min	Max	Unit	Note
t_{CP}	Clock Period (1÷ Freq)	-	-	ns	-
t_{CS}	Synchronization Latency	t_{CL}	$t_{CL} + t_{CP}$	ns	-

Symbol	Parameter (FASTCLK bit cleared)	Min	Max	Unit	Note
t_{CPA}	Clock Frequency, Async	12	25	MHz	-
t_{CPS}	Clock Frequency, Sync	20	25	MHz	-
t_{CH}	Clock High	14.58	$0.65 \cdot t_{CP}$	ns	1
t_{CL}	Clock Low	14.58	$0.65 \cdot t_{CP}$	ns	1

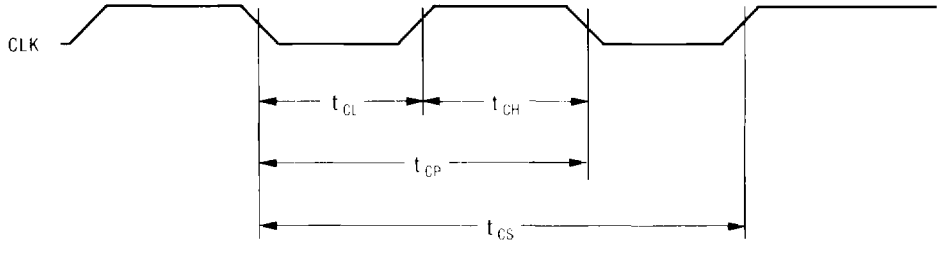
Symbol	Parameter (FASTCLK bit set)	Min	Max	Unit	Note
t_{CPA}	Clock Frequency, Async	20	40	MHz	-
t_{CPS}	Clock Frequency, Sync	38	40	MHz	-
t_{CH}	Clock High	$0.40 \cdot t_{CP}$	$0.60 \cdot t_{CP}$	ns	-
t_{CL}	Clock Low	$0.40 \cdot t_{CP}$	$0.60 \cdot t_{CP}$	ns	-

1 *For synchronous SCSI transfers and FASTCLK disabled, the clock must meet the following requirements:*

$2 \cdot t_{CP} + t_{CL} \geq 97.92$ *ns*

$2 \cdot t_{CP} + t_{CH} \geq 97.92$ *ns*

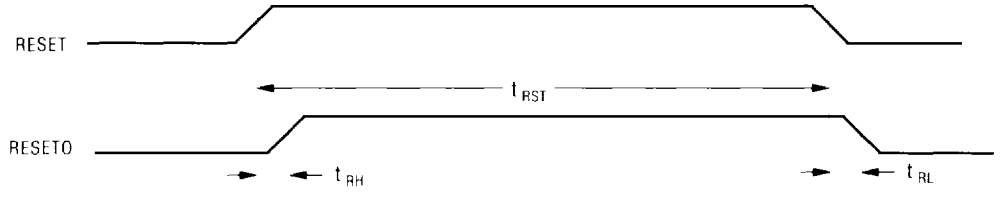
Figure 6-1. Clock Input



Reset Input

Symbol	Parameter	Min	Max	Unit	Note
t_{RST}	RESET pulse width	200	-	ns	-
t_{RH}	RESET high to RESETO high	-	50	ns	-
t_{RL}	RESET low to RESETO low	-	50	ns	-

Figure 6-2. Reset Input



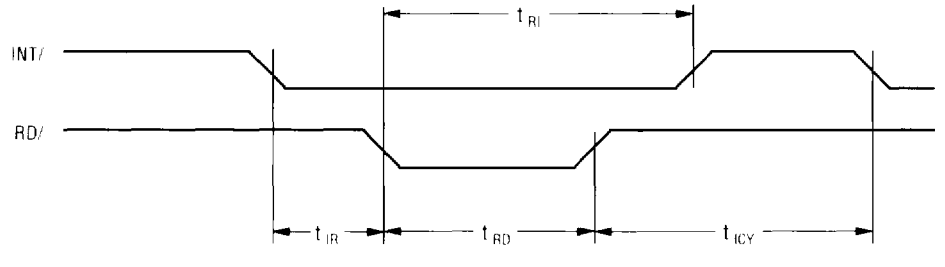
Interrupt Output

Symbol	Parameter	Min	Max	Unit	Note
t_{IR}	INT/ low to RD/ low	0	-	ns	1
t_{RD}	RD/ pulse width	25	-	ns	2
t_{RI}	RD/ low to INT/ high	-	75	ns	-
t_{ICY}	RD/ high to INT/ low	t_{CS}	-	ns	-

1 *The Interrupt register should not be read when INT/ is false.*

2 *Refer to the register read specifications for timing requirements of CS/, RD/, and address for reading the Interrupt register.*

Figure 6-3. Interrupt Output



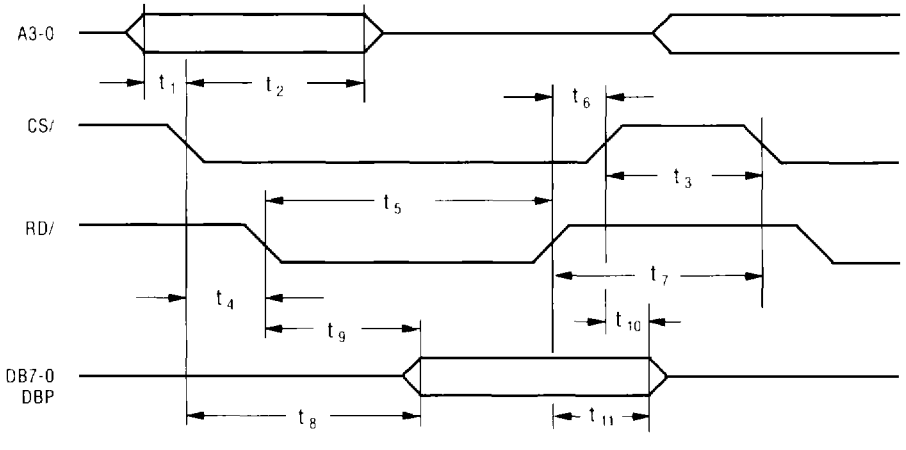
Register Interface Timing

Register Read Cycle

Symbol	Parameter	Min	Max	Unit	Note
t_1	Address setup to CS/ low	0	-	ns	-
t_2	Address Hold from CS/ low	50	-	ns	-
t_3	CS/ high to CS/ low	40	-	ns	-
t_4	CS/ low to RD/ low	0	-	ns	-
t_5	RD/ pulse width	25	-	ns	-
t_6	RD/ high to CS/ high	0	-	ns	-
t_7	RD/ high to CS/ low	40	-	ns	-
t_8	CS/ low to data valid	0	40	ns	1
t_9	RD/ low to data valid	0	25	ns	1
t_{10}	CS/ high to data release	2	25	ns	2
t_{11}	RD/ high to data release	2	25	ns	2

1 *Both t_8 and t_9 specifications must be met.*
2 *RD/ edges may precede or follow CS/ edges.*

Figure 6-4. Register Read Cycle Timing

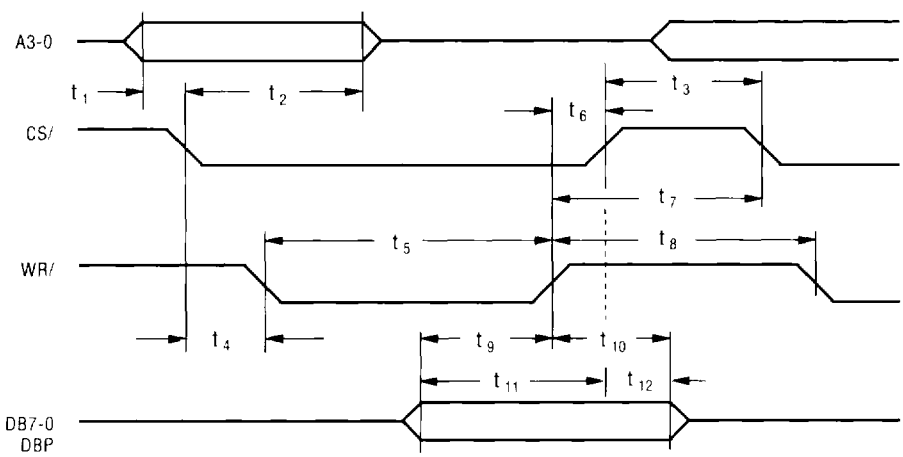


Register Write Cycle

Symbol	Parameter	Min	Max	Unit	Note
t_1	Address setup to CS/ low	0	-	ns	-
t_2	Address Hold from CS/ low	50	-	ns	-
t_3	CS/ high to CS/ low	40	-	ns	1
t_4	CS/ low to WR/ low	0	-	ns	2
t_5	WR/ pulse width	25	-	ns	-
t_6	WR/ high to CS/ high	0	-	ns	2
t_7	WR/ high to CS/ low	40	-	ns	-
t_8	WR/ high to WR/ low	40	-	ns	1
t_9	Data setup to WR/ high	8	-	ns	3
t_{10}	Data hold from WR/ high	0	-	ns	4
t_{11}	Data setup to CS/ high	10	-	ns	3
t_{12}	Data hold from CS/ high	35	-	ns	4

1 *If WR/ is held low t_3 is 35 ns (min).*
2 *WR/ edges may precede or follow CS/ edges.*
3 *Either t_9 or t_{11} specification must be met.*
4 *Either t_{10} or t_{12} specification must be met.*

Figure 6-5. Register Write Cycle Timing



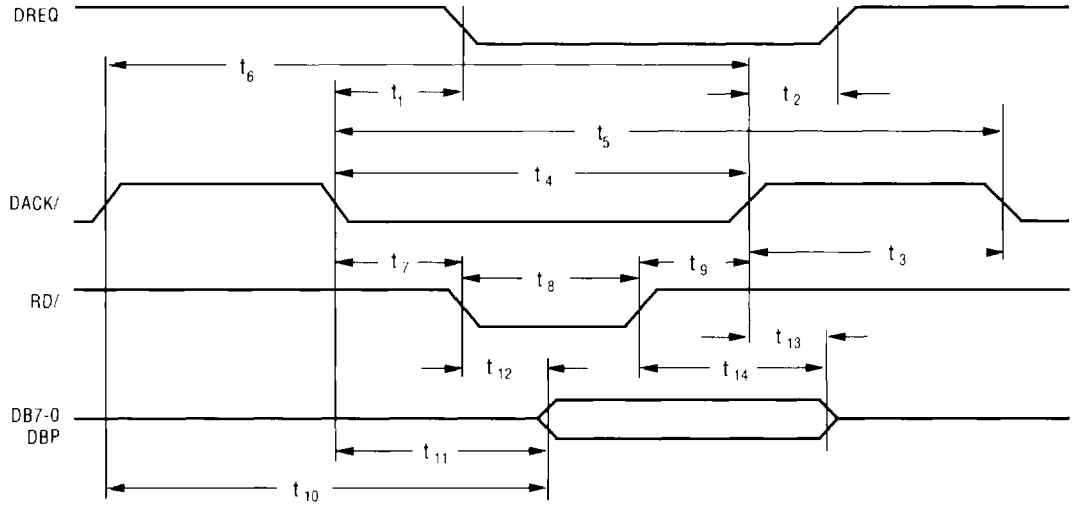
DMA Interface Timing

DMA Read Cycle

Symbol	Parameter	Min	Max	Unit	Note
t_1	DACK/ low to DREQ low	-	20	ns	1
t_2	DACK/ high to DREQ high	-	20	ns	2
t_3	DACK/ high to DACK/ low	12	-	ns	-
t_4	DACK/ pulse width	35	-	ns	-
t_5	DACK/ low to DACK/ low	75	-	ns	-
t_6	DACK/ high to DACK/ high	$t_{CS} + 30 - t_3$ and $2t_{CP}$	-	ns	3, 4
t_6	DACK/ high to DACK/ high	$2t_{CS} + 35 - t_3$ and $3t_{CP}$	-	ns	3, 5
t_7	DACK/ low to RD/ low	0	-	ns	6
t_8	RD/ pulse width	t_{12}	-	ns	-
t_9	RD/ high to DACK/ high	0	-	ns	7
t_{10}	DACK/ high to data valid	-	30	ns	8
t_{11}	DACK/ low to data valid	-	25	ns	8
t_{12}	RD/ low to data valid	-	25	ns	8
t_{13}	DACK/ high to data release	2	25	ns	-
t_{14}	RD/ high to data release	2	25	ns	-

1 *Negation pending.*
2 *Assertion pending.*
3 *Synchronous transfers only.*
4 *FASTCLK disabled.*
5 *FASTCLK enabled.*
6 *RD/ low may precede DACK/ low.*
7 *RD/ high may follow DACK/ high.*
8 *Both t_{10} and t_{11} specifications must be met.*

Figure 6-6. DMA Read Cycle Timing

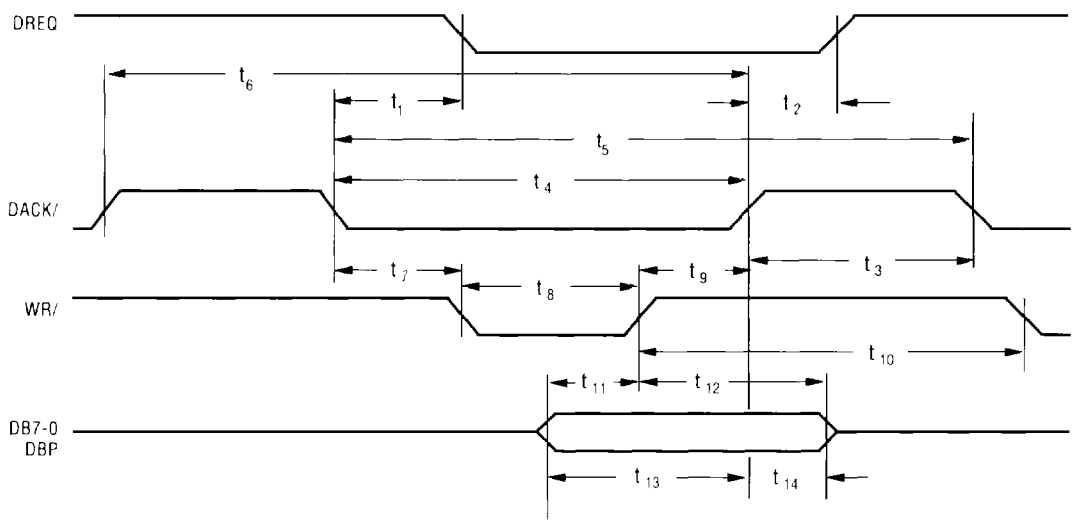


DMA Write Cycle

Symbol	Parameter	Min	Max	Unit	Note
t_1	DACK/ low to DREQ low	-	20	ns	1
t_2	DACK/ high to DREQ high	-	20	ns	2
t_3	DACK/ high to DACK/ low	12	-	ns	3
t_4	DACK/ pulse width	35	-	ns	-
t_5	DACK/ low to DACK/ low	75	-	ns	-
t_6	DACK/ high to DACK/ high	$t_{CS} + 30 - t_3$ and $2t_{CP}$	-	ns	4, 5
t_6	DACK/ high to DACK/ high	$2t_{CS} + 35 - t_3$ and $3t_{CP}$	-	ns	4, 6
t_7	DACK/ low to WR/ low	0	-	ns	7
t_8	WR/ pulse width	30	-	ns	-
t_9	WR/ high to DACK/ high	0	-	ns	8
t_{10}	WR/ high to WR/ low	30	-	ns	-
t_{11}	Data setup to WR/ high	8	-	ns	9
t_{12}	Data hold from WR/ high	0	-	ns	10
t_{13}	Data setup to DACK/ high	10	-	ns	9
t_{14}	Data hold from DACK/ high	10	-	ns	10

1 *Negation pending.*
2 *Assertion pending.*
3 *If WR/ is held low t_7 = 30 ns (min).*
4 *Synchronous transfers only.*
5 *FASTCLK disabled.*
6 *FASTCLK enabled.*
7 *WR// low may precede DACK/ low.*
8 *WR/ high may follow DACK/ high.*
9 *Either t_{11} or t_{13} specification must be met.*
10 *Either t_{12} or t_{14} specification must be met.*

Figure 6-7. DMA Write Cycle Timing



SCSI Interface Timing

SCSI Asynchronous Timing

Symbol	Parameter	Min	Max	Unit	Note
	SINGLE-ENDED MODE [1]				
t_1	ACKI/ low to REQO/ high	-	50	ns	-
t_2	ACKI/ high to REQO/ low	-	45	ns	3, 6
t_3	REQI/ high to ACKO/ high	-	50	ns	-
t_4	REQI/ low to ACKO/ low	-	50	ns	4, 6
	Output Cycle				
t_5	Data setup to REQO/ low	60	-	ns	-
t_5	Data setup to ACKO/ low	60	-	ns	-
t_6	Data hold from REQI/ high	5	-	ns	5
t_6	Data hold from ACKI/ low	5	-	ns	5
	DIFFERENTIAL MODE [2]				
t_1	ACKI/ low to REQO/ high	-	30	ns	-
t_2	ACKI/ high to REQO/ low	-	30	ns	3, 6
t_3	REQI/ high to ACKO/ high	-	25	ns	-
t_4	REQI/ low to ACKO/ low	-	30	ns	4, 6
	Output Cycle				
t_5	Data setup to REQO/ low	70	-	ns	-
t_5	Data setup to ACKO/ low	70	-	ns	-
t_6	Data hold from REQI/ high	5	-	ns	5
t_6	Data hold from ACKI/ high	5	-	ns	5
	INPUT CYCLE				
t_7	Data setup to REQI/ low	0	-	ns	-
t_7	Data setup to ACKI/ low	0	-	ns	-
t_8	Data hold from REQI/ low	-	18	ns	-
t_8	Data hold from ACKI/ low	-	18	ns	-

1 *200pF loading, data out on lines SDOP/, SDO7/-0/.*
2 *Data out on lines SDIP/, SDI7/-0/.*
3 *Data setup to REQO/ low specification must also be met (output cycle only).*
4 *Data setup to ACKO/ low specification must also be met (output cycle only).*
5 *FIFO is not empy.*
6 *FIFO is not full (input cycle only).*

Figure 6-8. SCSI Asynchronous Output

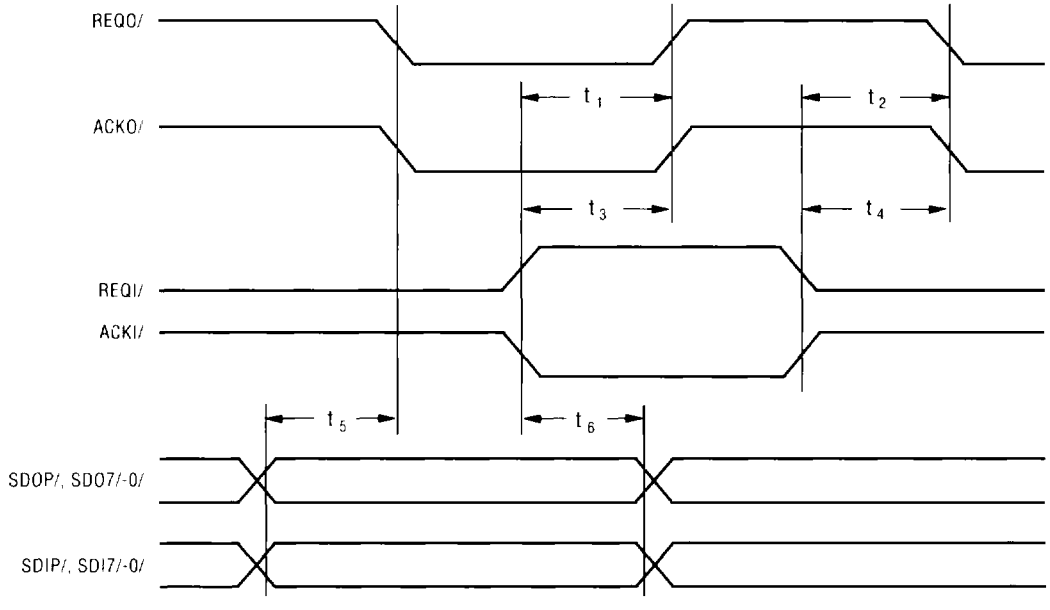
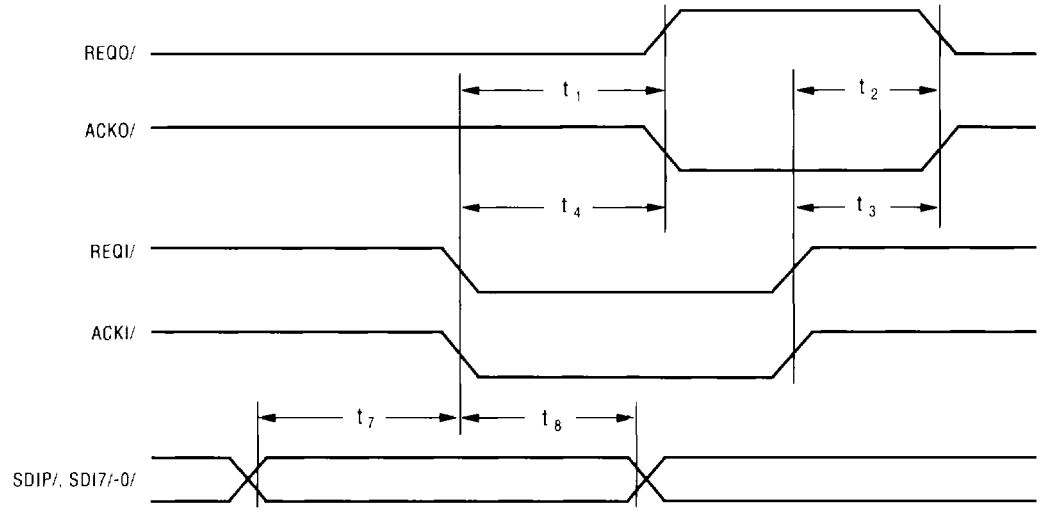


Figure 6-9. SCSI Asynchronous Input



SCSI Synchronous Timing

Symbol	Parameter	Min	Max	Unit	Note
	OUTPUT CYCLE				
	Normal SCSI, Single-Ended Mode [1]				
t_1	REQO/, ACKO/ assertion period	90	-	ns	-
t_2	REQO/, ACKO/ negation period	90	-	ns	-
t_3	Data setup to REQO/ low, ACKO/ low	55	-	ns	-
t_4	Data hold from REQO/ low, ACKO/ low	100	-	ns	-
	Normal SCSI, Differential Mode [2]				
t_1	REQO/, ACKO/ assertion period	96	-	ns	-
t_2	REQO/, ACKO/ negation period	96	-	ns	-
t_3	Data setup to REQO/ low, ACKO/ low	65	-	ns	-
t_4	Data hold from REQO/ low, ACKO/ low	110	-	ns	-
	Fast SCSI, Single-Ended Mode [3]				
t_1	REQO/, ACKO/ assertion period	30	-	ns	-
t_2	REQO/, ACKO/ negation period	30	-	ns	-
t_3	Data setup to REQO/ low, ACKO/ low	25	-	ns	-
t_4	Data hold from REQO/ low, ACKO/ low	35	-	ns	-
	Fast SCSI Differential Mode [4]				
t_1	REQO/, ACKO/ assertion period	40	-	ns	-
t_2	REQO/, ACKO/ negation period	40	-	ns	-
t_3	Data setup to REQO/ low, ACKO/ low	35	-	ns	-
t_4	Data hold from REQO/ low, ACKO/ low	45	-	ns	-
	INPUT CYCLE				
t_5	REQI/ assertion period	27	-	ns	-
t_6	REQI/ negation period	20	-	ns	-
t_7	ACKI/ assertion period	20	-	ns	-
t_8	ACKI/ negation period	20	-	ns	-
t_9	Data setup to REQI/ low, ACKI/ low	5	-	ns	-
t_{10}	Data hold from REQI/ low, ACKI/ low	15	-	ns	-

1 *5 MB/s max, data out lines SDOP/, SDO7/-0/.*
2 *5 MB/s max, data out on lines SDIP/, SDI7/-0/.*
3 *10 MB/s max, data out lines SDOP/, SDO7/-0/.*
4 *10 MB/s max, data out on lines SDIP/, SDI7/-0/.*

Figure 6-10. SCSI Synchronous Output

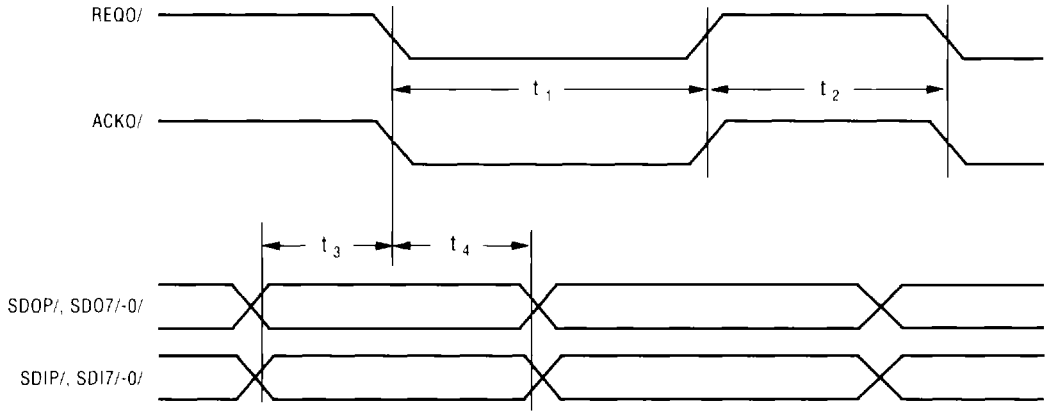


Figure 6-11. SCSI Synchronous Input