Signetics

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Status	Product Specification
FAST Products	

FAST 74F1604 LATCH

Dual Octal Latch

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1604	7.0 ns	70mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low state)**
- **Stores 16-Bit-Wide data inputs, multiplexed 8-Bit outputs**
- **Propagation delay 7.0ns typical**
- **Power supply current 70mA typical**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F1604N
28-Pin Plastic SOL	N74F1604D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

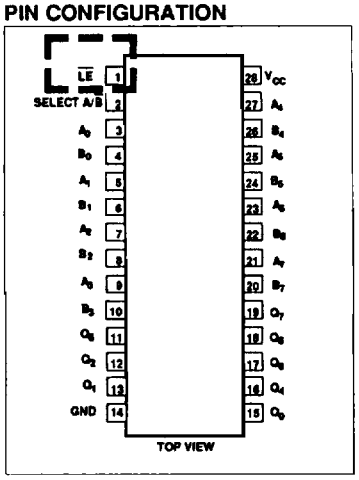
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs	1.0/.033	20μA/20μA
SELECT A/$\overline{B}$	Select input	1.0/.033	20μA/20μA
$\overline{LE}$	Latch Enable input (Active Low)	1.0/.033	20μA/20μA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

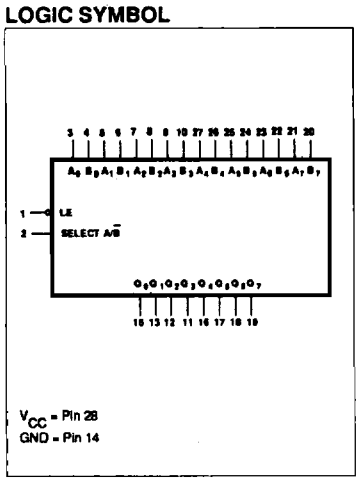
DESCRIPTION

The 74F1604 is a Dual Octal Transparent Latch. Organized as 8-bit A and B latches, the latch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT A/$\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight outputs. Data from the B inputs are selected when SELECT A/$\overline{B}$ is Low: data from the A inputs are selected when SELECT A/$\overline{B}$ is High. Data enters the latch on the falling edge of the Latch Enable ($\overline{LE}$) input. The Latch remains transparent to the data inputs while $\overline{LE}$ is Low, and stores the data that is present one setup time before the Low-to-High Latch Enable transition

PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)