IBM0616328RL6A

Advance **16Mb Double Data Rate Synchronous Graphics RAM**

Special Features

- 150MHz maximum clock frequency
- 300Mbps/pin maximum data rate
- Zero Latency operations:
  - Write to Read
  - Write to Precharge
- Read with Auto Precharge Command
  - Read Command to Auto Precharge delay of only one cycle
  - Requires only a minimum number of cycles to execute next Read command

Features

- Double Data Rate (DDR)
- Bidirectional Data Strobe with 1/2 clock cycle preamble and postamble
- On-chip DLL
- Quad bank operation
- Fully synchronous
- Programmable burst type, burst length, and $\overline{\text{CAS}}$ latency
- Burst Read and Write operations
- Read Burst termination by command
- 16 column Block Write in 2 clock cycles
- Independent byte operations
- Auto Precharge and Auto Refresh modes
- 2K Refresh cycles/16ms
- SSTL_2 compatible inputs
- Differential clocks
- Single 3.3V ± 0.3 power supply
- 100-pin LQFP (0.65mm lead pitch)

Timing Options	Marking
100 MHz clock rate	-10
125 MHz clock rate	-8
150 MHz clock rate	-6R7

Key Timing Parameters

Speed Grade	Clock Frequency (MHz)	DQ Burst Frequency (MHz)
-10	100	200
-8	125	250
-6R7	150[1]	300

[1] Target high speed sort.

Description

The IBM 512K x 32 SGRAM is a high speed 16Mb Double Data Rate (DDR) CMOS Synchronous DRAM with built-in graphics features. It is internally configured as a quad bank 128K x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal CLK). In addition, DQ and DQ Mask are registered at the 50% point between two successive clocks. Quad banks are organized as 512 rows x 256 columns x 32 bits.

Reads and Writes to the SGRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations. By having a Programmable Mode Register, the system can choose Read or Write burst lengths of 2, 4, or 8 locations. A Data Strobe (DQS) is provided to assist in reading data on each clock edge. Likewise, a DQS is provided by the controller during a Write, with data centered on the edge of the DQS.

An Auto Precharge function can be enabled to provide a self-timed precharge. For Reads, this precharge is initiated after the first cycle of the Read Burst. For Writes, it is initiated at the end of the burst sequence.

The SGRAM uses an internal pipelined architecture to achieve high speed operation, which also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing an alternate bank will hide the precharge cycles and provide seamless high speed random operation.

The SGRAM differs from the Synchronous DRAM (SDRAM) by providing a 16 column Block Write function and a Write-Per-Bit (WPB) function. The Block Write and WPB functions may be combined with the individual byte enables DM_0-DM_3.

The part is designed to operate at 3.3V only. An Auto Refresh mode is provided along with a power saving Power Down mode. All inputs and outputs are SSTL_2 compatible.

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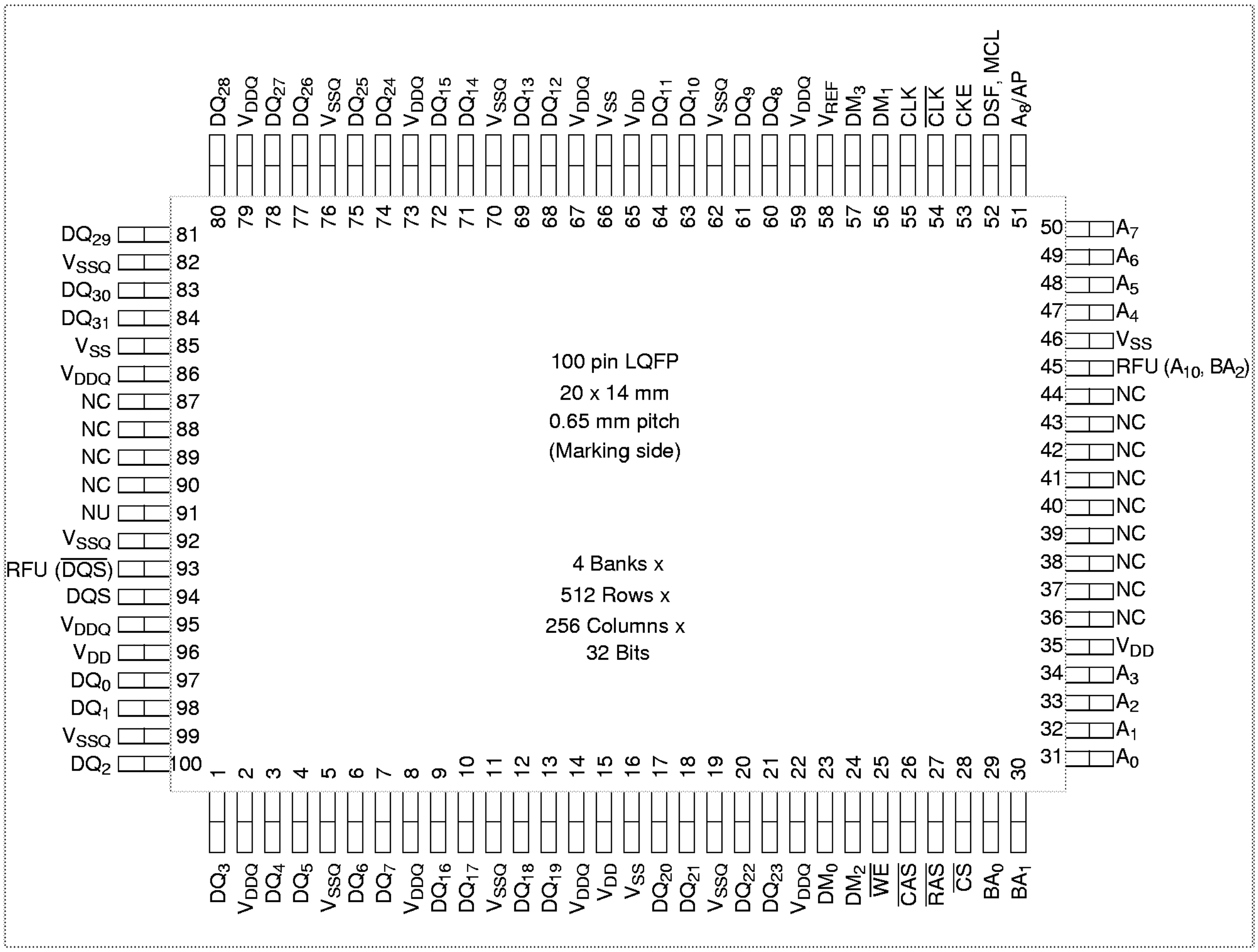
Pin Configuration



Symbol	Function
A_0-A_8	Address Inputs
A_0-A_8	Row Address Inputs
A_0-A_7	Column Address Inputs
BA_0, BA_1	Bank Selects (4 Bank)
A_8/AP	Auto Precharge
$\overline{CS}$	Chip Select
$\overline{CAS}$	Column Address Strobe
CKE	Clock Enable
CLK, $\overline{CLK}$	Differential System Clock Inputs
DQ_0-DQ_{31}	Data Inputs/Outputs (DDR)
DM_0-DM_3	DQ Mask Enables
DQS	Bidirectional Data Strobe

Symbol	Function
DSF	Special Function Enable
MCL	Must Connect Low
NC	No Connection (Chip to pin)
NU	Not Usable
$\overline{RAS}$	Row Address Strobe
V_{DD}	Supply Voltage
V_{SS}	Ground
V_{DDQ}	Supply Voltage for DQs
V_{SSQ}	Ground for DQs
V_{REF}	Reference Voltage for SSTL_2
$\overline{WE}$	Write Enable
RFU	Reserved for future use

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Input/Output Functional Description

Symbol	Type	Function
CLK, $\overline{CLK}$	Input	The differential system clock inputs. All of the SGRAM inputs are sampled on the rising edge of the clock except DQs and DMs which are sampled on both edges of the DQS.
CKE	Input	Activates the CLK signal when high and deactivates the CLK signal when low. By deactivating the clock, CKE low indicates the Power Down mode or the Self Refresh mode.
$\overline{CS}$	Input	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$	Input	Control inputs that are issued to the command decoder. See the Operative Command Table beginning on page 22 for details.
$\overline{CAS}$	Input	
$\overline{WE}$	Input	
DQS	Input/Output	Data Strobe for input and output data, active on both edges.
DM_0 - DM_3	Input	Masks Write data when high, with zero latency.
DQ_0 - DQ_{31}	Input/Output	Data Inputs/Outputs are multiplexed on the same pins.
BA_0, BA_1	Input	Selects which bank is to be active.
A_0 - A_8	Input	Row/Column addresses are multiplexed on the same pins. Row addresses: RA_0-RA_8; Column addresses: CA_0-CA_7. Column address A_8 is used for Auto Precharge.
V_{DD}, V_{SS}	Supply	Power and ground for the input buffers and the core logic.
V_{DDQ}, V_{SSQ}	Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	Supply	Reference voltage for inputs.
DSF, MCL		Enables Block Write and Write-per-Bit Functions and must be connected low to disable these special functions.
NU		Must be left unconnected.

Ordering Information

Part Number	Power	Self Refresh	Power Supply	Speed	Package	Notes
IBM0616328RL6A-6R7	SP	Y	3.3V	150	LQFP	1
IBM0616328RL6A-8				125		
IBM0616328RL6A-10				100		

1. SP = Standard Power

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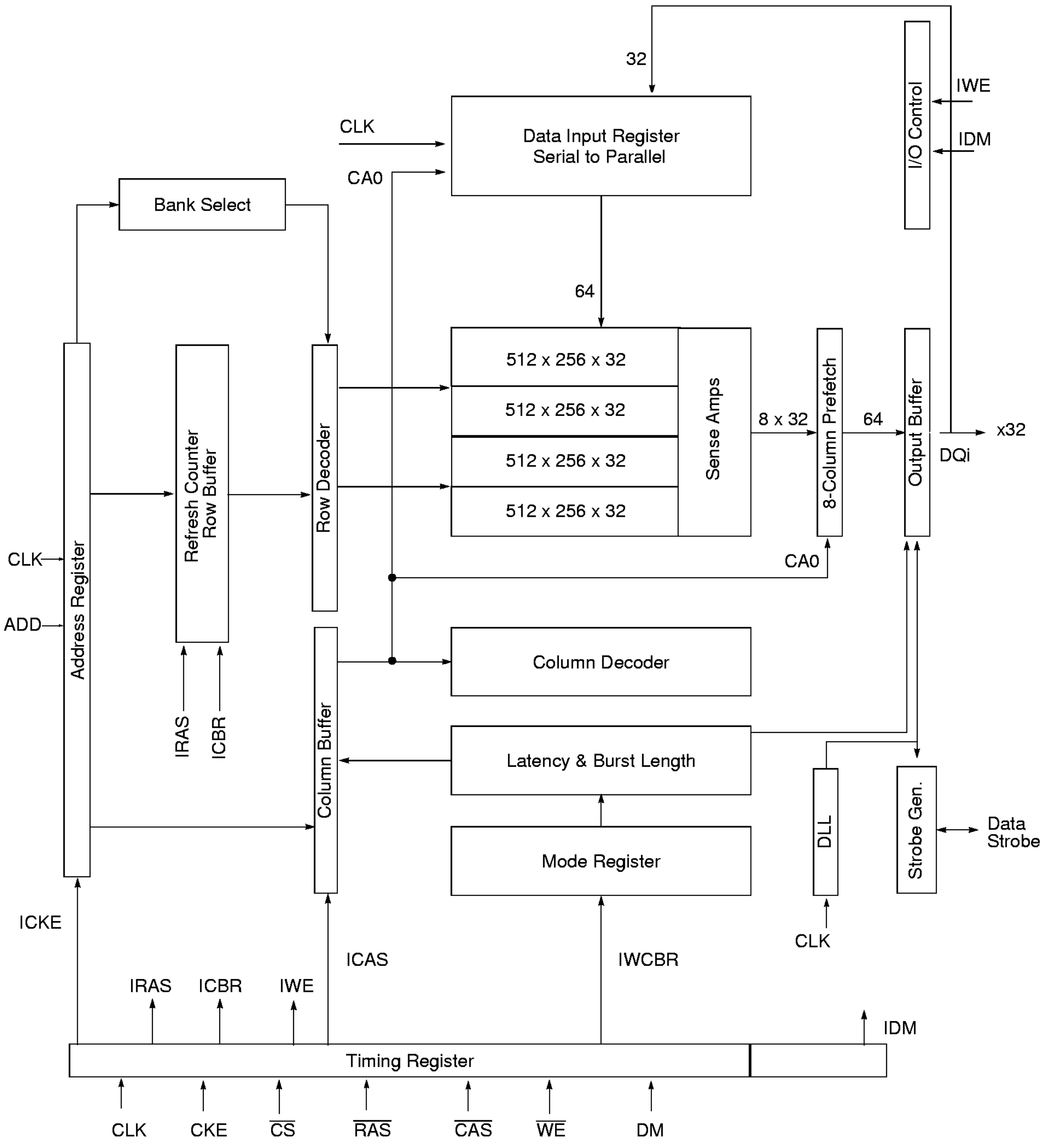
Block Diagram



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Functional Description

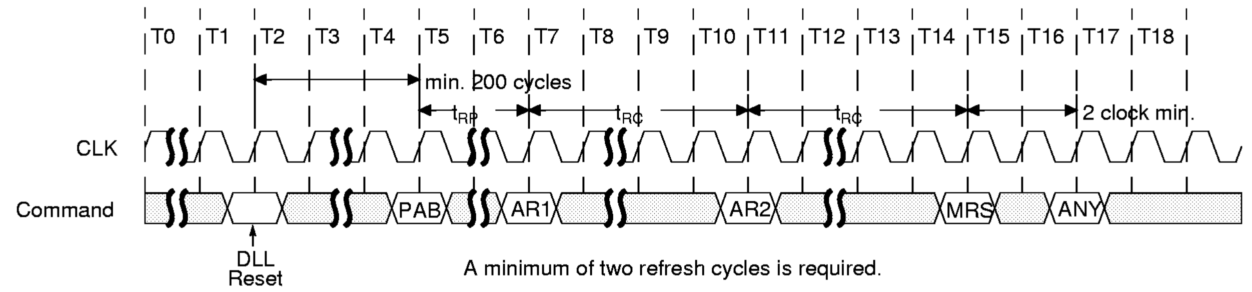
Power-Up Sequence

The following sequence is recommended for Power-Up.

1. Apply power and start clock. Attempt to maintain CKE and DM high and the other pins in a NOP condition at the input.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200µs.
3. Issue a Mode Register Set command for “DLL Reset”. An additional 200 cycles of clock input are required to lock the DLL.
4. Issue a Precharge command for all banks of the device.
5. Issue two or more Self Refresh commands.
6. Issue a Mode Register Set command to initialize the mode register.

Note: Steps 5 and 6 can be reversed (their order is irrelevant).

Power-Up Sequence and Auto Refresh (CBR) Timing



A minimum of two refresh cycles is required.

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Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of the DDR SGRAM. It programs $\overline{CAS}$ latency, addressing mode, burst length, test mode, and various other specific options to make the DDR SGRAM useful for a variety of applications. The default value of the mode register is not defined; therefore the mode register must be written after Power-Up to operate the DDR SGRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (the DDR SGRAM should be in Active mode with CKE already high prior to writing into the mode register). The state of address pins A_0-A_8 and BA_0-BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ going low is written in the mode register. Two clock cycles are requested to complete the Write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A_0-A_2, addressing mode uses A_3, and $\overline{CAS}$ latency (read latency from column address) uses A_4-A_6. A_7 is used for test mode and A_8 is used for DLL Reset. A_7, A_8, BA_0, and BA_1 must be set to low for normal DDR SGRAM operation. Refer to the Mode Register Functions table for specific codes of various burst length, addressing modes, and $\overline{CAS}$ latencies.

Mode Register Functions

BA_1	BA_0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address Key
Reserved for Future Use		DLL	TM	$\overline{CAS}$ Latency			BT	Burst Length			Mode Register

A_8	DLL Reset
0	Normal
1	Activate

A_7	Mode
0	Normal
1	Test

A_3	Burst Type
0	Sequential
1	Interleave

CAS Latency

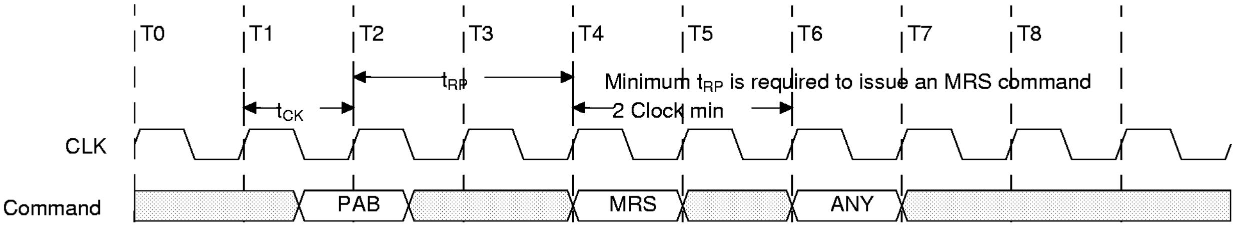
A_6	A_5	A_4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	1.5
1	1	0	2.5
1	1	1	Reserved (3.5)

Burst Length

A_2	A_1	A_0	Sequential	Interleave
0	0	0	Reserved	
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved (Full Page)	Reserved

* RFU (Reserved for future use)
should stay "0" during MRS cycle.

Mode Register Set Timing



MRS can be issued only when all banks are in the precharge or idle states.

Burst Mode Operation

Burst Mode Operation is used to provide a constant flow of data to memory locations (Write cycle), or from memory locations (Read cycle). Two parameters define how the burst mode will operate: burst sequence and burst length. These parameters are programmable and are determined by address bits A_0-A_3 during the Mode Register Set command. Burst type defines the sequence in which the burst data will be delivered or stored to the SGRAM. Two types of burst sequence are supported: sequential and interleave. The burst length controls the number of bits that will be output after a Read command, or the number of bits to be input after a Write command. The burst length can be programmed to have values of 2, 4, or 8. See the Burst Length and Sequence table below for programming information.

Burst Length and Sequence

Burst Length	Starting Address (A_2, A_1, A_0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 0, 1, 2
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

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Load Special Mode Register (LSMR)

The Load Special Mode Register command is used to load the mask and color registers, which are used in Block Write and Masked Write cycles.The data to be written to either the color register or the mask register is applied to the DQs and the control information is applied to the address inputs. During an LSMR cycle, if the address bit A_6 is "1" and all other address inputs are "0", the color register will be loaded with the data on the DQs. This color data is used for Block Write cycles. Similarly, when input A_5 is "1" and all other address inputs are "0" during an LSMR cycle, the mask register will be loaded with the data on the DQs.

Caution:
Never set bit A_5 to "1" when A_6 is set to "1" in the same Load Special Mode Register cycle to avoid unknown operation.

Color Register

The color register is a 32-bit register that supplies the data during Block Write cycles. The Color Register is loaded via the Load Special Mode Register command and will retain data until loaded again with new data or until power is removed from the SGRAM.

Mask Register

The Mask Register (or the Write-per-Bit mask register) is a 32-bit register which acts as a per-bit mask during Masked Write and Masked Block Write cycles. The Mask Register is loaded via the Load Special Mode Register command and will retain data until loaded again or until power is removed from the SGRAM.

Special Mode Register Functions

Address Bits										Functions
BA (A_9)	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	0	0	0	0	0	0	0	0	0	Do not load
0	0	0	0	1	0	0	0	0	0	Enable Mask
0	0	0	1	0	0	0	0	0	0	Load Color Register

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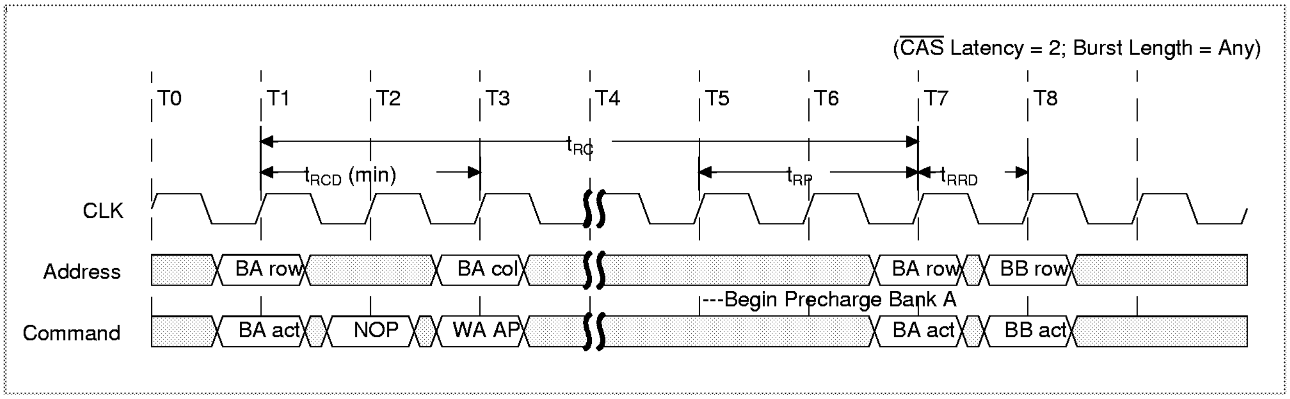
Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The DDR SGRAM has four independent banks, so two Bank Select addresses (BA_0 and BA_1) are supported. The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from the Bank Activate command to the first Read or Write command must meet or exceed the minimum $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD} min). Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD} min).

Bank Activation Timing



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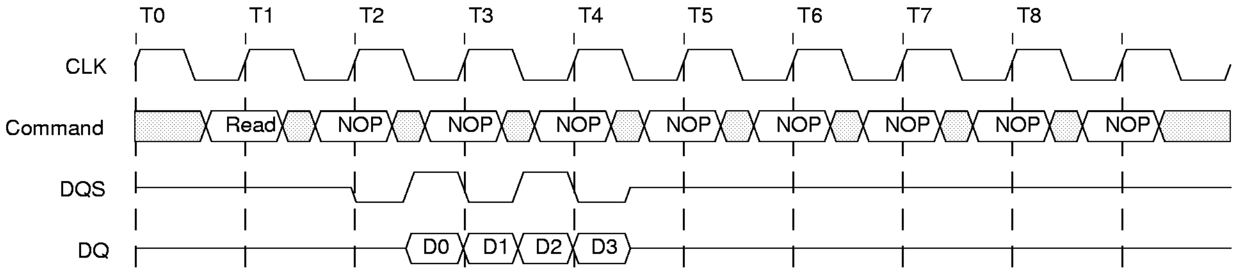
Burst Read Operation

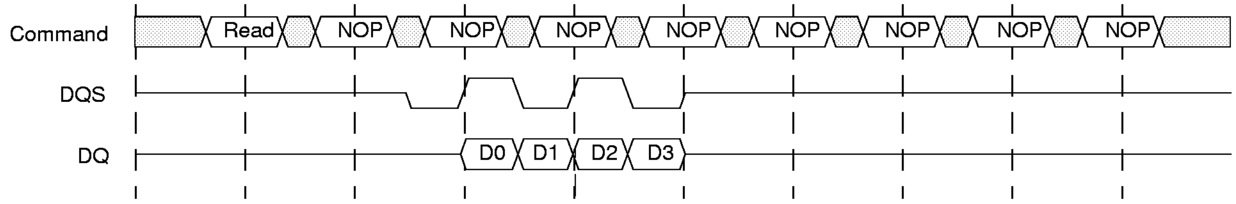
The Burst Read command in DDR SGRAM, as in traditional SGRAMs, is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock after t_{RCD} from the Bank Activate command. The address inputs (A_0-A_7) determine the starting address of the burst. The Mode Register sets the type of burst (sequential or interleave) and the burst length (2, 4, or 8). The first output data is available after the $\overline{CAS}$ latency from the Read command, and the consecutive data are presented on both the rising and falling edges of the Data Strobe (DQS) until the burst length is completed.

Burst Read Timings

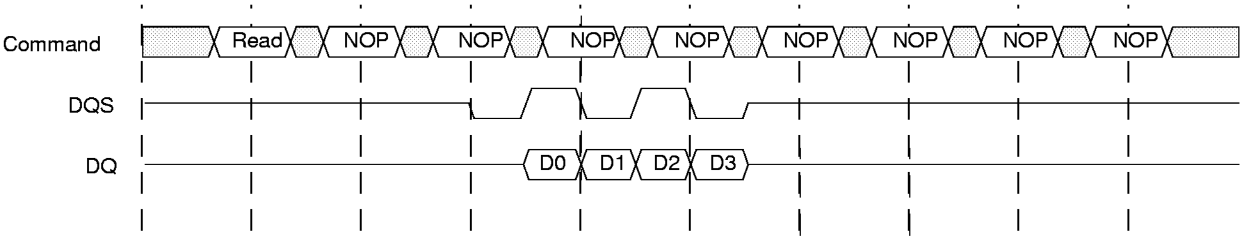
Burst Read Operation ($\overline{CAS}$ Latency = 1.5; Burst Length = 4)



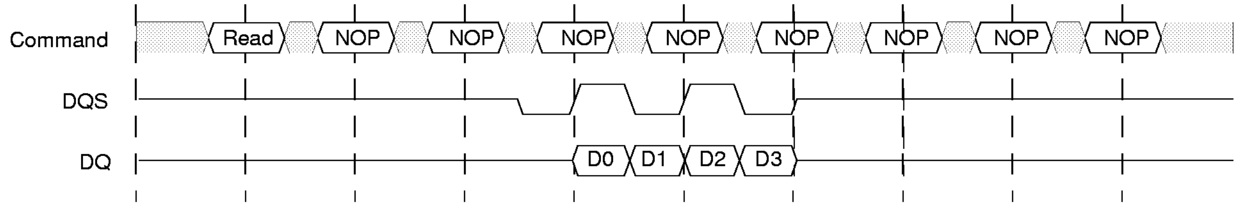
Burst Read Operation ($\overline{CAS}$ Latency = 2; Burst Length = 4)



Burst Read Operation ($\overline{CAS}$ Latency = 2.5; Burst Length = 4)



Burst Read Operation ($\overline{CAS}$ Latency = 3; Burst Length = 4)



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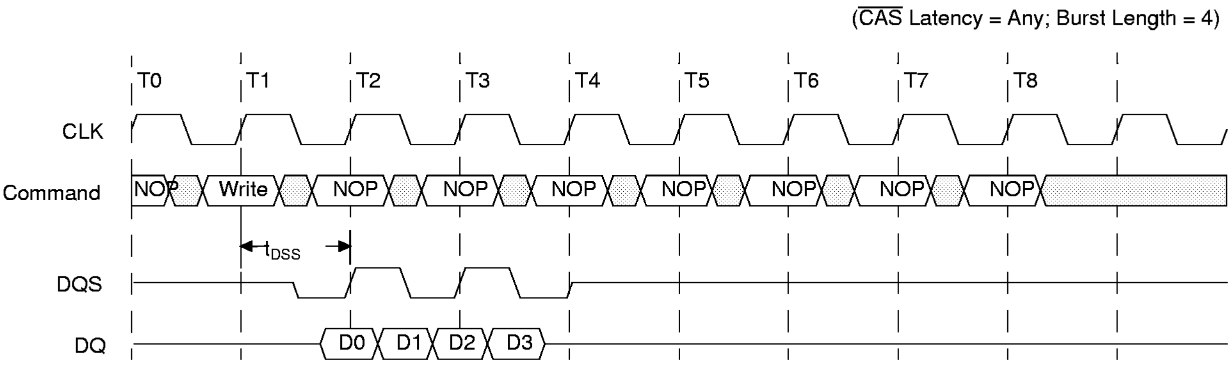
Burst Write Operation

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, DSF, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Data for the first Burst Write cycle must be applied on the DQ pins centered on the same data strobe edge after t_{DSS} from the rising edge of the clock on which the Write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

Burst Write Timing



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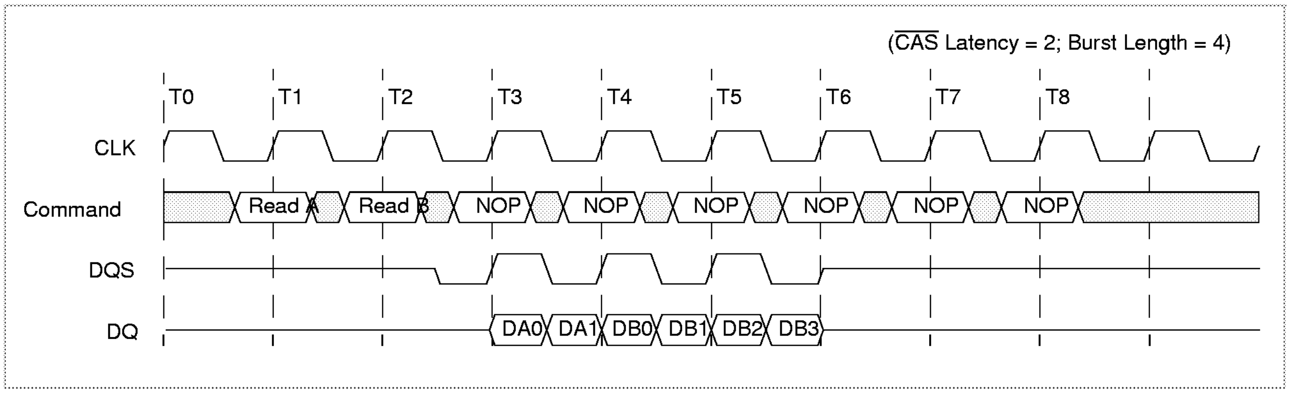
Burst Interruption

Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by a new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the CAS latency from the interrupting Read command is satisfied. At this point, the data from the interrupting Read command appears. Read commands can be performed on consecutive cycles.

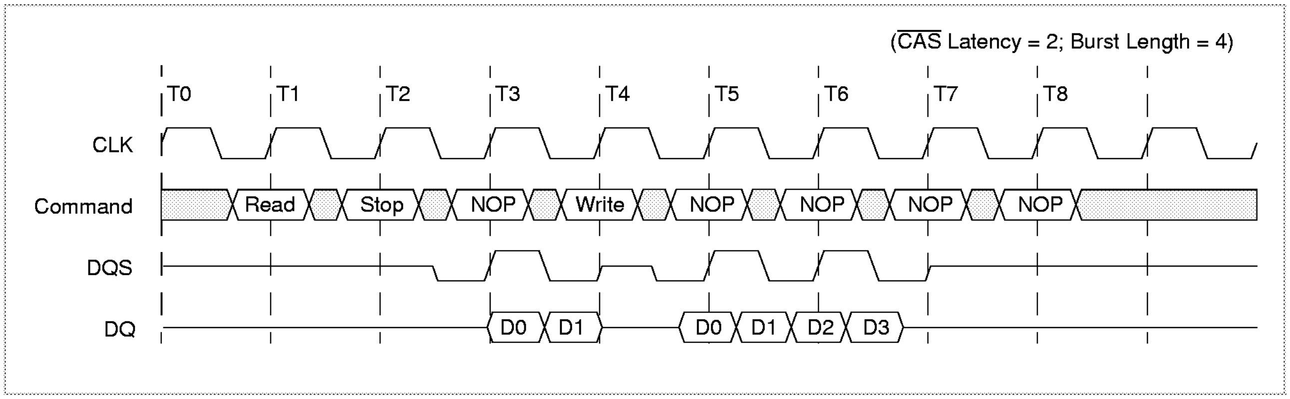
Read Interrupted by a Read Timing



Read Interrupted by a Write & Burst Stop

To interrupt a Burst Read with a Write Command, a Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQs (output drivers) in a high impedance state at least one clock cycle before write data can be driven into the DQs. To insure that the DQs are tri-stated one cycle before the Write operation begins, a Burst Stop command must be applied at least two clock cycles for CL=1.5 and CL=2, and at least three clock cycles for CL=2.5 and CL=3, before the Write command is issued.

Read Interrupted by a Write & Burst Stop Timing



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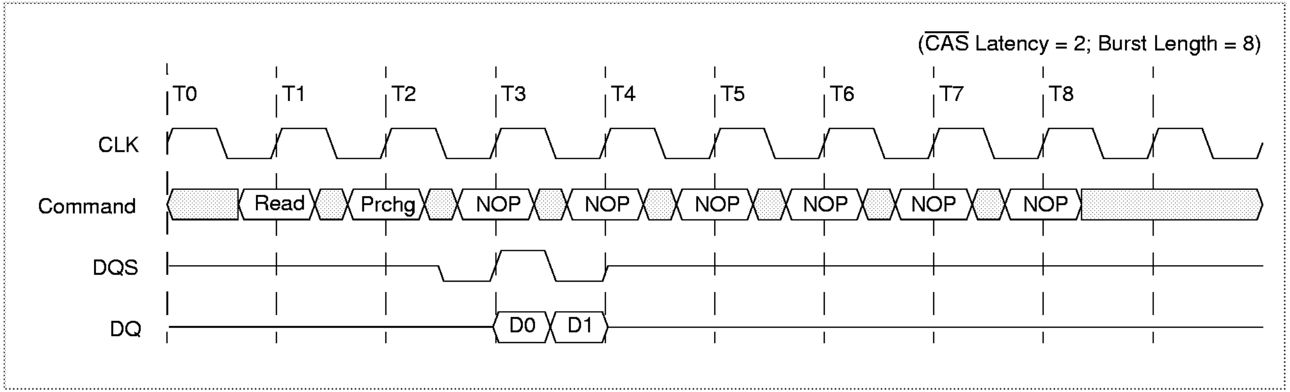
Read Interrupted by a Precharge

A Burst Read operation can be interrupted by a precharge of the same bank. The Precharge command to Output Disable latency is equivalent to the $\overline{\text{CAS}}$ latency.

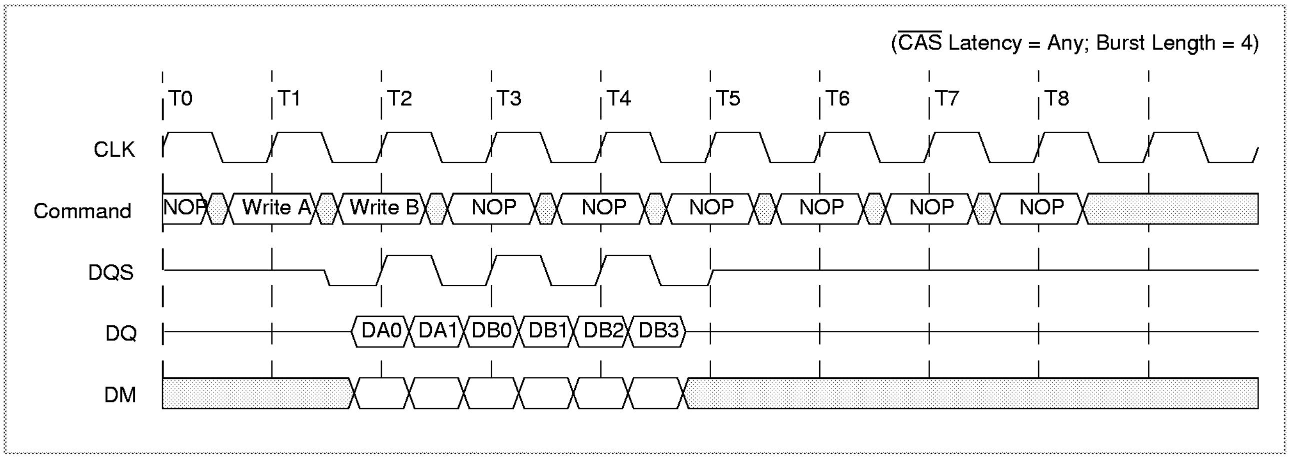
Read Interrupted by a Precharge Timing



Write Interrupted by a Write

A Burst Write can be interrupted before completion of the burst by a new Write command, with the only restriction being that the interval that separates the commands be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

Write Interrupted by a Write Timing



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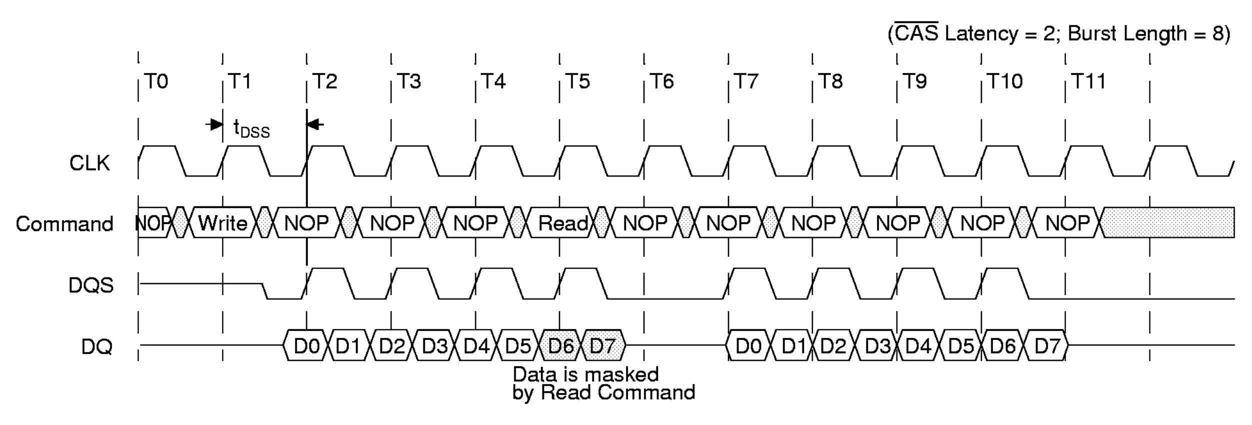
Write Interrupted by a Read

A Burst Write can be interrupted by a Read command of any bank. The DQs must be in a high impedance state at least one clock cycle before interrupting read data appears on the outputs in order to avoid data contention. Data that is present on the DQ pins coincident with or following the Read command will not be written to the memory.

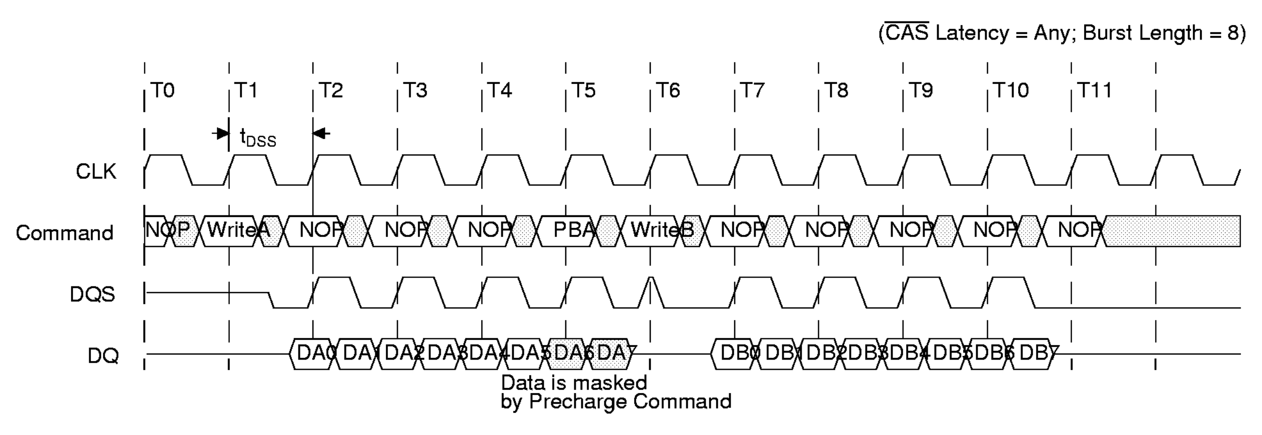
Write Interrupted by a Read Timing



Write Interrupted by a Precharge

A Burst Write operation can be interrupted before completion of the burst by a precharge of the same bank. Random column access is allowed. A Write Recovery time (t_{RDL}) is required from the Last Data to Precharge command. Once the Precharge command is asserted, any residual data from the Burst Write cycle will not be written to the memory.

Write Interrupted by a Precharge Timing



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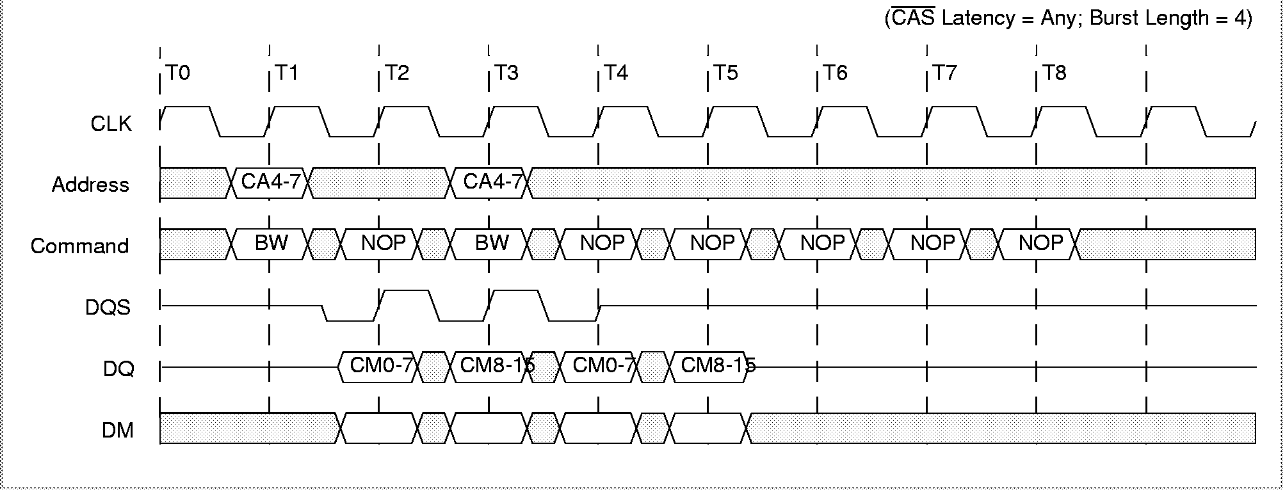
16 Column Block Write

A 16 Column Block Write can be performed by issuing the Block Write command followed by two cycles where the column address mask is provided on the 32 DQ pins. Another Block Write or normal Write commands can be issued after one NOP cycle following the Block Write command. This command writes up to 16 columns of data over two cycles, which is up to four times faster than a normal Write command.

The data written to the array comes from a register, known as the color register, that has one bit for each DQ. The color register is written in a special cycle that must be issued some time prior to issuing the Block Write command.

The two clock cycles following the Block Write command are used to enter the column mask information on the DQs. The 32 DQs are divided into four bytes: DQ_0-DQ_7, DQ_8-DQ_{15}, DQ_{16}-DQ_{23}, and DQ_{24}- DQ_{31}. Within each byte, the eight DQs are used as a column address mask, replacing address bits CA_0-CA_2. Each DQ is used as an address selection: DQ_0 (and DQ_8, DQ_{16}, and DQ_{24}) corresponds to A_0-A_2 equal to 000; DQ_1 (and DQ_9, DQ_{17}, and DQ_{25}) corresponds to A_0-A_2 equal to 001; etc. The DQs that are provided on the first cycle following the Block Write command are used for CA_3=0. The DQs that are provided on the second cycle following the Block Write command are used for CA_3=1. The column address bits provided with the Block Write command are used for CA_4-CA_7.

16 Column Block Write Timing



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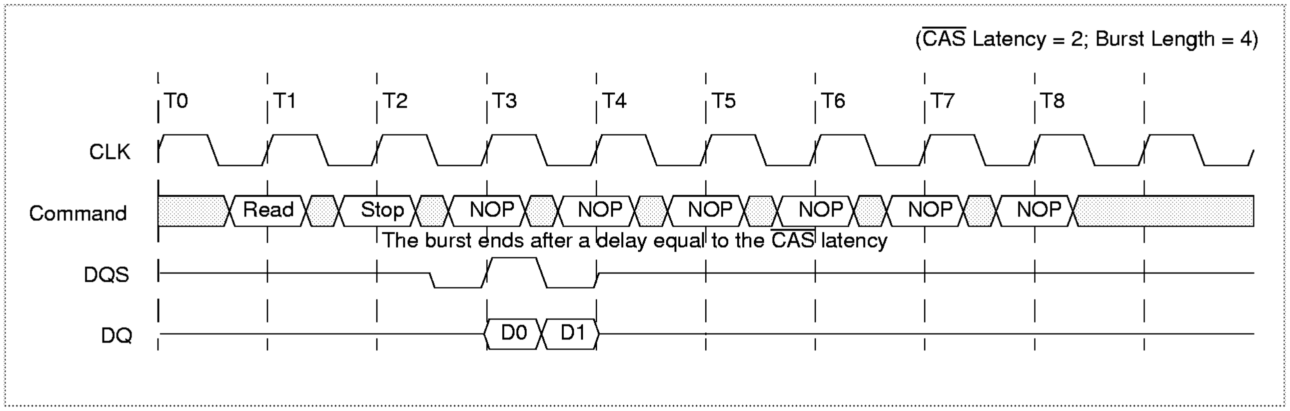
Burst Stop Command

The Burst Stop command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock. The Burst Stop command has the fewest restrictions, making it the easiest method to use when terminating a burst operation before it has been completed. When the Burst Stop command is issued during a Burst Read cycle, both the data and Data Strobe go to a high impedance state after a delay equal to the $\overline{CAS}$ latency. The Burst Stop command, however, is not supported during a Burst Write operation.

Burst Stop Timing



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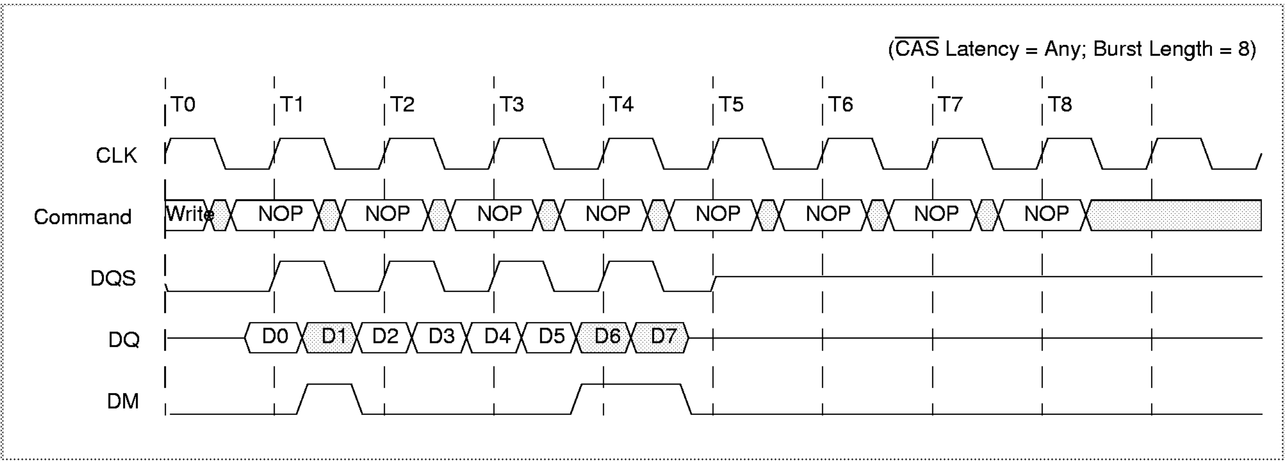
Data Mask Function

The DDR SGRAM has a Data Mask function that is used in conjunction with the Write cycle, but not the Read cycle. When the Data Mask is activated (DM high) during a Write operation, the Write is blocked (Mask to Data Latency = 0).

When issued, the Data Mask must be referenced to both the rising and falling edges of Data Strobe.

Data Mask Timing



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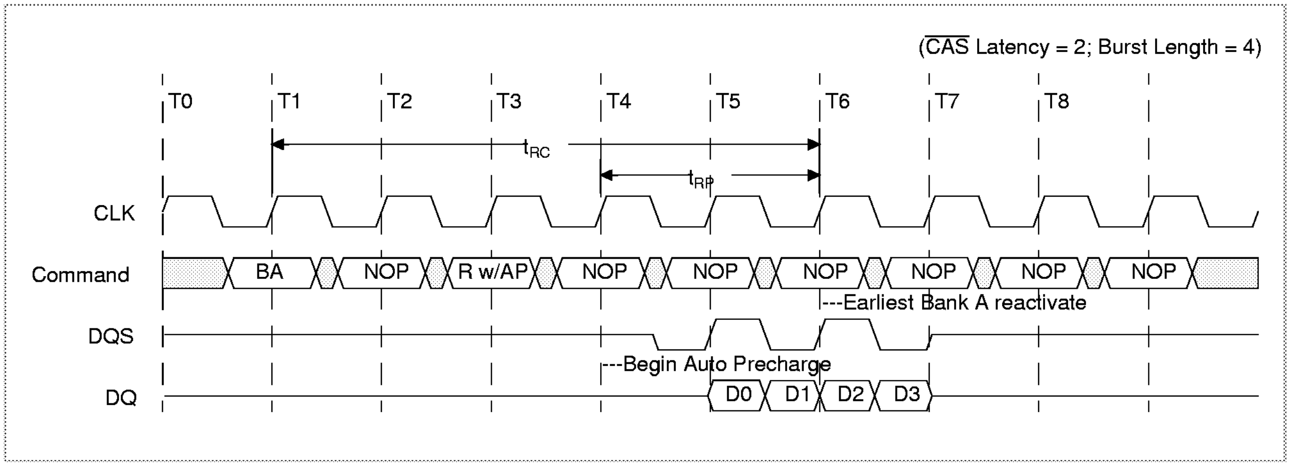
Auto Precharge Operation

The Auto Precharge operation can be issued by having column address A_8 high when a Read or Write command is asserted. If A_8 is low when a Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during the Read or Write cycle after t_{RAS} (min) is satisfied.

Read with Auto Precharge

If a Read with Auto Precharge command is initiated, the DDR SGRAM automatically enters the Precharge operation one clock cycle after the Read command regardless of burst length or $\overline{CAS}$ latency. If not, the precharge operation will be delayed until t_{RAS} (min) is satisfied. Once the Precharge operation has started, the bank cannot be reactivated and the new command cannot be asserted until the precharge time (t_{RP}) has been satisfied.

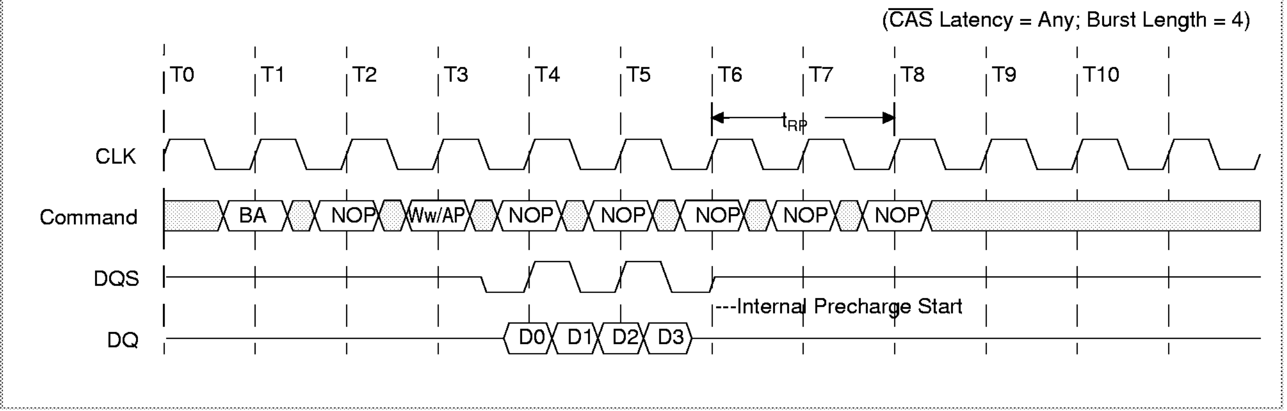
Read with Auto Precharge Timing



Write with Auto Precharge

If A_8 is high when a Write command is issued, the Write with Auto Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping t_{RDL}(min).

Write with Auto Precharge Timing



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Precharge Command

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is issued when $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. This command can be used to precharge each bank independently or all banks simultaneously. The Bank Select addresses (BA_0, BA_1) are used to define which bank is precharged when the command is initiated. After t_{RP} from the precharge, a Bank Activate command to the same bank can be initiated.

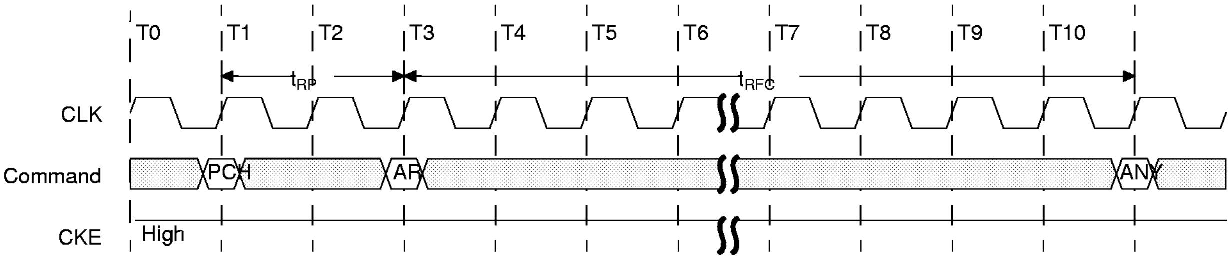
Bank Select for Precharge by Bank Address Bits

A_8/AP	BA_1	BA_0	Precharge
0	0	0	Bank A only
0	0	1	Bank B only
0	1	0	Bank C only
0	1	1	Bank D only
1	X	X	All banks

Auto Refresh

The Auto Refresh command is issued by having $\overline{CS}$, $\overline{RAS}$, and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock. All banks must be precharged and idle for a t_{RP}(min) before the Auto Refresh command is applied. No control of the address pins is required once this cycle has started because of the internal address counter. When the Auto Refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate command or subsequent Auto Refresh command must be greater than or equal to the t_{RFC}(min).

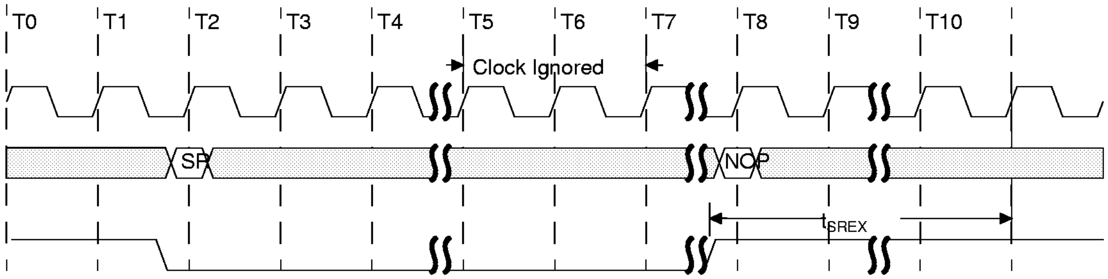
Auto Refresh Timing



Self Refresh

The Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the Self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. During the Self Refresh mode, all of the external control signals are disabled except CKE. The DLL is internally disabled during Self Refresh operation and the clock is ignored to reduce power. To exit the Self Refresh mode, supply stable clock input while returning CKE high, assert a deselect or NOP command, then assert CKE high for a time longer than t_{SREX} in order to lock DLL.

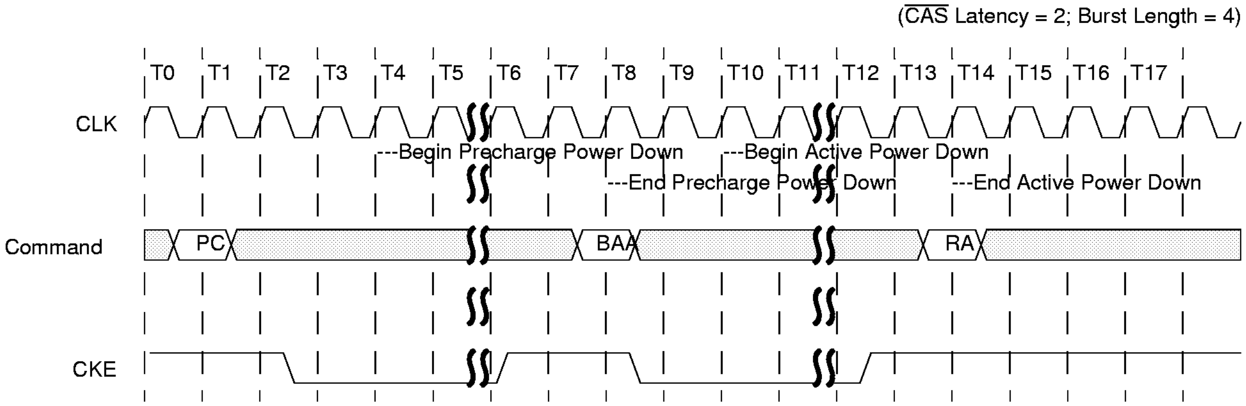
Self Refresh Timing



Power Down Mode

The Power Down mode is entered when CKE is low and exited when CKE is high. Once the Power Down mode is initiated, all of the receiver circuits except CLK, $\overline{CLK}$, CKE, and the DLL circuitry are gated off to reduce power consumption. All banks should be in an idle state prior to entering the Precharge Power Down Mode and CKE should be set high at least 1CLK+t_{IS} prior to the Row Activate command. During Power Down Mode, refresh operations cannot be performed: therefore, the device cannot remain in Power Down Mode longer than the refresh period (t_{REF}) of the device.

Power Down Mode Timing



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Operative Command Table (Part 1 of 6)

Current State	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	DSF	Address	Command	Action	Notes
Idle	H	X	X	X	X	X	INHBT	NOP or Power Down	3
	L	H	H	X	X	X	NOP or BST	NOP or Power Down	3
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	1
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	1
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	Row Active: No I/O Mask	
	L	L	H	H	H	BA, RA	ACTM	Row Active: I/O Mask	
	L	L	H	L	X	BA, PA	PRE/PREAL	NOP	
	L	L	L	H	X	X	REF/SREF	Refresh or Self Refresh	4
	L	L	L	L	L	Op-Code	LMR	Mode Register Access	
	L	L	L	L	H	Op-Code	LSMR	Special Mode Register Access	
Row Active	H	X	X	X	X	X	INHBT	NOP	
	L	H	H	X	X	X	NOP or BST	NOP	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Begin Read: Determine AP	9
	L	H	L	L	L	BA, CA, AP	WR/WRA	Begin Write: Determine AP	9
	L	H	L	L	H	BA, CA, AP	BW/BWA	Block Write: Determine AP	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	1
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	
	L	L	H	L	X	BA, PA	PRE/PREAL	Precharge	6
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	Special Mode Register Access	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All input buffers except CKE will be disabled.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask preceding data which don't satisfy t_{DPL}.
9. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8)
BA = Bank Address (BA_0-BA_1)
PA = Precharge All (A_8)
NOP = No Operation Command
CA = Column Address (A_0 - A_7)
AP = Auto Precharge (A_8)

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Operative Command Table (Part 2 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Action	Notes
Read	H	X	X	X	X	X	INHBT	Continue Burst to End → Row Active	
	L	H	H	X	X	X	NOP	Continue Burst to End → Row Active	
	L	H	H	L	X	X	BST	Burst Stop → Row Active	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Term Burst, New Read: Determine AP	7
	L	H	L	L	L	BA, CA, AP	WR/WRA	Term Burst, Start Write: Determine AP	2, 7
	L	H	L	L	H	BA, CA, AP	BW/BWA	Term Burst, Start Block Write: Determine AP	2, 7
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	1
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREAL	Term Burst, Precharging	
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	
Write	H	X	X	X	X	X	INHBT	Continue Burst to End → Row Active	
	L	H	H	X	X	X	NOP	Continue Burst to End → Row Active	
	L	H	H	L	X	X	BST	ILLEGAL	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Term Burst, New Read: Determine AP	7
	L	H	L	L	L	BA, CA, AP	WR/WRA	Term Burst, Start Write: Determine AP	2, 7
	L	H	L	L	H	BA, CA, AP	BW/BWA	Term Burst, Start Block Write: Determine AP	2, 7
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	1
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREAL	Term Burst, Precharging	8
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All input buffers except CKE will be disabled.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask preceding data which don't satisfy t_{DPL}.
9. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8)
BA = Bank Address (BA_0-BA_1)
PA = Precharge All (A_8)
NOP = No Operation Command
CA = Column Address (A_0 - A_7)
AP = Auto Precharge (A_8)

Operative Command Table (Part 3 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Action	Notes
Read with Auto Precharge	H	X	X	X	X	X	INHBT	Continue Burst to End → Precharging	
	L	H	H	X	X	X	NOP	Continue Burst to End → Precharging	
	L	H	H	L	X	X	BST	ILLEGAL	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	1
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	1
	L	L	L	H	X	X	REF/SREF	ILLEGAL	1
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	INHBT	Continue Burst to End → Precharging	
	L	H	H	X	X	X	NOP	Continue Burst to End → Precharging	
	L	H	H	L	X	X	BST	ILLEGAL	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	1
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	1
	L	L	L	H	X	X	REF/SREF	ILLEGAL	1
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	

ABBREVIATIONS: H = High level; L = Low level; X = Don’t care (high or low); V = Valid data input

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All input buffers except CKE will be disabled.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask preceding data which don’t satisfy t_{DPL}.
9. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8)
BA = Bank Address (BA_0-BA_1)
PA = Precharge All (A_8)
NOP = No Operation Command
CA = Column Address (A_0 - A_7)
AP = Auto Precharge (A_8)

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Operative Command Table (Part 4 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Action	Notes
Precharging	H	X	X	X	X	X	INHBT	NOP → Enter idle after t_{RP}	
	L	H	H	X	X	X	NOP	NOP → Enter idle after t_{RP}	
	L	H	H	L	X	X	BST	NOP → Enter idle after t_{RP}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	1
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	1
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	1
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	1
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREAL	NOP → Enter Idle after t_{RP}	1
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	Load Special Mode Register	
Row Activating	H	X	X	X	X	X	INHBT	NOP → Enter Row Active after t_{RCD}	
	L	H	H	X	X	X	NOP	NOP → Enter Row Active after t_{RCD}	
	L	H	H	L	X	X	BST	NOP → Enter Row Active after t_{RCD}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	1
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	1
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	1
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	1, 5
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	1, 5
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	1
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	Load Special Mode Register	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All input buffers except CKE will be disabled.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask preceding data which don't satisfy t_{DPL}.
9. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8)
BA = Bank Address (BA_0-BA_1)
PA = Precharge All (A_8)
NOP = No Operation Command
CA = Column Address (A_0 - A_7)
AP = Auto Precharge (A_8)

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Operative Command Table (Part 5 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Action	Notes
Write Recovering	H	X	X	X	X	X	INHBT	NOP → Enter Row Active after t_{WR}	
	L	H	H	X	X	X	NOP	NOP → Enter Row Active after t_{WR}	
	L	H	H	L	X	X	BST	NOP → Enter Row Active after t_{WR}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	Start Read, Determine AP	2
	L	H	L	L	L	BA, CA, AP	WR/WRA	New Write, Determine AP	
	L	H	L	L	H	BA, CA, AP	BW/BWA	New Block Write, Determine AP	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	1
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	1
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	Load Special Mask Register	
Write Recovering with Auto Precharge	H	X	X	X	X	X	INHBT	NOP → Enter Precharge after t_{WR}	
	L	H	H	X	X	X	NOP	NOP → Enter Precharge after t_{WR}	
	L	H	H	L	X	X	BST	NOP → Enter Precharge after t_{WR}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	1, 2
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	1
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	1
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	1
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	1
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	1
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All input buffers except CKE will be disabled.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask preceding data which don't satisfy t_{DPL}.
9. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8)
BA = Bank Address (BA_0-BA_1)
PA = Precharge All (A_8)
NOP = No Operation Command
CA = Column Address (A_0 - A_7)
AP = Auto Precharge (A_8)

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Operative Command Table (Part 6 of 6)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Action	Notes
Refreshing	H	X	X	X	X	X	INHBT	NOP → Enter idle after t_{RC}	
	L	H	H	X	X	X	NOP	NOP → Enter idle after t_{RC}	
	L	H	H	L	X	X	BST	NOP → Enter idle after t_{RC}	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	OP-CODE	LSMR	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	INHBT	NOP → Enter idle after two clocks	
	L	H	H	X	X	X	NOP	NOP → Enter idle after two clocks	
	L	H	H	L	X	X	BST	NOP → Enter idle after two clocks	
	L	H	L	H	X	BA, CA, AP	RD/RDA	ILLEGAL	
	L	H	L	L	L	BA, CA, AP	WR/WRA	ILLEGAL	
	L	H	L	L	H	BA, CA, AP	BW/BWA	ILLEGAL	
	L	L	H	H	L	BA, RA	ACT	ILLEGAL	
	L	L	H	H	H	BA, RA	ACTM	ILLEGAL	
	L	L	H	L	X	BA, PA	PRE/PREAL	ILLEGAL	
	L	L	L	H	X	X	REF/SREF	ILLEGAL	
	L	L	L	L	L	Op-Code	LMR	ILLEGAL	
	L	L	L	L	H	Op-Code	LSMR	ILLEGAL	

ABBREVIATIONS: H = High level; L = Low level; X = Don't care (high or low); V = Valid data input

NOTE: All entries assume that CKE was active (High level) during the preceding clock cycle.

1. Illegal to bank specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. If both banks are idle, and CKE is inactive (Low level), the device will enter Power Down Mode. All input buffers except CKE will be disabled.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self Refresh Mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RRD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must mask preceding data which don't satisfy t_{DPL}.
9. Illegal if t_{RCD} is not satisfied.

RA = Row Address (A_0 - A_8)
BA = Bank Address (BA_0-BA_1)
PA = Precharge All (A_8)
NOP = No Operation Command
CA = Column Address (A_0 - A_7)
AP = Auto Precharge (A_8)

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Function Truth Table

All inputs are latched on the rising edge of the clock, except the DQs and DMs which are latched at rising and falling edges of DQS.

Operation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DM	BA_0, BA_1	A_7	A_8	A_6-A_0	MNE	Notes
	n-1	n												
Device Deselect	H	X	H	X	X	X	X	X	X	X	X	X	INHBT	
	H	X	H	X	X	X	X	X	X	X	X	X		
No Operation	H	X	L	H	H	H	X	X	X	X	X	X	NOP	
Load Mode Register	H	X	L	L	L	L	L	X	OP CODE				LMR	1
Load Special Mode Register	H	X	L	L	L	L	H	X	OP CODE				LSMR	1, 5, 6
Row Activate	H	X	L	L	H	H	L	X	BS	Row Address			ACT	2
Row Activate w/WPB	H	X	L	L	H	H	H	X	BS	Row Address			ACTM	2
Read	H	X	L	H	L	H	X	X	BS	X	L	Col.	RD	3
Read w/ Auto Precharge	H	X	L	H	L	H	X	X	BS	X	H	Col.	RDA	3
Write Command	H	X	L	H	L	L	L	X	BS	X	L	Col.	WR	3, 7
Write w/ Auto Precharge	H	X	L	H	L	L	L	X	BS	X	H	Col.	WRA	3, 7
Block Write	H	X	L	H	L	L	H	X	BS	X	L	Col.	BW	4, 7, 8
Block Write w/ Auto Precharge	H	X	L	H	L	L	H	X	BS	X	H	Col.	BWA	4, 7, 8
Burst Termination	H	X	L	H	H	L	X	X	X	X	X	X	BST	
Precharge Single Bank	H	X	L	L	H	L	X	X	BS	X	L	X	PRE	
Precharge All Banks	H	X	L	L	H	L	X	X	X	X	H	X	PREAL	
Auto Refresh	H	H	L	L	L	H	X	X	X	X	X	X	REF	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	X	X	SREF(EN)	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	X	X	SREF(EX)	1
	L	H	L	H	H	H	X	X	X	X	X	X		
Power Down Mode (entry)	H	L	H	X	X	X	X	X	X	X	X	X	PDN-(EN)	
	H	L	L	H	H	H	X	X	X	X	X	X		
Power Down Mode (exit)	L	H	X	X	X	X	X	X	X	X	X	X	PDN-(EX)	

1. Should be issued only after both banks are deactivated (PREAL command).
2. Should be issued only after the corresponding bank has been deactivated (PRE command).
3. Should be issued after the corresponding bank has been activated (ACT command).
4. Use Mask Register data only after ACTM command. DM byte masking is active regardless of WPB mask.
5. Loading Mask Register: Initiate an LSMR cycle with address pin A_5=1 to load the Mask Register with the mask data present on the DQ pins on the following cycle. All other address pins must be "0".
6. Loading Color Register: Initiate an LSMR cycle with address pin A_6=1 to load the Color Register with the color input data on the DQ pins on the following cycle. All other address pins must be "0".
7. Any Write or Block Write cycles given to the selected bank/row while active will be masked according to the contents of the mask register, in addition to the DM signals and the column/byte mask information (the latter for Block Writes only).
8. Block Writes are not burst oriented and always apply to the 16 column locations selected by A_7-A_4.

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Function Truth Table for CKE

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
Self Refreshing	H	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	Exit Self Refresh (idle after t_{SREX})	1
	L	H	L	H	H	H	X	Exit Self Refresh (idle after t_{SREX})	1
	L	H	L	H	H	L	X	ILLEGAL	1
	L	H	L	H	L	X	X	ILLEGAL	1
	L	H	L	L	X	X	X	ILLEGAL	1
	L	L	X	X	X	X	X	NOP (maintain Self Refresh)	1
Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit power down (idle after t_{PDEX})	
	L	L	X	X	X	X	X	NOP (maintain power down)	
All Banks Idle	H	H	X	X	X	X	X	Refer to the Function Truth Table on page 28.	2
	H	L	L	L	L	H	X	Enter Self Refresh	2
	H	L	H	X	X	X	X	Exit Power Down	2
	H	L	L	H	H	H	X	Exit Power Down	2
	H	L	L	H	H	L	X	ILLEGAL	2
	H	L	L	H	L	X	X	ILLEGAL	2
	H	L	L	L	X	X	X	ILLEGAL	2
	L	X	X	X	X	X	X	Refer to Power Down in this table	2
Any state other than listed above	H	H	X	X	X	X	X	Refer to the Function Truth Table on page 28.	

ABBREVIATIONS:
H=High Level; L=Low Level; X=Don't Care

NOTES:
1. CKE low-to-high transition re-enables CLK and other inputs asynchronously. A minimum setup time must be satisfied before any commands other than EXIT are executed.
2. Power Down and Self Refresh can be entered only from the All Bank Idle state.

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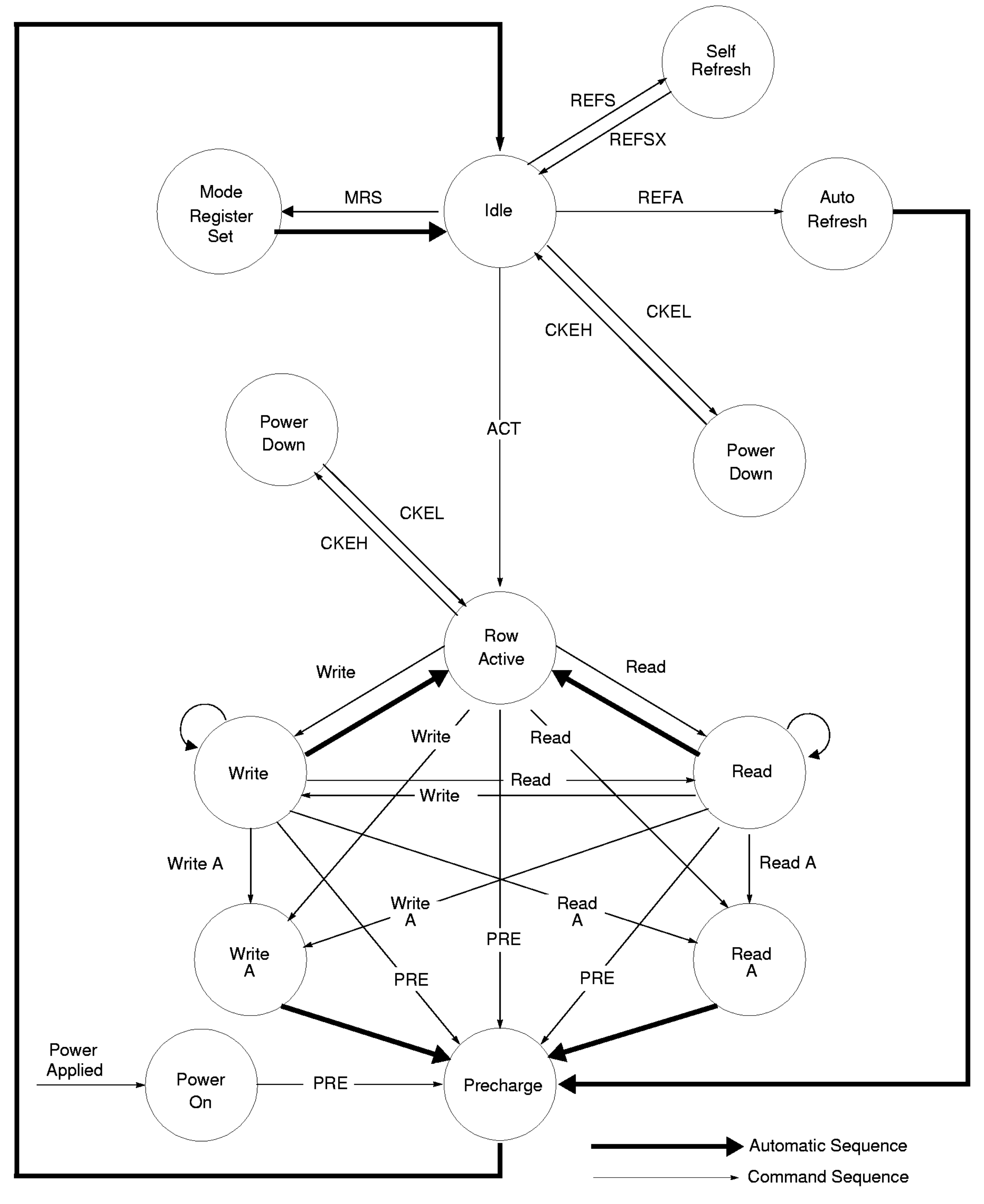
Simplified State Diagram



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Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-1.0 to 4.6	V
V_{DD}, V_{DDQ}	Voltage on V_{DD} supply relative to V_{SS}	-1.0 to 4.6	V
T_{STG}	Storage Temperature	-55 to +150	°C
P_D	Power Dissipation	13.2	W
I_{OUT}	Short Circuit Current	50	mA

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

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Stub Series Terminated Logic (SSTL_2)

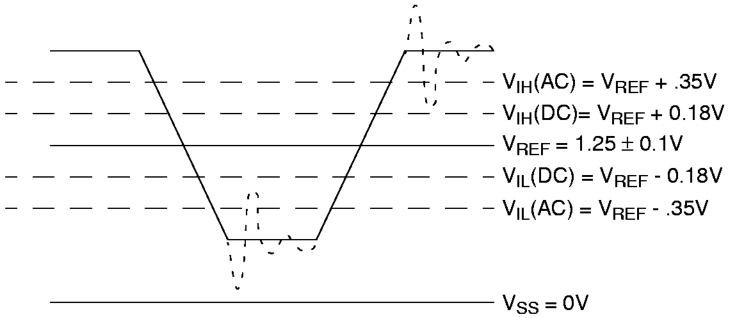
DC Input Levels

SSTL_2 DC input levels reduce the effects of ringing and define the final logic state unambiguously. Once a receiver input has crossed a DC level, it will change and maintain the new state.

AC Input Levels

SSTL_2 AC input levels must be met for the receiver to meet the timing specifications.

SSTL_2 Input Levels (V_{DDQ}=2.5V)



SSTL_2 Supply Voltage Levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Device Supply Voltage	V_{DDQ}	No Requirement		V	
V_{DDQ}	Output Supply Voltage	2.3	2.5	2.7	V	1
V_{REF}	Input Reference Voltage	1.15	1.25	1.35	V	2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. Peak to peak AC noise on V_{REF} may not exceed ±2% V_{REF} (DC). V_{REF} is also expected to track noise variations in V_{DDQ}.
3. V_{TT} of the transmitting device must track V_{REF} of the receiving device.

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SSTL_2 Input AC/DC Logic Levels

Symbol	Parameter	Min	Max	Units	Notes
V_{IH} (DC)	DC Input Logic High	V_{REF}+0.18	V_{DDQ}+0.3	V	1
V_{IH} (AC)	AC Input Logic High	V_{REF}+0.35	—	V	
V_{IL} (DC)	DC Input Logic Low	-0.30	V_{REF}-0.18	V	
V_{IL} (AC)	AC Input Logic Low	—	V_{REF}-0.35	V	

1. The relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of V_{IH} (max) (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (e.g., a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0V (High corner V_{DDQ}+300mV).

SSTL_2 AC Test Conditions

Symbol	Parameter	Value	Units	Notes
V_{REF}	Input Reference Voltage	0.5*V_{DDQ}	V	1
V_{SWING} (max)	Input Signal Maximum Peak to Peak Swing	1.5	V	1, 2
SLEW	Input Signal Minimum Slew Rate	1.0	V/ns	3

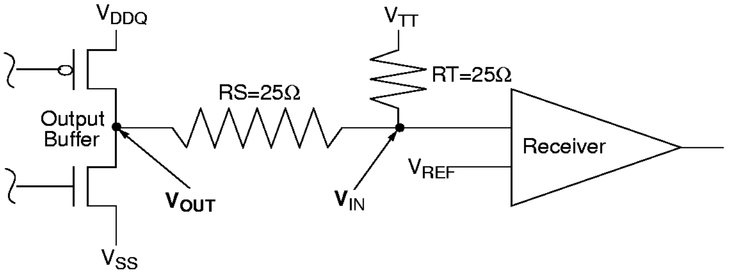
1. Input waveform timing is referenced to the input signal crossing the V_{REF} level applied to the device.
2. Compliant devices must still meet the V_{IH} (AC) and V_{IL} (AC) specifications under actual use conditions.
3. The 1V/ns input signal minimum slew rate is to be maintained in the V_{IL} max (AC) to V_{IL} min (AC) range of the input signal swing.

SSTL_2 Output Buffers

The input voltage provided to the receiver depends on three parameters:

- V_{DDQ} and current drive capabilities of the output buffer
- Termination voltage
- Termination resistance

Class II SSTL_2 Output Buffer (Driver)



Note:
V_{IN} must be at least 380mV above or below V_{REF} as a result of V_{OUT} attaining its maximum low or its minimum high value.
I_{RT} = 15.2mA (for V_{REF} ±.38)

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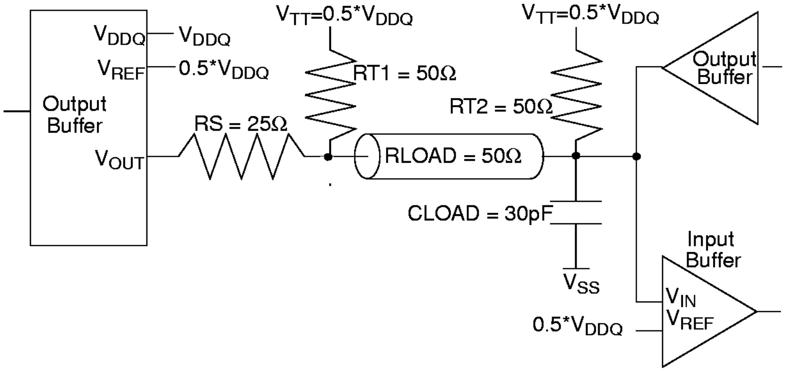
SSTL_2 Output Buffer Characteristics

Symbol	Parameter	Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.76	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} – 0.76	V	
V_{OTR}	Input Signal Minimum Slew Rate	0.5*V_{DDQ}	V	2
I_{OH}	Output Minimum Source DC Current	-15.2	mA	3, 4
I_{OL}	Output Minimum Sink DC Current	15.2	mA	4, 5
RT	Termination Resistor	25	Ω	
RS	Series Resistor	25	Ω	

1. Since V_{IN} must be at least 0.38V above or below V_{REF} as a result of V_{OUT}, using a series resistor of 25Ω for a Class II output driver results in a minimum requirement of a 0.76V swing relative to V_{TT}.
2. The V_{DDQ} of the device under test is referenced.
3. V_{DDQ} = 2.3V; V_{OUT} = V_{DDQ} – .43V.
4. The DC value of V_{REF} applied to the receiving device is expected to be set to V_{TT}.
5. V_{DDQ} = 2.3V; V_{OUT} = 0.35V.

SSTL_2 Class II Push-Pull Output Buffer

Designed for symmetrically double parallel terminated loads with series resistor for DQs.



AC Characteristics (T$_A$=0 to +70°C, V$_{CC}$=3.3 ± 0.3V)

Symbol	Parameter		-6R7		-8		-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CK}	Clock Period	CL=1.5	13.4		16		20		
		CL=2	10		12		15		
		CL=2.5	8.4		10		12.8		
		CL=3	6.7		8		10		
t_{RC}	Row Cycle Time	Operation	60		70		90		ns
t_{RFC}		Auto Refresh	60		80		90		ns
t_{RAS}	Row Active Time		40	100K	48	100K	60	100K	ns
t_{RCD}	RAS to CAS Delay		20		24		30		ns
t_{RP}	Row Precharge Time		20		24		30		ns
t_{RRD}	Row Activate to Row Activate Delay		1		1		1		CLK
t_{WR}	Last Data in to Row Precharge		.5		.5		.5		CLK
t_{CDLR}	Last Data in to Read Command Delay		.5	1	.5	1	.5	1	CLK
t_{CCD}	Col. Address to Col. Address Delay		1		1		1		CLK
t_{CH}	CLK High Level Width		0.4	0.6	0.4	0.6	0.4	0.6	CLK
t_{CL}	CLK Low Level Width		0.4	0.6	0.4	0.6	0.4	0.6	CLK
t_{DQCK}	Output Data Edge to Clock Edge		-0.7	+0.7	-0.8	+0.8	-1	+1	ns
t_{DQSCK}	Data Strobe Edge to Clock Edge		-0.7	+0.7	-0.8	+0.8	-1	+1	ns
t_{DQSO}	Data Strobe Edge to Output Data Edge		-0.5	+0.5	-0.6	+0.6	-0.75	+0.75	ns
t_{DQSI}	Data Strobe Edge to Input Data Edge		-0.1	+0.1	-0.1	+0.1	-0.1	+0.1	CLK
t_{DM}	Data Strobe Edge to Data Mask Edge		-0.1	+0.1	-0.1	+0.1	-0.1	+0.1	CLK
t_{DQV}	Input Data Valid time		0.25	—	0.25	—	0.25	—	CLK
t_{DMV}	Data Mask Valid time		0.25	—	0.25	—	0.25	—	CLK
t_{SLZ}	DQS Low-Z to Valid DQS Delay		tCK/2-1ns	tCK/2+1ns	tCK/2-1ns	tCK/2+1ns	tCK/2-1ns	tCK/2+1ns	ns
t_{SHZ}	Valid DQS to DQS High-Z Delay		tCK/2-1ns	tCK/2+1ns	tCK/2-1ns	tCK/2+1ns	tCK/2-1ns	tCK/2+1ns	ns
t_{HZQ}	Data Out Active to High-Z		3		3		3		ns
t_{DSS}	CLK to Valid DQS-In		.75	1.25	.75	1.25	.75	1.25	CLK
t_{SIH}	DQS-In High Level Width		0.4	0.6	0.4	0.6	0.4	0.6	CLK
t_{SIL}	DQS-In Low Level Width		0.4	0.6	0.4	0.6	0.4	0.6	CLK
t_{SIC}	DQS-In Cycle Time		1		1		1		CLK
t_{IS}	Input Setup Time		.15		.15		.15		CLK
t_{IH}	Input Hold Time		.15		.15		.15		CLK
t_{MRD}	Mode Register Set Cycle Time		2		2		2		CLK
t_{PDEX}	Power Down Exit Time		10		10		10		ns
t_{SREX}	Self Refresh Exit Time		200		200		200		Cycles
t_{BWC}	Block Write Cycle Time		2		2		2		CLK
t_T	CLK Transition Time		0.5		0.5		0.5		ns
t_{LZ}	Clock to Output in Low-Z		TBD	TBD	TBD	TBD	TBD	TBD	
t_{HZ}	Clock to Output in High-Z		3	—	4	—	5	—	

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DC Electrical Characteristics (T_A = 0 to +70°C)

Symbol	Parameter	$\overline{CAS}$ Latency	Version	Rating	Units	Notes
I_{CC1}	Operating Current (One Bank Active) Burst length=4; $t_{RC} \geq t_{RC}$(min); I_{OL}=0mA	1.5	-6R7	TBD	mA	1
		2	-8	TBD		
		2.5	-8	TBD		
		3	-10	125		
$I_{CC2}P$	Precharge Standby Current in Power Down Mode CKE $\leq V_{IL}$(max); t_{CK}=t_{CK}(min)		-6R7	TBD	mA	
			-8	TBD		
			-10	20		
$I_{CC2}N$	Precharge Standby Current in Non Power Down Mode CKE $\geq V_{IH}$(min); $\overline{CS} \geq V_{IH}$(min); t_{CK}=t_{CK}(min) Input signals are changed once per three clock cycles --		-6R7	TBD	mA	
			-8	TBD		
			-10	45		
$I_{CC3}P$	Active Standby Current in Power Down Mode CKE $\leq V_{IL}$(max); t_{CK}=t_{CK}(min)		-6R7	TBD	mA	
			-8	TBD		
			-10	30		
$I_{CC3}N$	Active Standby Current in Non Power Down Mode CKE $\geq V_{IH}$(min); $\overline{CS} \geq V_{IH}$(min); t_{CK}=t_{CK}(min) Input signals are changed once per three clock cycles		-6R7	TBD	mA	
			-8	TBD		
			-10	60		
I_{CC4}	Operating Current (Burst Mode) All Banks Activated; I_{OL}=0mA; t_{CCD}=2CLKs	1.5	-6R7	TBD	mA	1, 3
			-8	TBD		
			-10	180		
		2	-6R7	TBD		
			-8	TBD		
			-10	TBD		
		2.5	-6R7	TBD		
			-8	TBD		
			-10	TBD		
		3	-6R7	TBD		
			-8	TBD		
			-10	TBD		
I_{CC5}	Refresh Current $t_{RC} \geq t_{RC}$(min)	--	-6R7	TBD	mA	2
			-8	TBD		
			-10	210		
I_{CC6}	Self-Refresh Current CKE $\leq$ 0.2V	--	-6R7	2	mA	2
			-8	2		
			-10	2		
I_{CC7}	Operating Current (Block Write) t_{CK} = t_{CK}(min) t_{BWC} = t_{BWC}(min)	--	-6R7	TBD	mA	4, 5
			-8	TBD		
			-10	TBD		

1. Measured with outputs open.
2. Refresh period is 16ms.
3. Addresses are changed only one time during t_{CK}(min).
4. Addresses are changed only one time during t_{BWC}(min).
5. Specified for SGRAMs only.

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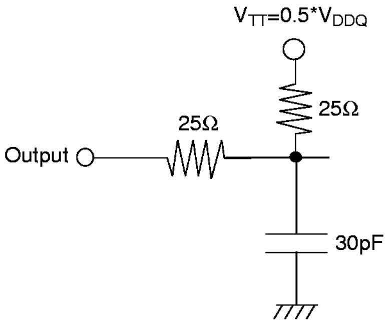
AC Operating Test Conditions (V_{DD}=3.3V ± 0.3V, T_A = 0 to +70°C)

Parameter	Value	Units
Input Reference Voltage for CLK	0.5*V_{DDQ}	V
CLK Signal Maximum Peak Swing	2.0	V
CLK Signal Minimum Slew Rate	1.0	V/ns
CLK Input Levels (V_{IH}/V_{IL})	V_{REF}+0.4 / V_{REF}-0.4	V
Output Timing Measurement Reference Level	V_{TT}	V
Output Load Condition	See AC Output Load Circuit figure below	
Input level (V_{IH}/V_{IL}) — SSTL_2	2.4 / 0.4	V
Input Timing Measurement Reference Level — V_{REF}	1.5	V

AC Output Load Circuit



Capacitance (V_{DD}=3.3V ± 0.3V, T_A = 0 to +70°C)

Parameter	Symbol	Min.	Max.	Units
Input Capacitance (A_0-A_8, BA_0-BA_1)	C_{IN1}	2.5	5	pF
Input Capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	2.5	4	pF
Data & DQs Input/Output Capacitance	C_{OUT}	4	6.5	pF
Input Capacitance (DM)	C_{IN3}	4	6.5	pF

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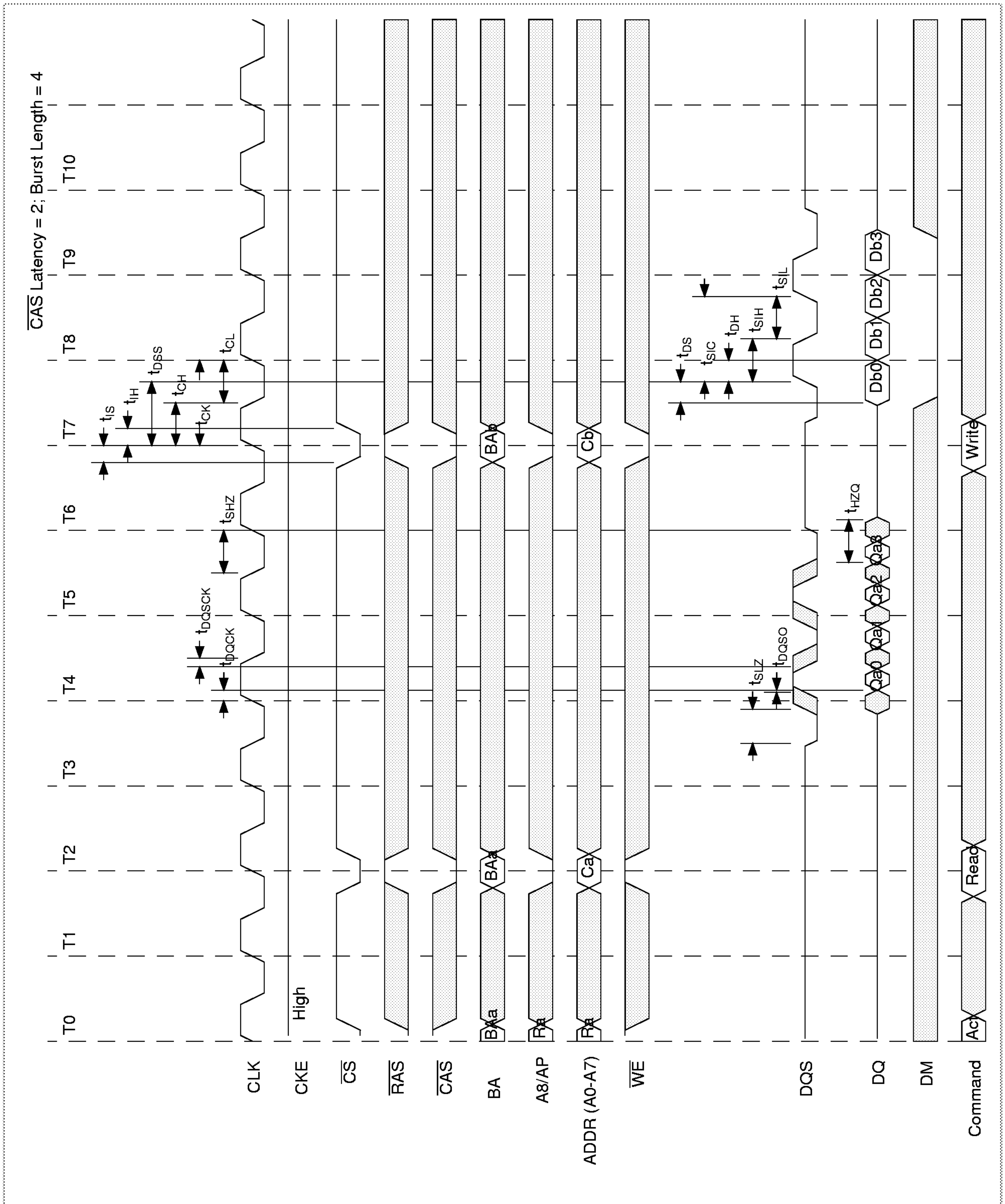
Basic Timing: Setup, Hold, and Access Times



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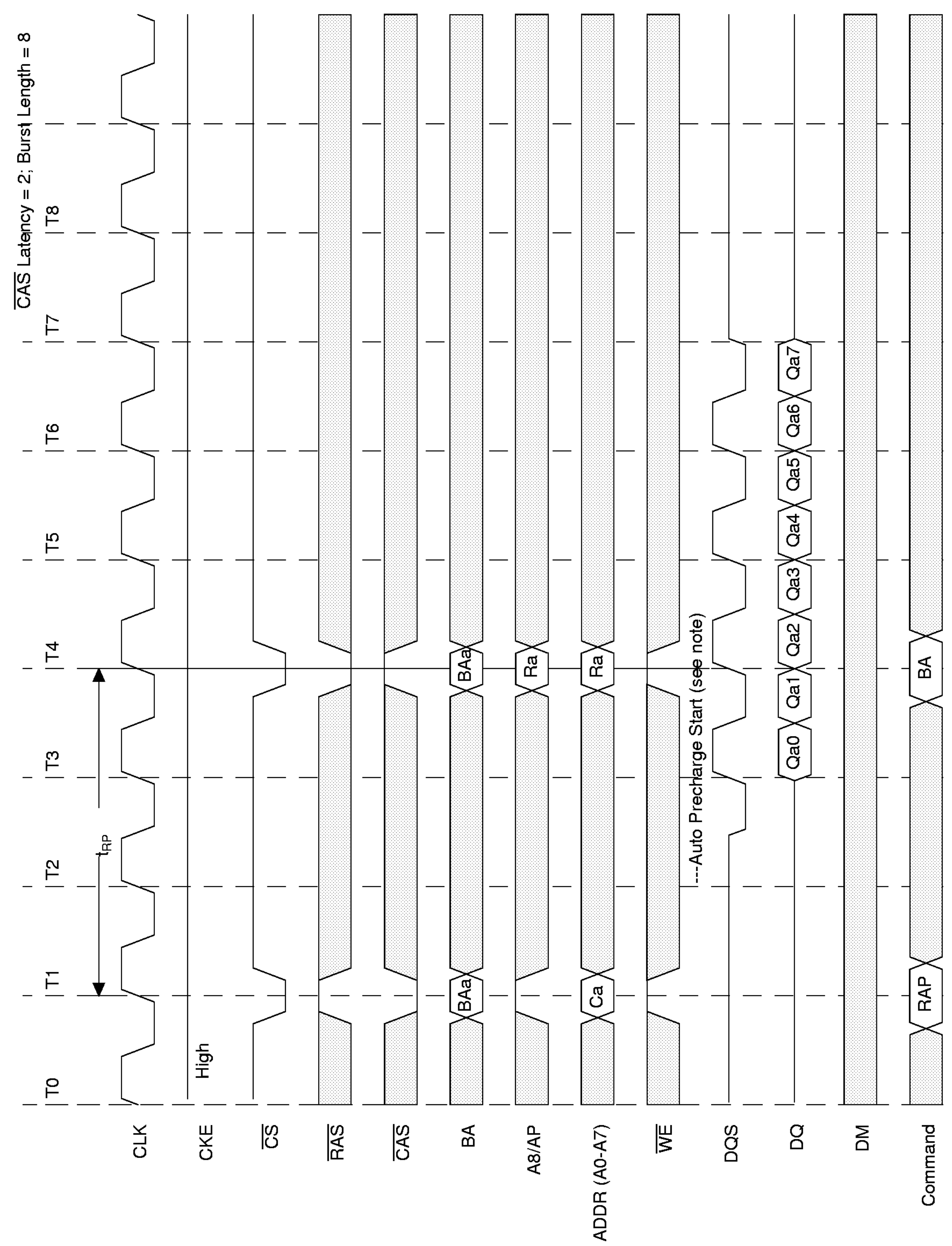
Auto Precharge After Read Burst



$\overline{\text{CAS}}$ Latency = 2; Burst Length = 8

Note: The Row Activate command of the precharged bank can be issued from this point. The new Read or Write command of another activated bank can be issued from this point. At Burst Read or Write with Auto Precharge, $\overline{\text{CAS}}$ interrupt of the same/another bank is illegal.

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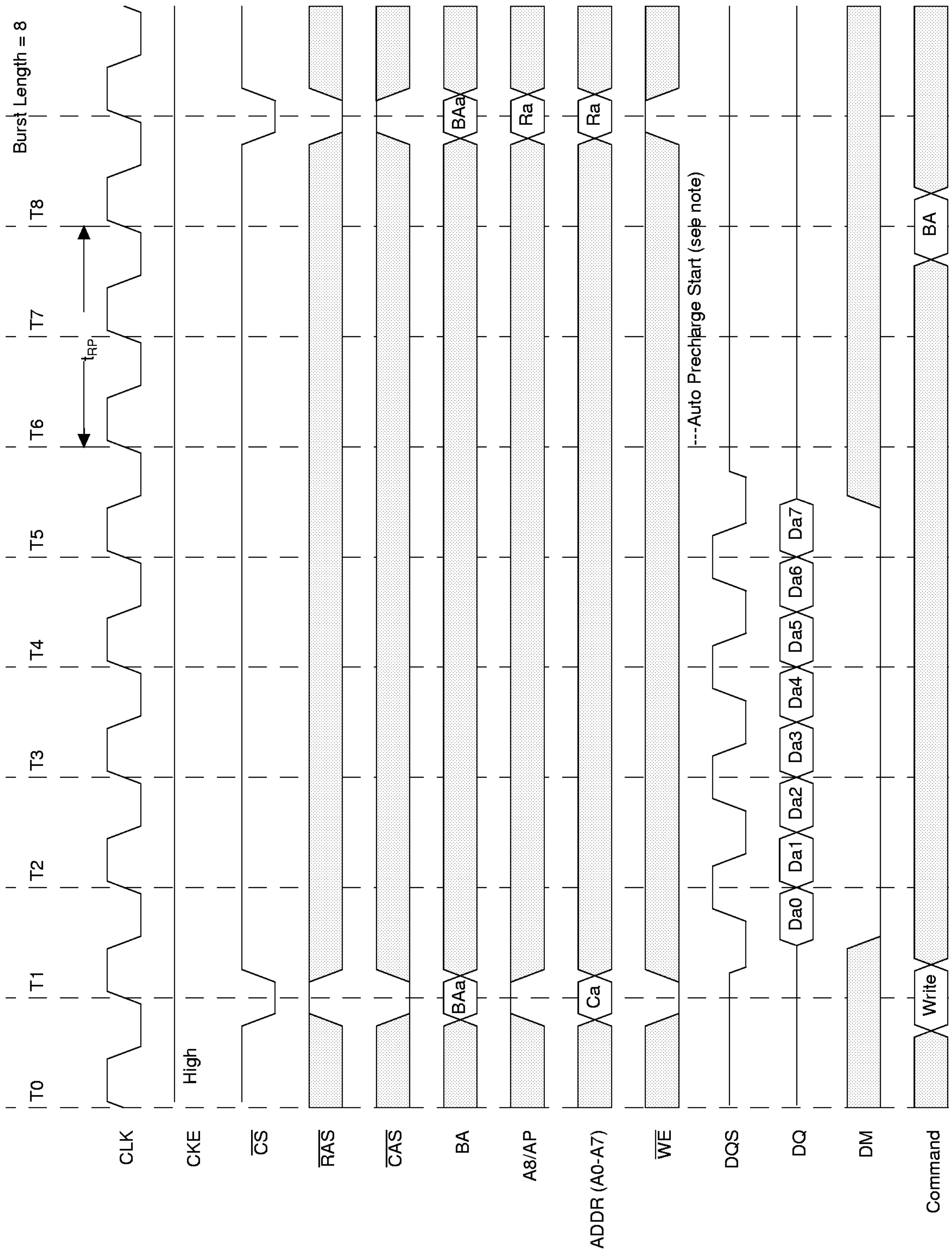
Auto Precharge After Write Burst



Note: The Row Active command of the precharged bank can be issued after t_{RP} from this point. The new Read or Write command of another activated bank can be issued from this point. At Burst Read or Write with Auto Precharge, $\overline{CAS}$ interrupt of the same/another bank is illegal.

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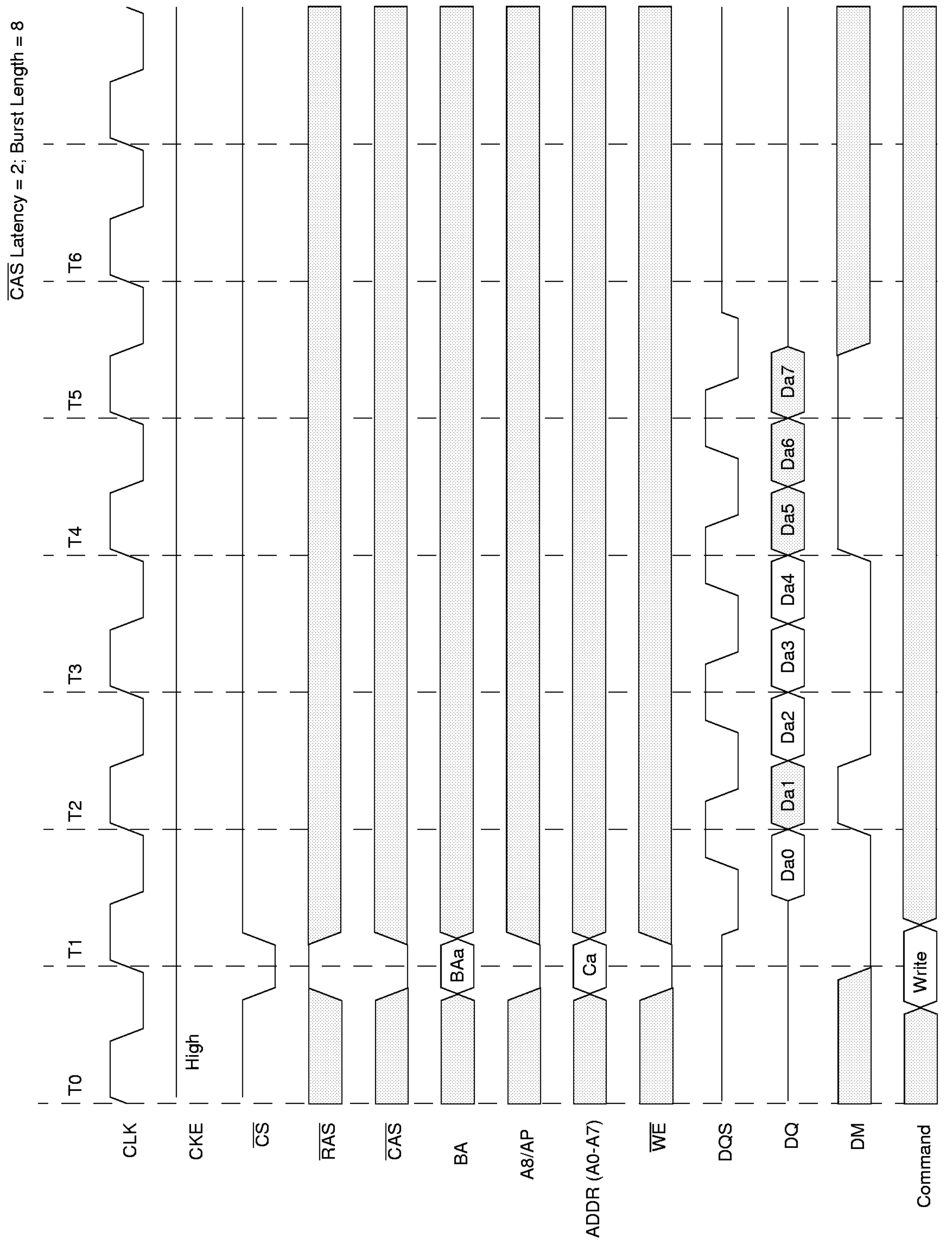
Data Mask Function Only for Write



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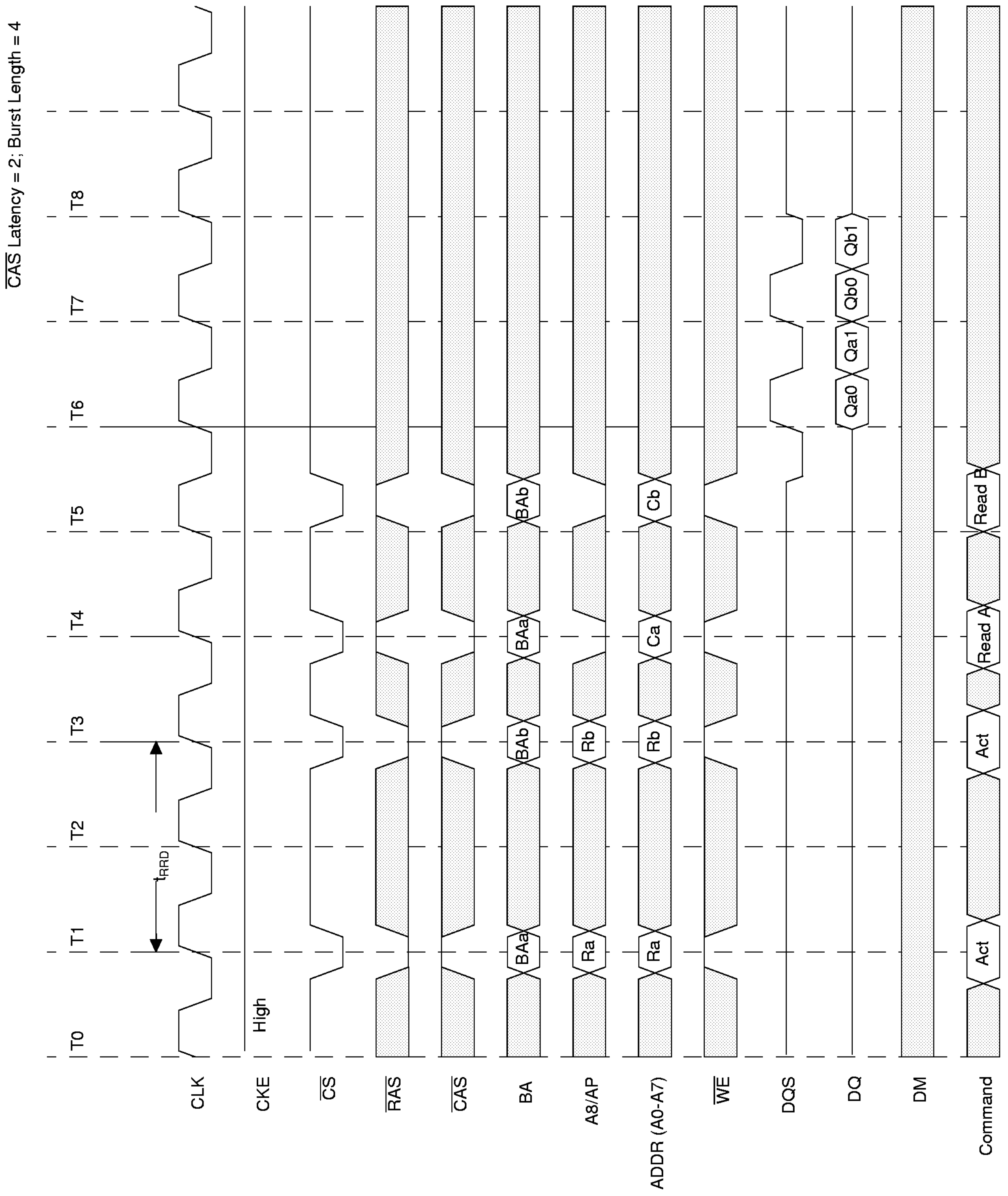
Multibank Interleaving Read



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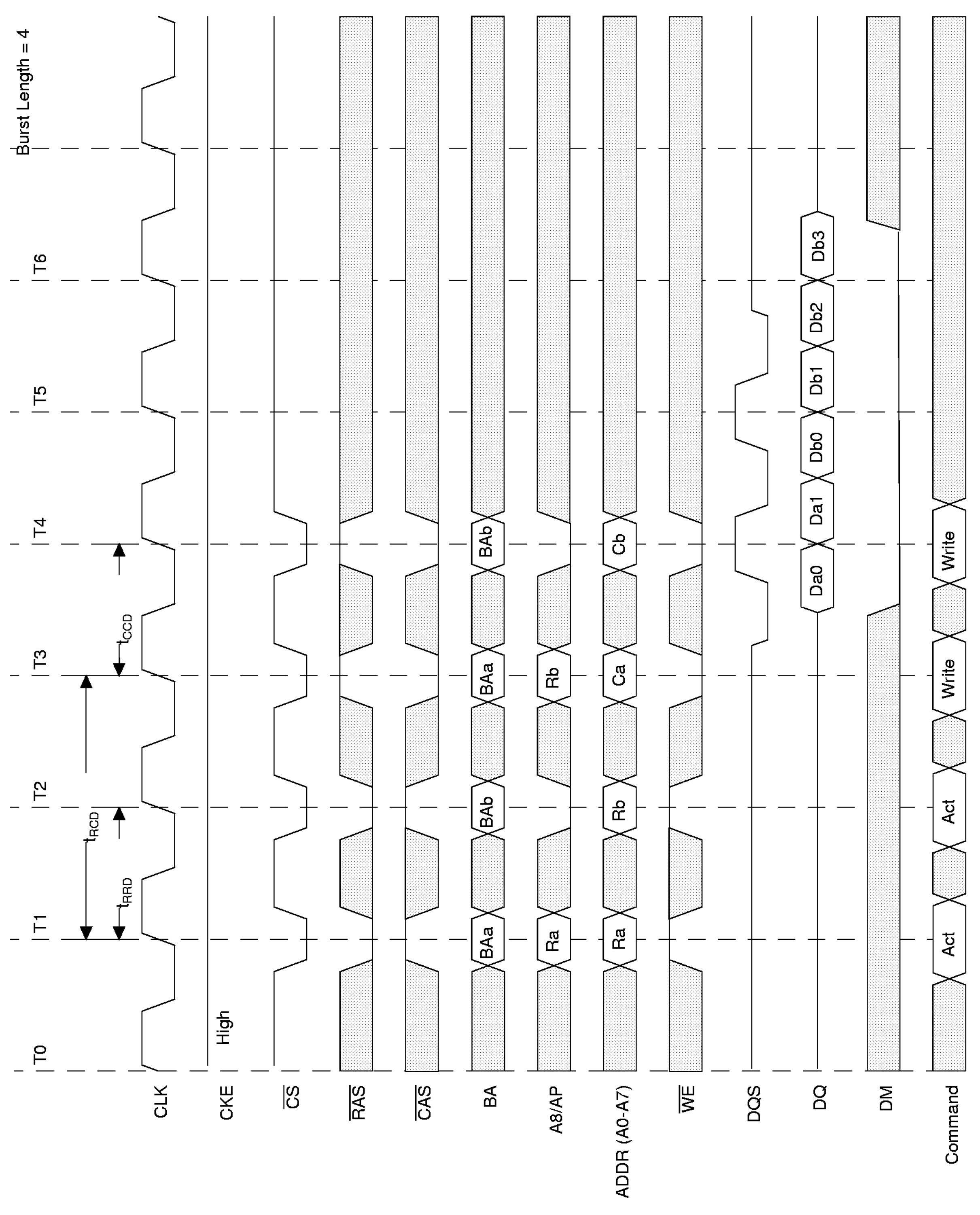
Multibank Interleaving Write



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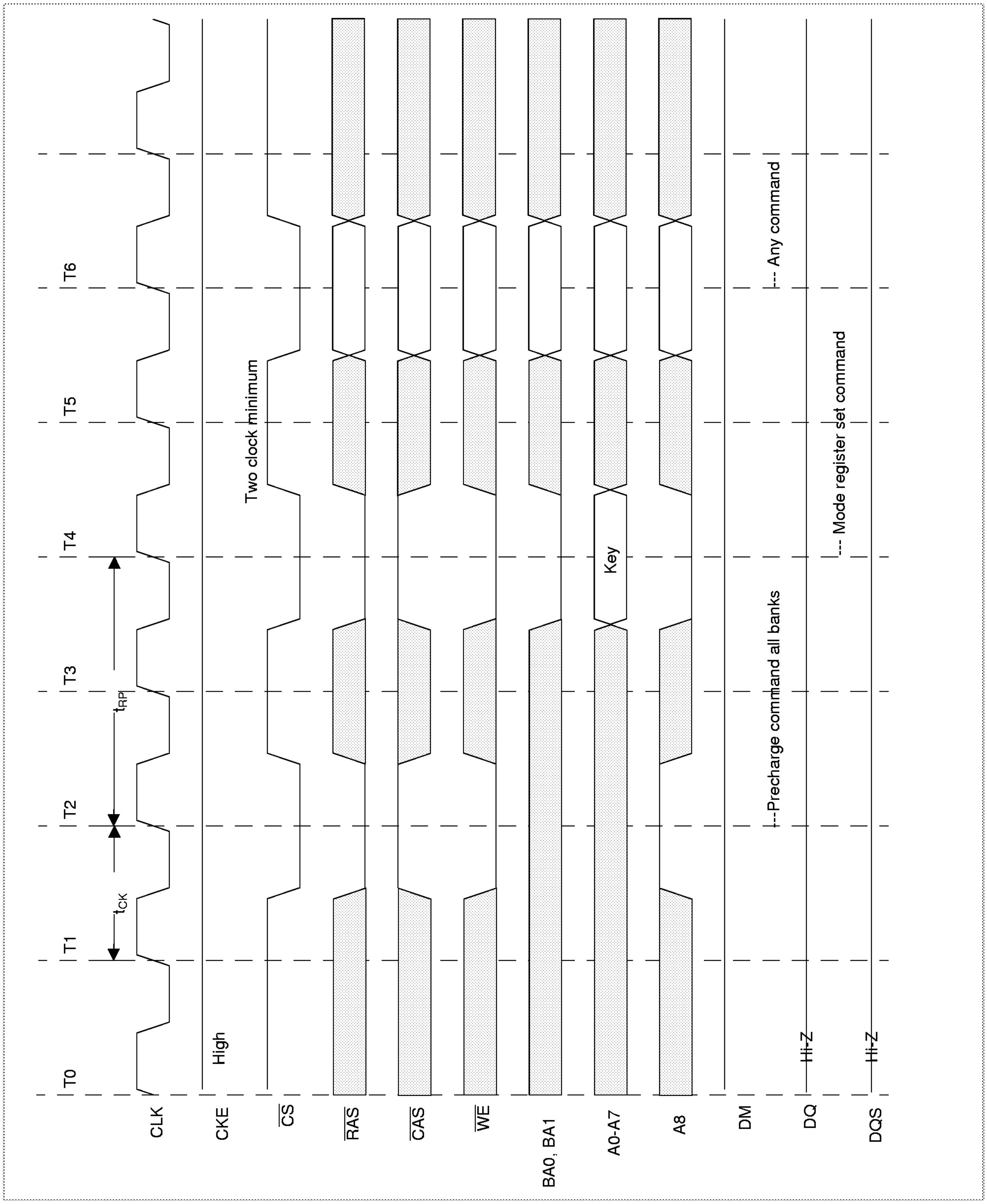
Mode Register Set



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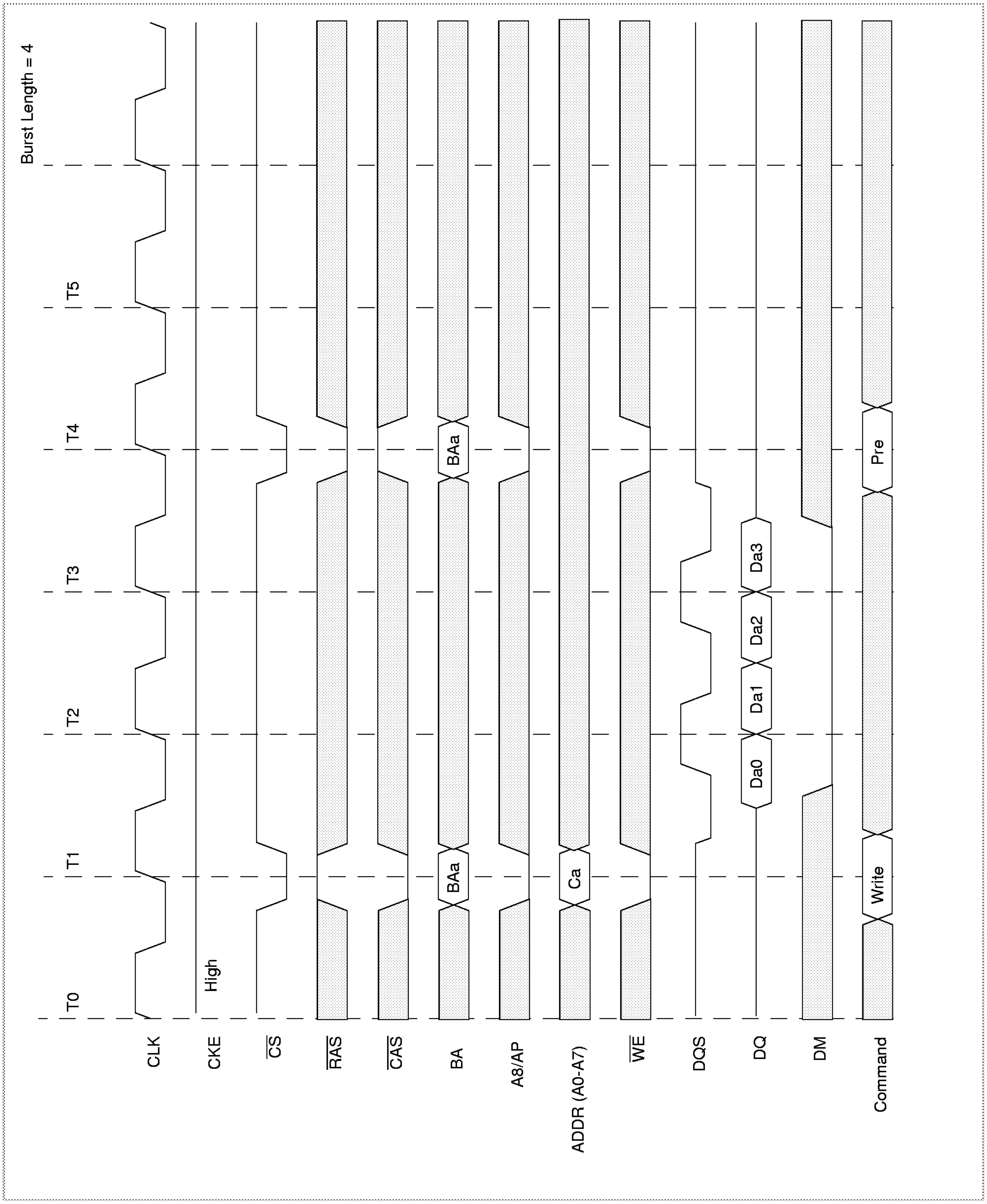
Write Burst



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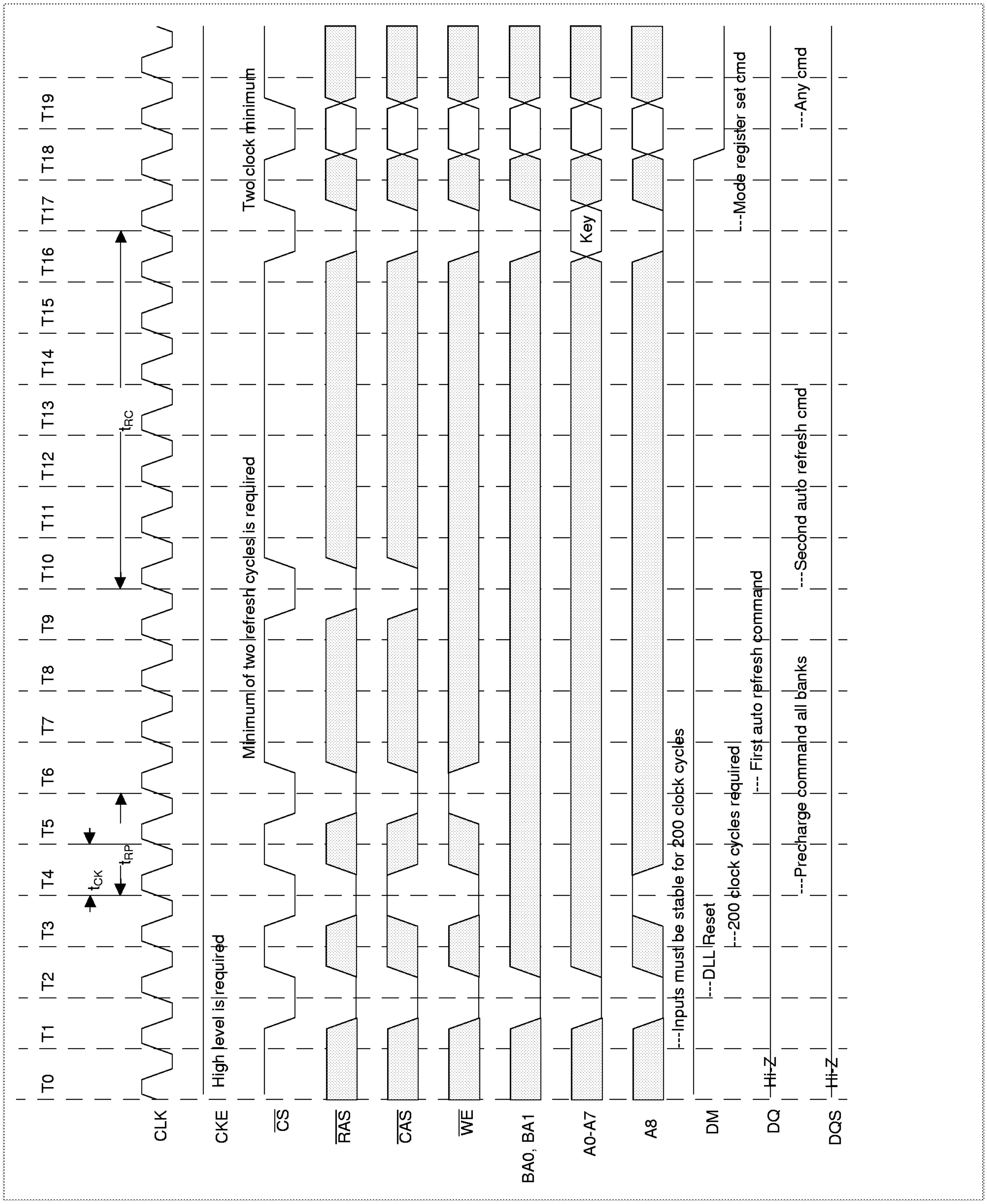
Power Up Sequence and Auto Refresh (CBR)



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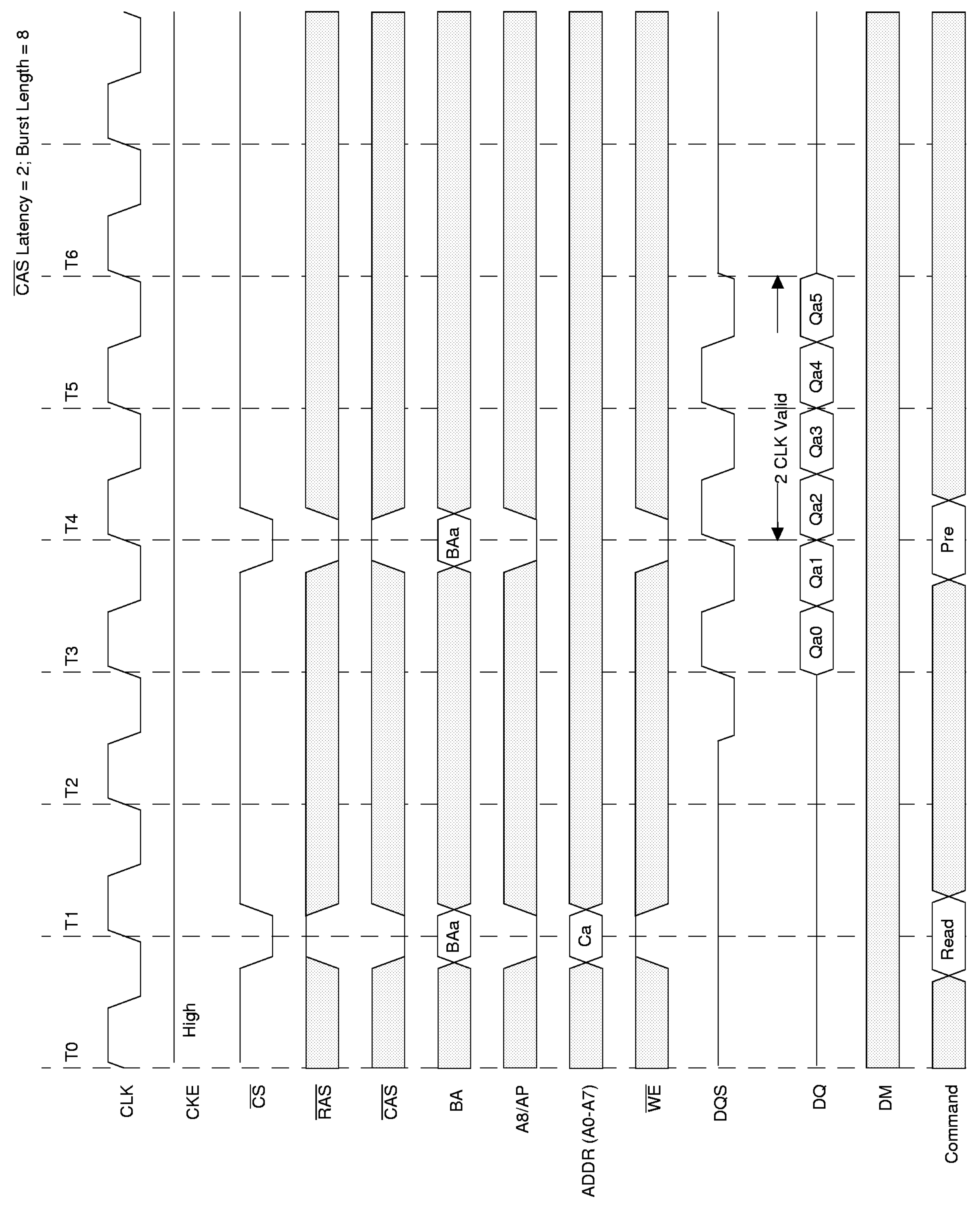
Read Interrupted by a Precharge



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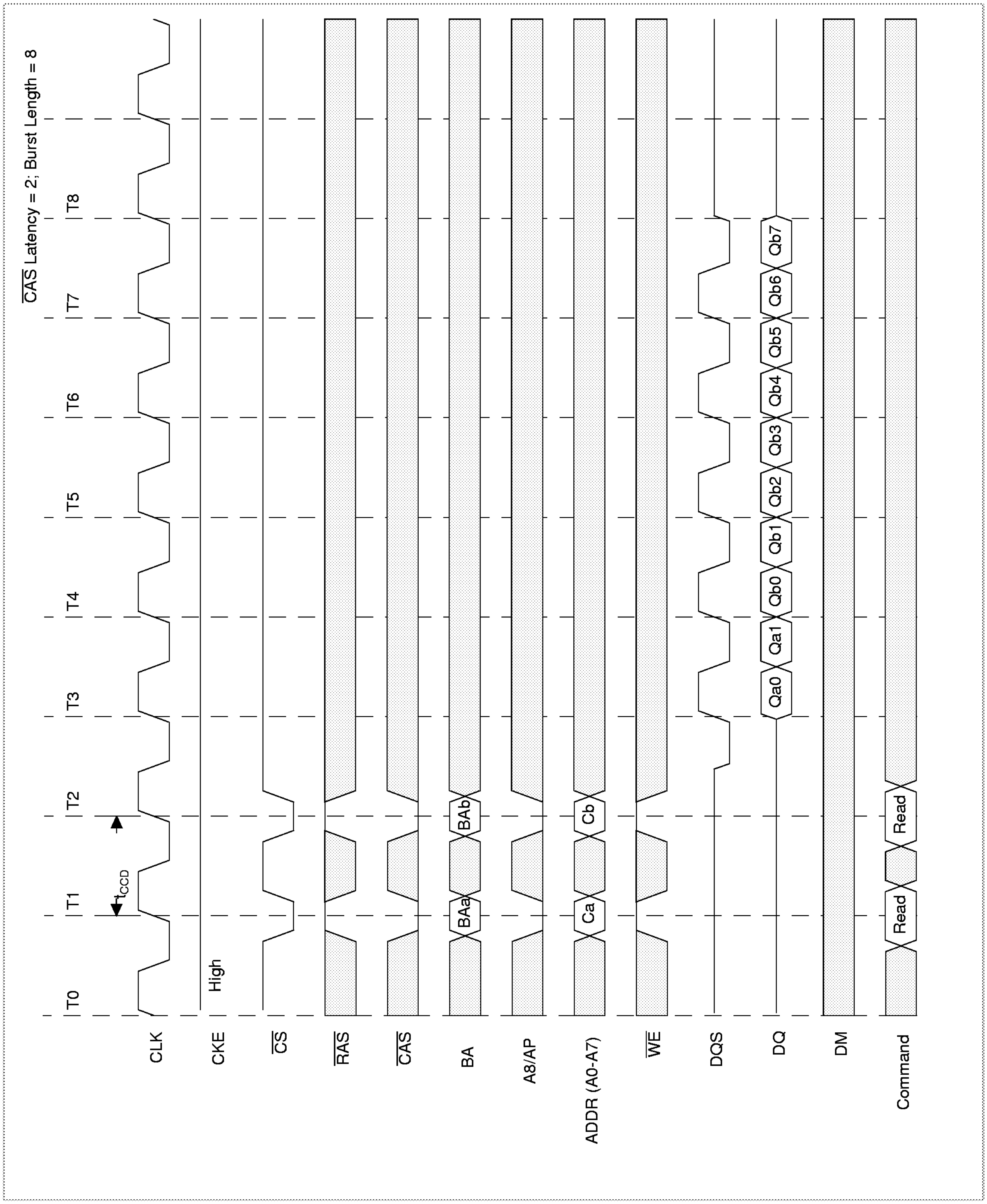
Read Interrupted by a Read



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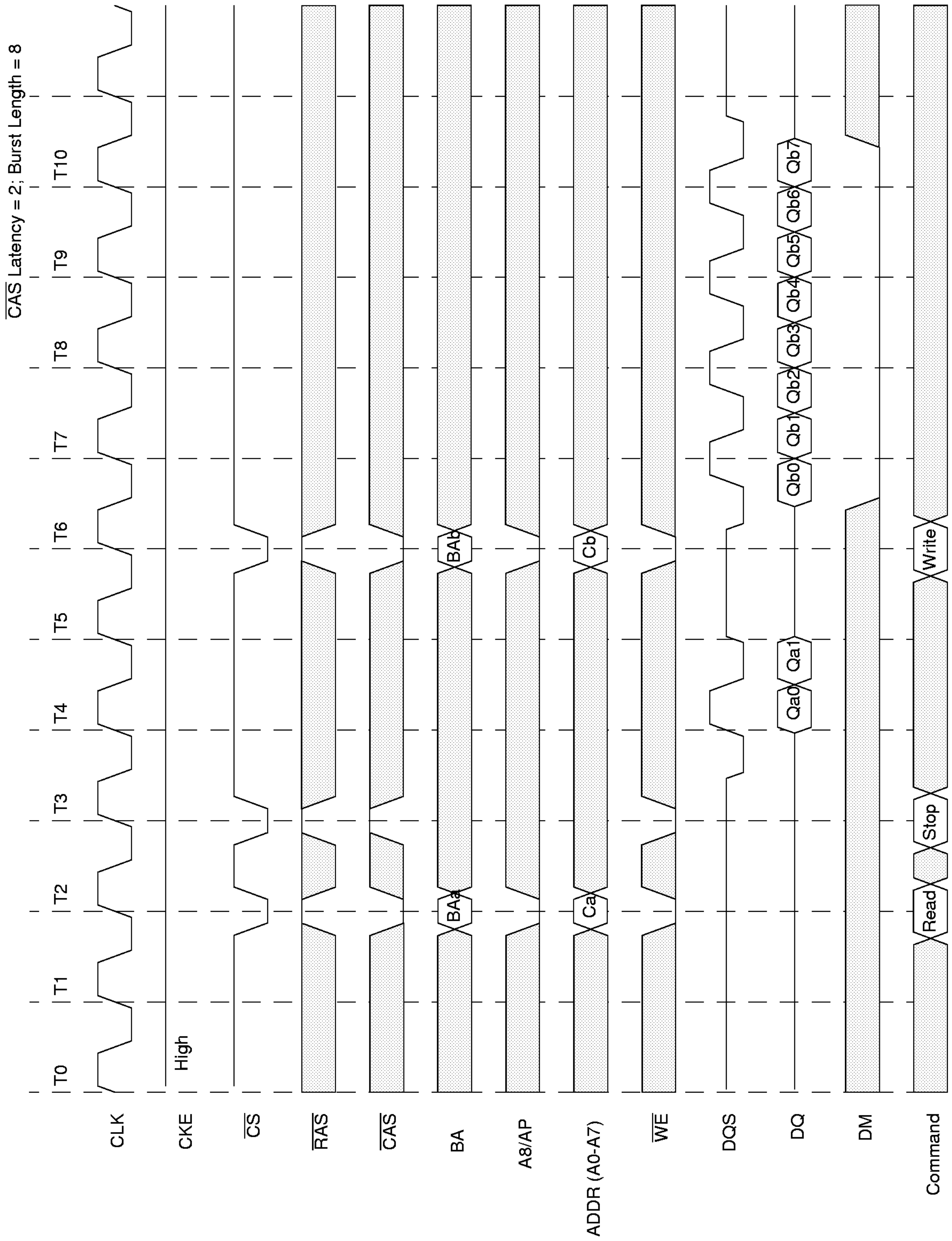
Read Interrupted by a Write and Burst Stop



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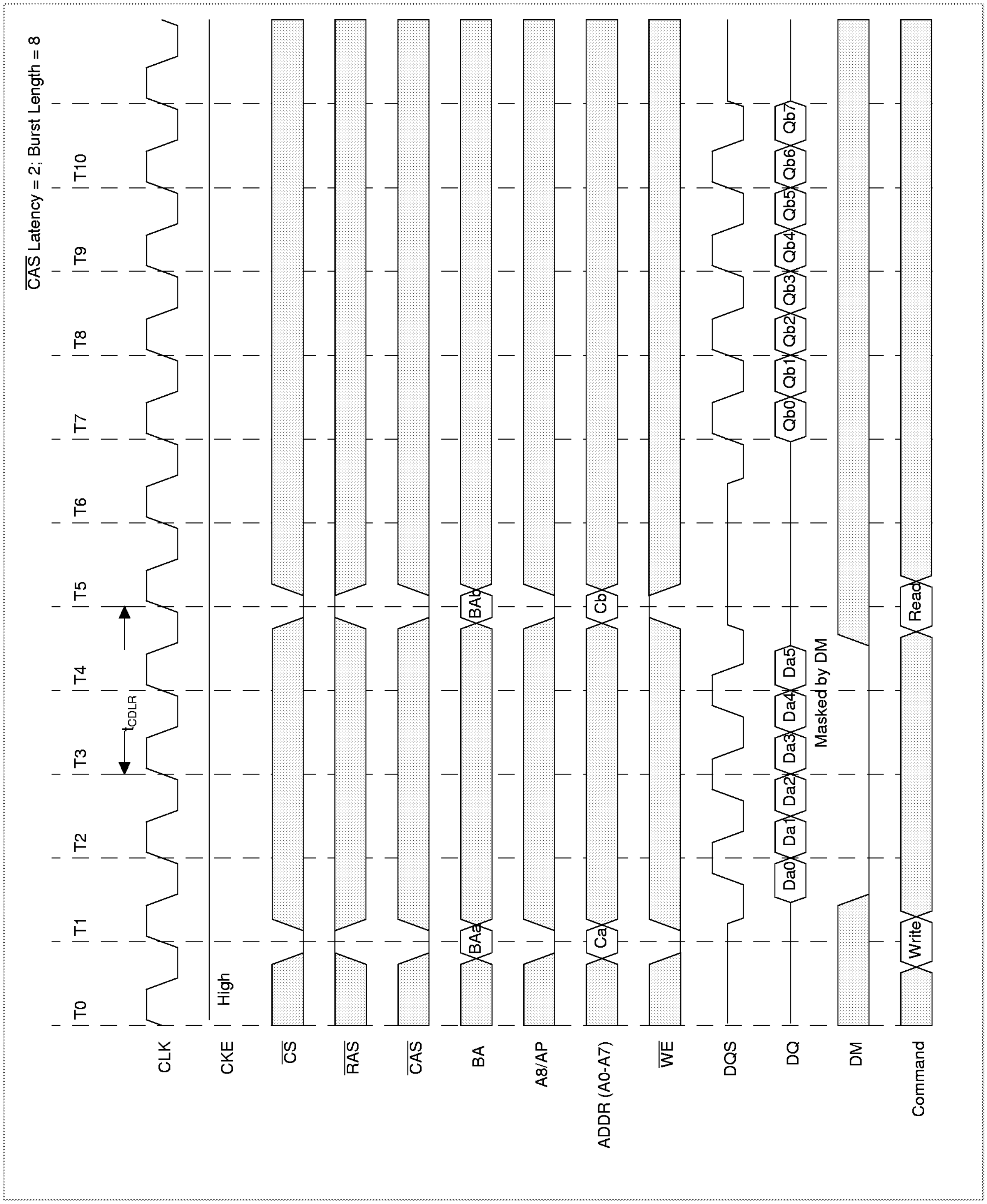
Write Interrupted by a Read



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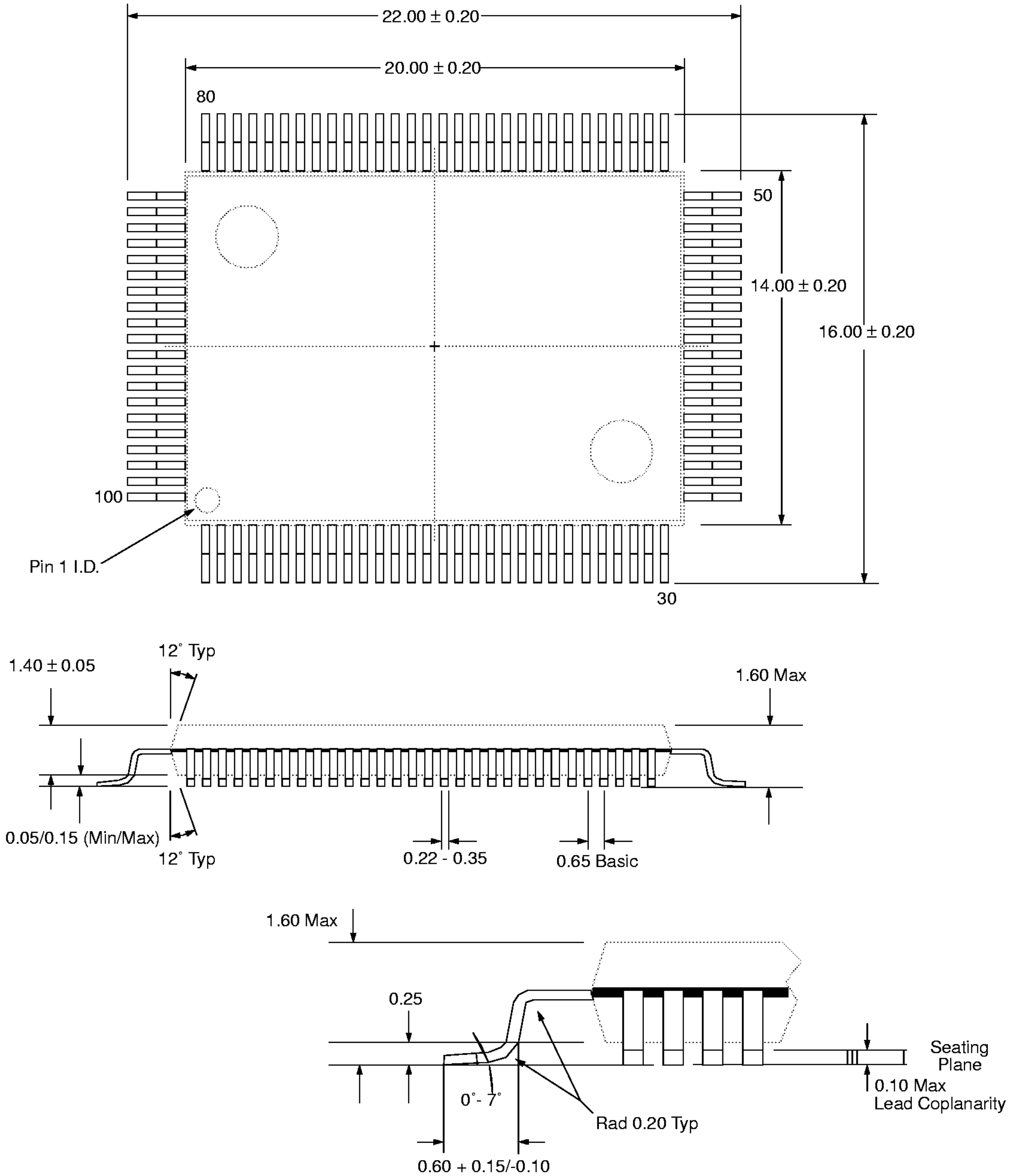
Package Diagram (LQFP)



All dimensions in millimeters
Conforms to JEDEC MS-026/Variation BHA

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Revision Log

Rev	Contents of Modification
12/97	Initial publication.

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