Features

- Low Power CMOS Operation
  - 100 μA max. Standby
  - 30 mA max. Active at 5 MHz
- Fast Read Access Time - 120ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP
  - 32-Pad OTP PLCC
- 5V± 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
- Fast Programming - 4ms/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

128K (16K x 8) UV Erasable CMOS EPROM

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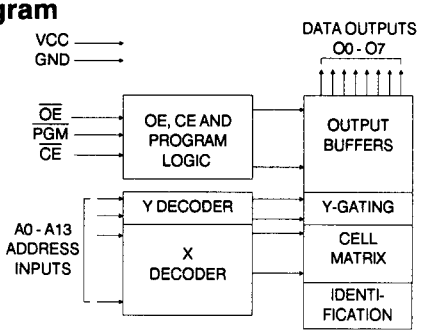
Block Diagram



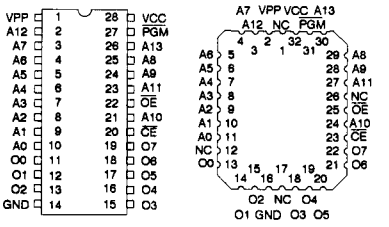
Description

The AT27C128 chip is a low-power, high performance 131,072 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 16K x 8. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

Atmel's 1.5 micron CMOS technology provides optimum speed, low power and high noise immunity. Power consumption is typically only 10mA in Active Mode and less than 10μA in Standby. In addition to the speed, power and reliability advantages of the CMOS process, the CMOS technology is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

Pin Configurations

Pin Name	Function
A0-A13	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect



Note: PLCC package Pins 1 and 17 are DON'T CONNECT

Description (Continued)

The AT27C128 comes in a choice of industry standard JEDEC-approved packages including; 32-pin DIP in ceramic or one time programmable (OTP) plastic, and 32-pin OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 16K byte storage capability, the AT27C128 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C128 has additional features to ensure high quality and efficient production use. The Fast Programming Algorithm reduces the time required to program the part and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C128 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15 W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 $w \cdot sec/cm^2$

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	Ai	X(1)	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9 = V_H (3) A0 = V_{IH} or V_{IL} A1-A13 = V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming Characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code Byte.
5. Standby V_{CC} current (I_{SB}) is specified with $V_{PP}=V_{CC}$. $V_{CC} > V_{PP}$ will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C128			
		-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC} + 0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind.,Mil.		40	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -400µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

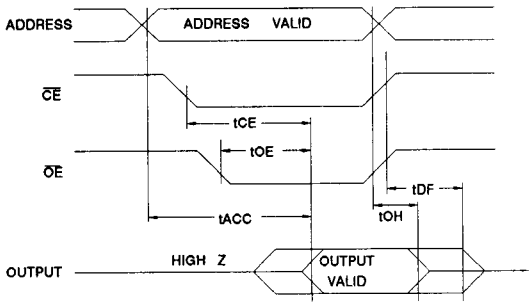
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C128								
				-12		-15		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		120		150		200		250	ns
			Ind.		120		150		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			120		150		200		250	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			60		70		75		100	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}			50		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			0		0		0		0	ns

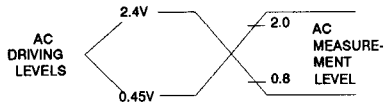
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



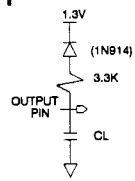
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



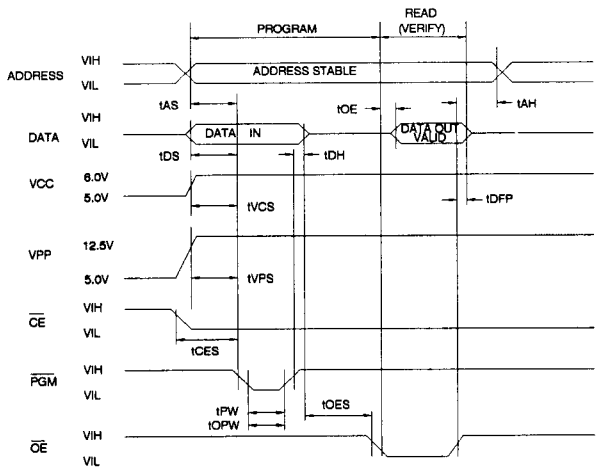
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C128 a 0.1μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, V_{PP}=12.5±0.5V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	Vcc Supply Current (Program and Verify)			30	mA
I_{PP2}	VPP Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.0±0.25V, V_{PP}=12.5±0.5V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	VPP Setup Time		2		µs
t_{VCS}	Vcc Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(Note 3)	0.95	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(Note 4)	2.85	78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Initial Program Pulse width tolerance is 1msec±5%.
4. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

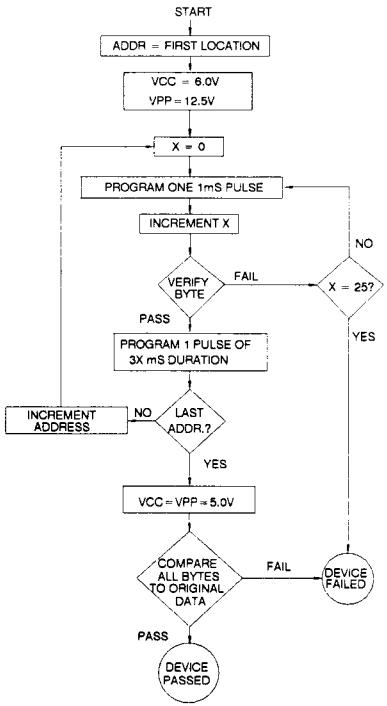
Atmel's 27C128 Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	1	1F
Device Type	1	1	0	0	0	0	0	1	1	83

Fast Programming Algorithm

Two $\overline{PGM}$ pulse widths are used to program; initial and overprogram. Ai are set to address the desired byte. V_{CC} is raised to 6.0V. The first $\overline{PGM}$ pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram $\overline{PGM}$ pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then V_{CC} is lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	30	0.1	AT27C128-12DC	28DW6	Commercial (0°C to 70°C)
120	40	0.2	AT27C128-12DI	28DW6	Industrial (-40°C to 85°C)
150	30	0.1	AT27C128-15DC AT27C128-15PC AT27C128-15JC	28DW6 28P6 32J	Commercial (0°C to 70°C)
150	40	0.2	AT27C128-15DI AT27C128-15PI AT27C128-15JI	28DW6 28P6 32J	Industrial (-40°C to 85°C)
200	30	0.1	AT27C128-20DC AT27C128-20PC AT27C128-20JC	28DW6 28P6 32J	Commercial (0°C to 70°C)
200	40	0.2	AT27C128-20DI AT27C128-20PI AT27C128-20JI	28DW6 28P6 32J	Industrial (-40°C to 85°C)
250	30	0.1	AT27C128-25DC AT27C128-25PC AT27C128-25JC	28DW6 28P6 32J	Commercial (0°C to 70°C)
250	40	0.2	AT27C128-25DI AT27C128-25PI AT27C128-25JI	28DW6 28P6 32J	Industrial (-40°C to 85°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)