2.5 Gbit/s Clock and Data Recovery Circuit GD16504

Preliminary

General Description

The GD16504 is a high performance monolithic integrated 2.488 Gbit/s *Clock and Data Recovery* (CDR) device applicable for optical communication systems including:

- SDH STM-16
- SONET OC-48.

The CDR contains all circuits needed for reliable acquisition and lock of the VCO phase onto the incoming data.

The electrical input sensitivity is better than 20 mV. Optical receivers with sensitivity better than -34 dBm have been obtained without optical pre-amplification.

The device meets all ITU-T jitter requirements when used with the recommended loop filter (jitter tolerance, -transfer and -generation).

The integrated 1:16 demultiplexer with differential ECL outputs ensures a simple and universal interface to the system CMOS ASICs.

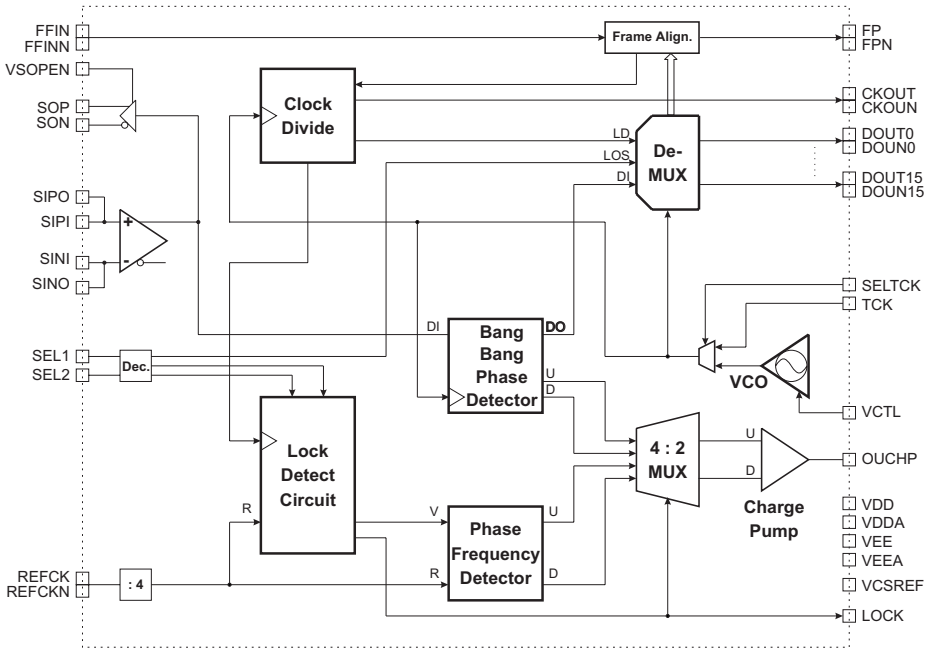
The 155 MHz output clock is maintained within 500 ppm tolerance even in absence of data.

A triggerable Frame Alignment circuit detecting the occurrence of a framing pattern and aligning data at the 16 bit output interface. Once the frame is found, the circuit detects and flags all A1A1A2A2 sequences at the aligned byte boundary.

All high speed I/O levels are ECL compatible. The data input has improved sensitivity and is connected via a 50 Ω loop through transmission line to minimize stub related reflections.

It is packed in a plastic fpBGA with internal 50 Ω transmission lines, heat transport to PCB, reduced mechanical stress and removed requirement for a heat sink. All signals are available in two outher ring for easy routing.

It is also available in a 68 pin leaded Multi Layer Ceramic (MLC) package with 50 Ω transmission lines and cavity down for easy cooling/heat sinking.



Features

- Clock and Data Recovery at 2.488 Gbit/s.
- SDH STM-16, SONET OC-48 compatible.
- Differential Data inputs better than 20 mV sensitivity for BER 10^{-9}.
- Differential ECL Data and Clock outputs.
- Acquisition time < 500 µs.
- Few external passive components needed.
- 50 Ω Loop-Through data inputs for higher sensitivity.
- Frame Detection and user triggered alignment at 16 bits boundary.
- Single supply operation.
- Power dissipation: 2.5 W
- Available in:
  - 144 ld. fpBGA
  - 68 pin Multi Layer Ceramic leaded package with 50 Ω transmission lines.
- GD16504-68BA is 100% interchangeable with GD16045, only loop filter has to be changed.

Applications

- Clock and Data Recovery for:
  - SDH STM-16
  - SONET OC-48 systems

Functional Details

The main application of the GD16504 is as Clcok and Data Recovery in optical communication systems including:

- SDH STM-16
- SONET OC-48

It integrates:

- a Voltage Controlled Oscillator (VCO)
- a Lock Detect Circuit
- a Frequency Detector (PFD)
- a 1:16 DeMUX with framer.
- a Bang-Bang Phase Detector

into a clock and data recovery circuit followed by a 1:16 demultiplexer with differential ECL data and clock outputs.

VCO

The VCO is a low noise LC-type differential oscillator running 2.488 GHz. Tuning is done by applying a voltage to the VCTL pin.

Lock Detect Circuit

The Lock Detect Circuit continuously monitors the difference between the reference clock, which is at 1/16 of the data rate, and the divided VCO clock. If the reference clock and the divided VCO frequency differs by more than 500 ppm (or 2000 ppm, selectable), it switches the PFD into the PLL in order to pull the VCO back inside the lock-in range. This mode is called **the acquisition mode.** Once the VCO is inside the lock-range the lock-detection circuit switches the Bang-Bang phase detector into the PLL in order to lock to the data signal. This mode is called **CDR mode**. The status of the lock-detection circuit is given by output pin LOCK. In acquisition mode LOCK is low.

In acquisition mode a PFD is used to ensure predictable lock up conditions for the GD16504 by locking the VCO to an external reference clock source. It is only used during acquisition and pulls the VCO into the lock range where the Bang-Bang phase detector is capable of acquiring lock. The PFD is made with digital set/reset cells giving it a true phase and frequency characteristic. The reference clock input, REFCK, to the PFD is at 1/16 of the data rate.

Bang-Bang Phase Detector

The Bang-Bang phase detector is used in **CDR mode** as a true digital type phase detector, producing a binary output. It samples the incoming data twice each bit period, once on the transition of the previous bit period and once in the middle of the bit period. When a transition occurs between 2 consecutive bits - the value of the sample in the transition between the bits determines whether the VCO clock leads or lags the data. Hence the *Phase Locked Loop* (PLL) is controlled by the bit transition point, thereby ensuring that data is sampled in the middle of the eye, once the system is in CDR mode. The external loop filter controls the characteristics of the PLL.

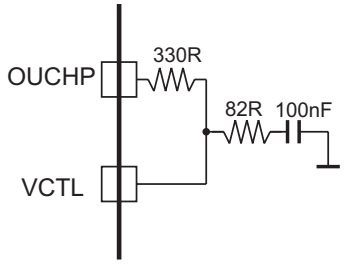


Figure 1. *Loop Filter*

The binary output of either the PFD or the Bang-Bang phase detector (depending of the mode of the lock-detection circuit) is fed to a charge pump capable of sinking or sourcing current or tristating. The output of the charge pump is filtered through the loop filter and controls the tuning-voltage of the VCO.

A result of the continuous lock-detect monitoring circuit is that the VCO frequency never deviates more than 500 ppm (2000 ppm) from the reference clock before the PLL is considered to be 'Out of Lock'. Hence the acquisition time is predictable and short and the output clock CKOUT is always kept within the 500 ppm (2000 ppm) limits ensuring safe clocking of down stream circuitry.

The LOCK Signal

The LOCK output may be used to generate *Loss of Signal* (LOS). The time for LOCK to assert is predictable and short, equal to the time to go into lock, but the time for LOCK to de-assert must be considered. When the line is down (i.e. no information received) the optical receiver circuit may produce random noise. It is possible that this random noise will keep the GD16504 within the 500 ppm (2000 ppm) range of the line frequency, hence LOCK will remain asserted for a non-deterministic time. This may be prevented by injecting a small current at the loop filter node, which actively pulls the PLL out of the lock range when the output of the phase detector acts randomly. The negligible penalty paid is a static phase error. However, due to the nature of the phase detector the error will be small (few degrees), forcing the loop to be at one edge of the error-function shaped transfer characteristic of the detector.

If a LOS is detected by the optical circuit in front of GD16504, the SEL1 and SEL2 may be configured to force the PLL to use the Frequency Detector providing a stable output clock locked only to reference input regardless of Lock Detect status and at the same time force all outputs to logic low.

The configuration signals (SEL1 and SEL2) may be tied to VDD or VEE directly. The combination resets all Flip Flops, and sets both Up and Down active at the input of the Charge Pump, leaving the output in the middle of its output range. Since the circuit is self synchronizing, reset need not be asserted during power up.

Data Inputs

The input amplifier (pins SIPI / SINI and SIPO / SINO) is designed as a limiting amplifier with a sensitivity better than ±20 mV (differential). The inputs may be either AC or DC coupled. In either case input termination is made through pins SIPO / SINO. If the inputs are AC-coupled the amplifier features an internal offset cancelling DC feedback path. All four AC coupling capacitors should be identical for optimum performance. Notice that the offset cancellation will only work when the input is differential and AC- coupled as shown in the Figure 3.

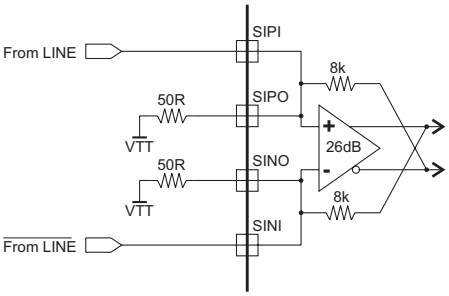


Figure 2. *DC Coupled Input (Ignoring internal offset compensation)*

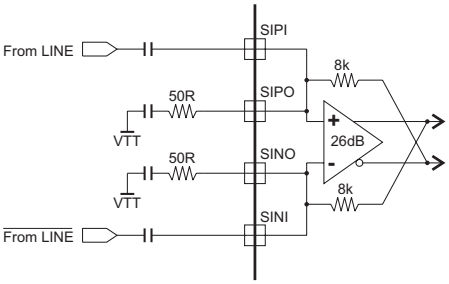


Figure 3. *AC Coupled Input (Using internal offset compensation)*

Following the CDR block the data is 1:16 demultiplexed with frame detect and alignment, and output together with a 155 MHz clock. The data and clock outputs are differential ECL outputs that should be terminated via 50 Ω to -2 V.

The GD16504 includes a serial open collector output intended to loop data to GD16505 as shown in Figure 4 below.

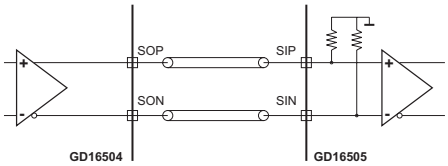


Figure 4. *Test Link Connection between GD16504 and GD16505*

Frame Alignment

The *Frame Detect Alignment* (FDA) circuit uses the available 48 A1 bytes in the incoming data stream to align byte wise and search for valid Frame Sequences (A1-A1-A2-A2). At the falling edge of the FFIN signal, the FDA starts looking for valid A1's in the incoming data stream, regardless of byte boundary. To align at the byte boundary, at least 7 A1's should be valid in a row, followed by more than 2 valid A1's for each erroneous A1.

When the byte alignment is locked, the FDA asserts FP at the first occurrence of A1-A1-A2-A2, which must be valid. Note that the A1 used for byte alignment could be the same as used for the frame alignment, meaning that a sequence of 7 A1's followed by 2 A2's will result in 100% alignment. When a frame has been found and the FFIN is not triggered, only frame sequences (A1-A1-A2-A2) occurring at the previously aligned byte boundary is detected. This way the circuit serves two functions.

When acquiring Frame Alignment, the assertion of the FFIN / FFINN signal starts the FDA alignment and when the first valid sequence is found, the byte boundary is fixed and the FP / FPN output signal is pulsed. The byte boundary is held until the next falling edge on FFIN / FFINN, and only valid sequences at the fixed byte boundary will be flagged by the FP / FPN signal. This allows the user to control when to align, and to have flagged all valid sequences once alignment is achieved.

Note that all valid sequences (7 A1's followed by 2 A2's) will be flagged, regardless of their mutual distance.

The mean time to align and detect a frame pulse (BER = 0) is 0.5 x Frame (62.5 µs), since the FDA will align and pulse FP upon reception of the first Frame Sequence.

GD16504-68BA

The 68 pin CQFP has a reduced pin count, this will affect some at the differential signals that will become single ended.

The unconnected (inverted) input is biased to -1.3 V internally on the chip. This will give the threshold at the single ended signal.

Affected signals are:
- Inputs: FFIN and REFCK
- Output: FP

Pin List

Mnemonic:	Pin No.: 144 EA	Pin No.: 68 BA	Pin Type:	Description:
SIP, SIPO	E1, F1	62, 61	Anl. IN	Loop-through serial positive differential input. Optimised for max. sensitivity; may be used as ECL input.
SIN, SINO	D1, C1	63, 64	Anl. IN	Loop-through serial negative differential input. Optimised for max. sensitivity; may be used as ECL input.
SOP, SON	J1, H1	58, 59	CML OUT	Buffered differential serial data output. High speed Open Collector Drain output to be used in conjunction with GD16505 for remote/optical loop back. Consult GIGA for information.
DOUT0, DOUN0 DOUT1, DOUN1 DOUT2, DOUN2 DOUT3, DOUN3 DOUT4, DOUN4 DOUT5, DOUN5 DOUT6, DOUN6 DOUT7, DOUN7 DOUT8, DOUN8 DOUT9, DOUN9 DOUT10, DOUN10 DOUT11, DOUN11 DOUT12, DOUN12 DOUT13, DOUN13 DOUT14, DOUN14 DOUT15, DOUN15	A11, A10 B12, A12 D11, C12 D12, E11 F12, F11 G12, G11 H12, H11 J12, J11 L12, K12 M11, M12 M9, M10 L8, L9 M7, M8 M6, L7 M4, M5 L3, M3	12, 11 15, 13 19, 16 22, 20 24, 23 27, 25 29, 28 32, 30 36, 33 39, 37 41, 40 44, 42 46, 45 49, 47 53, 50 56, 54	ECL OUT	Retimed differential data output from DeMUX, bit 15 is the first received. After frame synchronisation, the data is byte-aligned with the first A2 byte placed at bit 15 through 8. When LOCK = “0" or SEL1= ”1" and SEL2 = “0" (LOS), all outputs will be logic low
REFCK, REFCKN	A6, A7	6, N/A	ECL IN	155 MHz reference clock input. Both biased to -1.3 V in 68BA version
CKOUT, CKOUN	A9, B9	10, 8	ECL OUT	Regenerated differential output clock, 155 MHz.
SEL1, SEL2	A1, E12	67, 18	ECL IN	Single-ended inputs, PLL set-up of Internal/ External switch mode and LOCK: SEL1 SEL2 0 0 Auto lock, 500ppm. 0 1 Global Reset for test purpose only. 1 0 Manual, Phase/ Freq. det, 500 ppm,LOS mode. 1 1 Manual, Phase detector, 2000 ppm. The LOS mode cause all 16 data outputs, FP and LOCK into logic low.
FFIN, FFINN	B8, A8	7, N/A	ECL IN	Frame FINd signal. A falling edge at this input activates the frame search. Single ended in 68-pin CQFP.
LOCK	B6	5	ECL OUT	Single ended CDR Lock alarm output. When low, the divided VCO freq. deviates more than 500/2000 ppm from REFCK. When system is unlocked, all 16 data outputs and FP will be logic low. When SEL1 = "1" and SEL2 = "0" (LOS), the LOCK will be logic low.
FP, FPN	M1, L1	57, N/A	ECL OUT	Frame Pulse. One pulse (6.1 ns) indicates that a valid Frame Sequence has been detected. When LOCK = “0" SEL1 = ”1" and SEL2 = “0" (LOS), the FP / FPN will be logic low. FP/ FPN is also low during reset. single ended output in 68-pin CQFP. Differential in other packages.
VCTL	A3	2	Anl. IN	VCO control voltage input.
OUCHP	A4	3	Anl. OUT	Phase detector or Phase / frequency charge pump output.
TCK	A2	66	ECL IN	DC - functional and parametric test clock input. Bypasses the VCO when SELTCK is high.

Mnemonic:	Pin No.: 144 EA	68 BA	Pin Type:	Description:
VDD	B1, C2, D2, D4..9, E2, E4..9, F2, F4..9, G1, G2, G4..9, H2, H4..H9, J2, J4..J9, K1, K2, M2	4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65	PWR	0 V Power for core and ECL I/O.
VEE	C3..5, C10, D3, D10, E3, E10, F3, F10, G3, G10, H3, H10, J3, J10, K3..5	34, 35, 68	PWR	-5 V Power for core and ECL I/O.
VDDA	A5, B5	17	PWR	0 V Power for VCO
VEEA	B3, B4	52	PWR	-5 V Power for VCO.
SELTCK	B2	1	PWR	Select test clock, for DC test only, connect to VEE.
VSOPEN	L2	51	PWR	0 V power for Serial Output (SOP/SON). If output is not used, VSOPEN may be left open (or connected to VEE), saving power. Nominal current is 0.5 mA.
VCSREF	L6	N/A	ANALOG	Internal reference voltage, leave open
NC	B7, B10, B11, C6..9, C11, K6..9, K10, K11, L10, L11, L4, L5	N/A		Not used. Reserved for future use.

Package Pinout

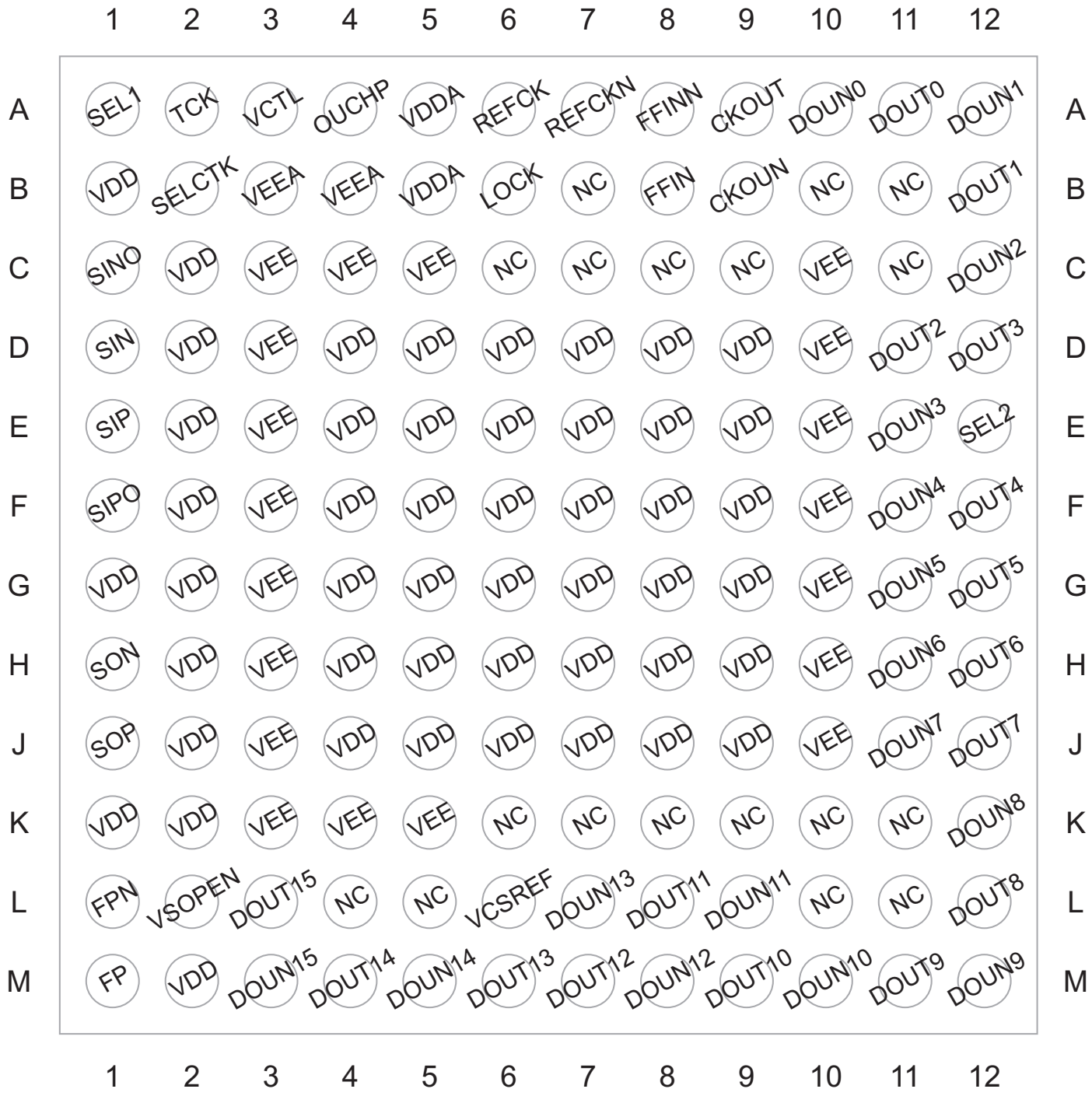


Figure 5. *Package Pinout, 144 EA - Top View (seen through the package)*

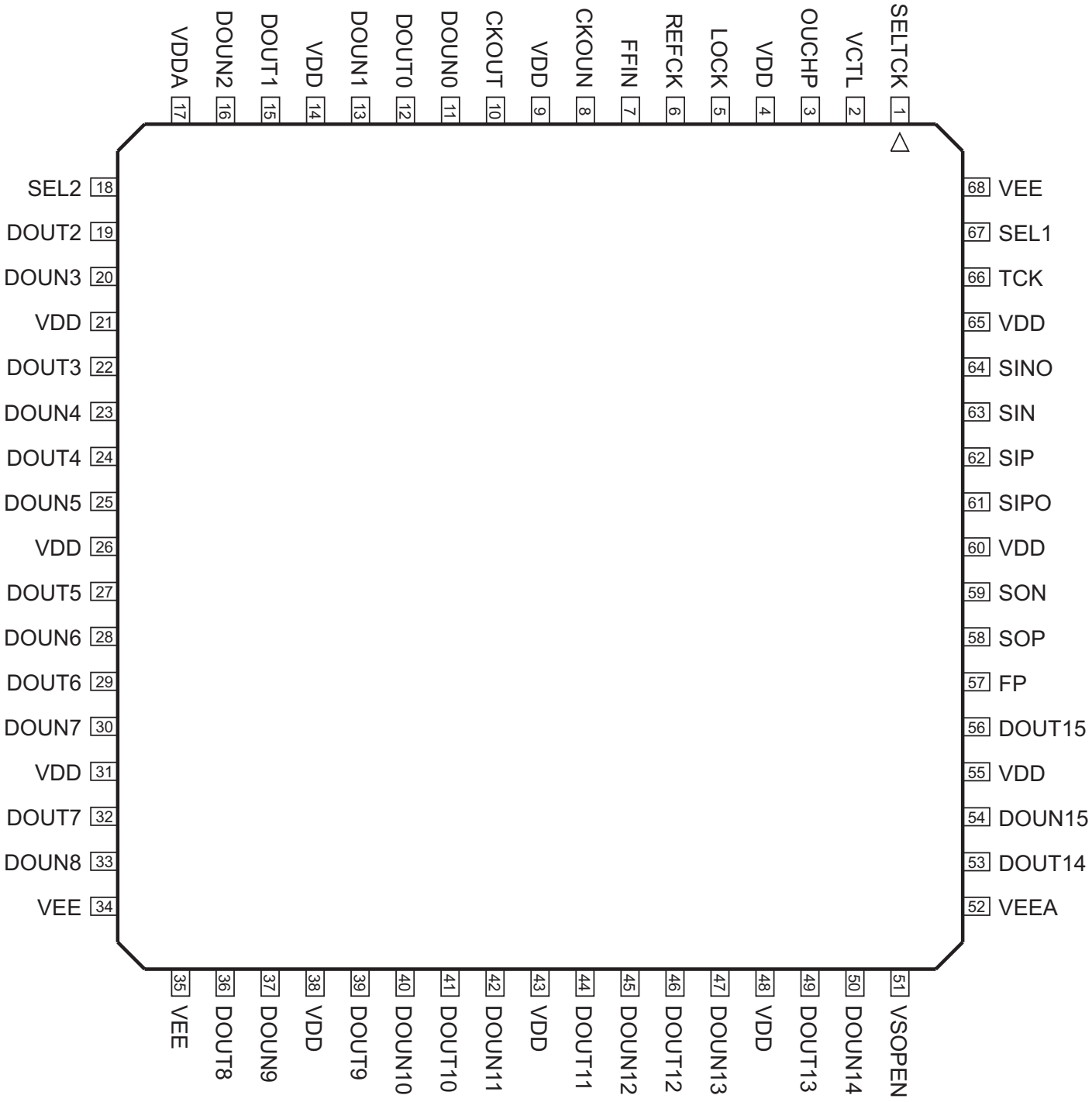


Figure 6. *Package Pinout, 68 BA - Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to VDD.
All currents in the table are defined positive out of the pin.

Symbol:	**Characteristic:**	**Conditions:**	**MIN.:**	**TYP.:**	**MAX.:**	**UNIT:**
V_{EE}, V_{EEA}	Negative Supply		-7		0	V
V_0 *ECL*	Output Voltage	ECL	V_{EE} -0.5		0.5	V
I_0 *ECL*	Output Current	ECL			40	mA
I_0 *MAX, CHPO*	Output Current				0.25	mA
V_1 *ECL*	Input Voltage	ECL	V_{EE} -0.5		0.5	V
I_1 *ECL*	Input Current	ECL	-1.0		1.0	mA
T_0	Operating Temperature	Junction	-40		+125	°C
T_S	Storage Temperature		-65		+150	°C

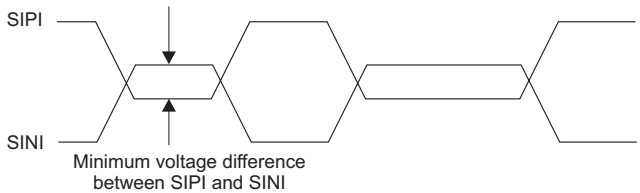
DC Characteristics

T_{CASE} = 0 °C to 85 °C, V_{EE} = -4.75 to -5.25 V
θ_{J-C} = 7°C/W, for 68-pin CQFP.

All voltages in the table are referred to VDD.
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
V_{EE}	Supply Voltage		-5.25		-4.75	V
I_{EE}	Supply Current				500	mA
V_I *SINX/SIPX*	Minimum Data Input Swing for 10^{-9} BER	Note 5			25	mV
V_I *SINX/SIPX*	Data Input Swing	Note 5			1000	mV
V_{ICM} *SINX/SIPX*	Data Common Mode Voltage		-2	-1.3	-1	V
V_{IL} *ECL*	ECL Input LO Voltage	Note 1	V_{EE}		-1.5	V
V_{IH} *ECL*	ECL Input HI Voltage	Note 1	-1.1		0	V
I_{IH} *ECL*	ECL Input HI Current	V_{IH} = -0.7		12	100	µA
I_{IL} *ECL*	ECL Input LO Current	V_{IL} = -1.8		0.01	-1	µA
V_{OH} *ECL*	ECL Output HI Voltage	Note 1, 2	-1.0		-0.5	V
V_{OL} *ECL*	ECL Output LO Voltage	Note 1, 2	V_{TT}		-1.6	V
I_{OH} *ECL*	ECL Output HI Current	Note 3	20	23	30	mA
I_{OL} *ECL*	ECL Output LO Current	Note 3	-2	5	8	mA
I_{OH} *CML*	CML Output HI Current			0		mA
I_{OL} *CML*	CML Output LO Current			8		mA
V_{VCTL}	VCO Control Voltage	I_{VCTL} < 30 µA	V_{EE}		-1	V
I_{OH} *CHP*	OUCHP Source Current (DC Steady)	Note 4		100		µA
I_{OL} *CHP*	OUCHP Sink Current (DC Steady)	Note 4		100		µA

Note 1: V_{TT} = -2.0 V ±5 %
Note 2: R_{LOAD} = 50 Ω to V_{TT}
Note 3: Not tested, consistent with V_{OH} and V_{OL} tests.
Note 4: Output terminated to -2.5 V during test.
Note 5: Minimum data input swing to ensure 10^{-9} BER. It is defined as the differential (p-p) voltage between the two inputs, i.e. as the p-p voltage on SIPI + the p-p voltage on SINI. In case of unbalanced signals it is defined as twice the minimum voltage difference between SIPI and SINI (see figure below).



AC Characteristics

T_{CASE} = 0 °C to 85 °C, V_{EE} = -4.75 V to -5.25 V.

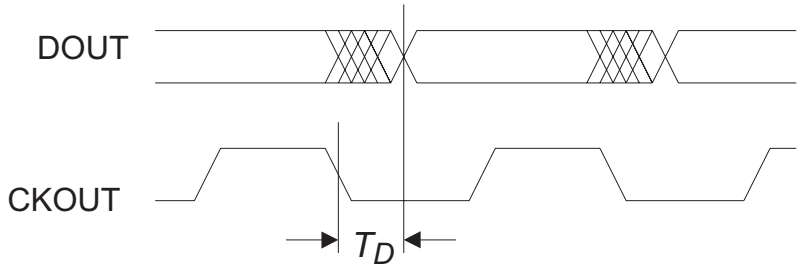


Figure 7. *Time (T_D)*

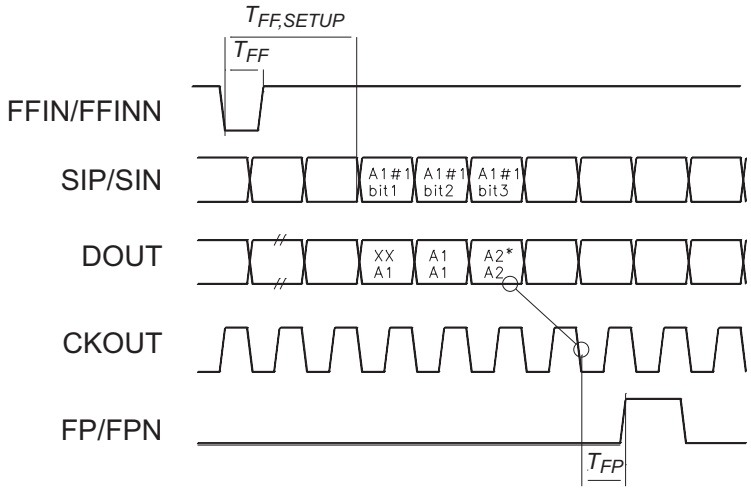


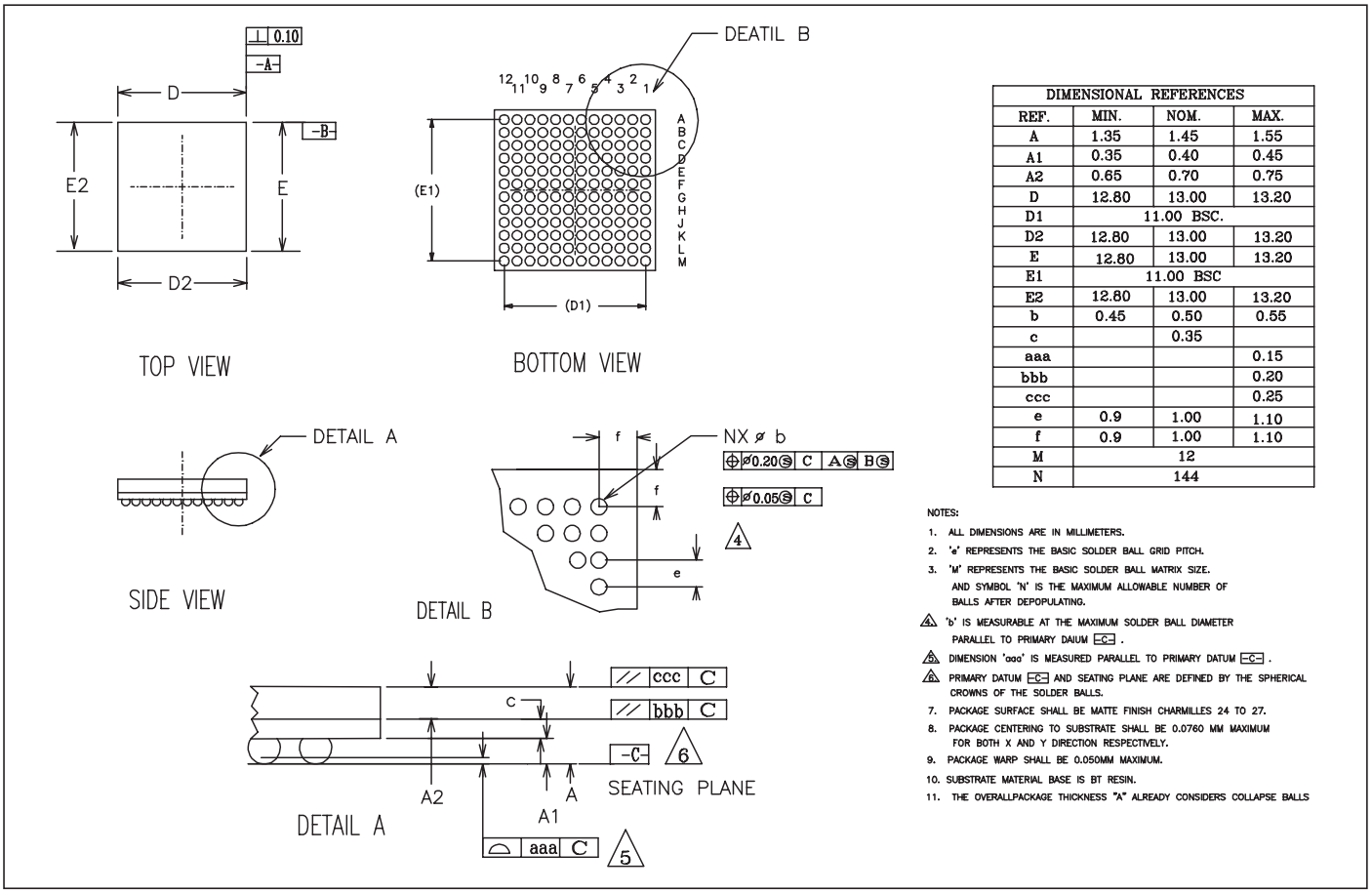
Figure 8. *Frame Align Signal Timing*
Note: During align, A2 byte marked with * may not be valid although frame is correctly aquired ($F6_H$ or 28_H)

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{TOL}	Jitter Tolerance	2 Hz < F < 100 kHz (Note 1) 1 MHz < F< 5 MHz (Note 1)	1.5 0.15	>2 >0.35		$UI_{16, PP}$ $UI_{16, PP}$
J_{TRF}	Jitter Transfer	5 kHz < F < 2 MHz (Note 2)		0.08	0.1	dB
J_{CLK}	Output Clock Intrinsic Jitter	5 kHz < F < 20 MHz (Note 3) 1 MHz < F < 20 MHz (Note 3)			0.125 0.05	UI_1 UI_1
T_A	Aquisition time	2^{23}-1 PRBS		50	500	µs
L_{CID}	Consecutive Identical Digits	No. bits with no transitions	400	1000		bits
D_C	Input Clock / REFXI frequency deviation	Note 4	-200		200	ppm
$C_{DUTY\ REFCK}$	REFCK clock duty cycle	$V_{Thresh.}$= -1.3 V	40		60	%
$C_{DUTY\ CKOUT}$	Output clock duty cycle	$V_{Thresh.}$= -1.3 V, 50 Ω to -2 V	45		55	%
$T_{TLH\ DATA}$	Output data rise time	20 – 80 %, 50 Ω to -2 V		350	700	ps
$T_{THL\ DATA}$	Output data fall time	80 – 20 %, 50 Ω to -2 V		350	700	ps
T_D	DOUT from CKOUT	*See figure 7*		275		ps
T_{FP}	FP from CKOUT	*See figure 8*		275		ps
$T_{FF,\ SETUP}$	FFIN set-up from FRAME start	*See figure 8*	1000	600		ps

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
T_{FF}	FFIN pulse width	*See figure 8*	3			ns
$N_{SERIAL-PARALLEL}$	no. of bits stored in pipelines				40	bits

Note 1: 1 UI_{16} = 40 ns; Data Pattern 2^{23}-1 PRBS.
Note 2: Data Pattern 2^{23}-1 PRBS. Through careful filter design, loop peaking may be controlled which is the major contribute to Jitter Transfer.
Note 3: In the absence of input jitter, the intrinsic jitter at CKOUT as measured over a 60 seconds interval shall not exceed these limits (1 UI_1 = 6.43 ns).
Note 4: Max. deviation between reference clock input and divided VCO clock when in lock.

Package Outline



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.35	1.45	1.55
A1	0.35	0.40	0.45
A2	0.65	0.70	0.75
D	12.80	13.00	13.20
D1		11.00 BSC.	
D2	12.80	13.00	13.20
E	12.80	13.00	13.20
E1		11.00 BSC	
E2	12.80	13.00	13.20
b	0.45	0.50	0.55
c		0.35	
aaa			0.15
bbb			0.20
ccc			0.25
e	0.9	1.00	1.10
f	0.9	1.00	1.10
M		12	
N		144	

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE. AND SYMBOL 'N' IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. 'b' IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DAIUM -C- .
5. DIMENSION 'aaa' IS MEASURED PARALLEL TO PRIMARY DATUM -C- .
6. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE MATTE FINISH CHARMILLES 24 TO 27.
8. PACKAGE CENTERING TO SUBSTRATE SHALL BE 0.0760 MM MAXIMUM FOR BOTH X AND Y DIRECTION RESPECTIVELY.
9. PACKAGE WARP SHALL BE 0.050MM MAXIMUM.
10. SUBSTRATE MATERIAL BASE IS BT RESIN.
11. THE OVERALLPACKAGE THICKNESS "A" ALREADY CONSIDERS COLLAPSE BALLS

Figure 9. *Package 144 pfBGA*

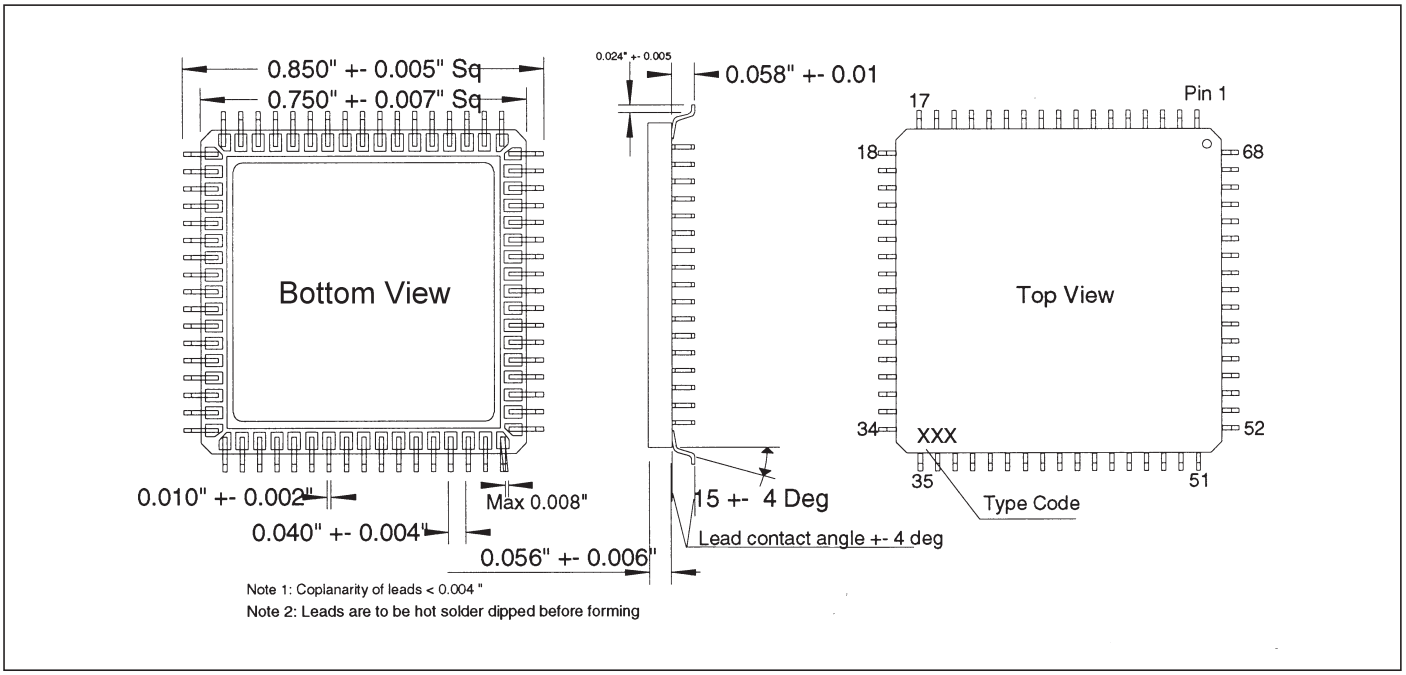


Figure 10.*Package 68 pin MLC*

Device Marking

Ordering Information

Please order as specified below:

Product Name:	Package Type:	Case Temperature Range:	Options:
GD16504-144EA	144 pfBGA	0..85 °C	
GD16504-68BA	68 pin Ceramic (MLC)	0..85 °C	

GD16504, Data Sheet Rev. 04 - Date: 11 May 1999

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