MOTOROLA

MC74F543

OCTAL REGISTERED TRANSCEIVER, NON-INVERTING, 3-STATE

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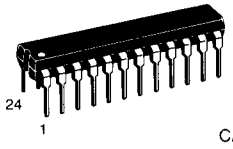
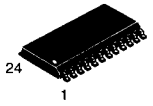
FAST™ SCHOTTKY TTL

The MC74F543 Octal Registered Transceivers contain two sets of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The MC74F543 has a noninverting data path. The A outputs are guaranteed to sink 20 mA while the B outputs are rated for 64 mA.

- Combines 74F245 and 74F373 Type Functions in One Chip
- 8-Bit Octal Transceiver
- Non-Inverting
- Back-to-Back Registers for Storage
- Separate Controls for Data Flow in Each Direction
- Glitchless Outputs During 3-State Power Up or Power Down Operation
- High Impedance Outputs in Power Off State
- A Outputs Sink 24 mA and Source 3.0 mA
- B Outputs Sink 64 mA and Source 15 mA
- See F544 for Inverting Version
- ESD Protection > 4000 Volts



N SUFFIX
PLASTIC
CASE 724-03

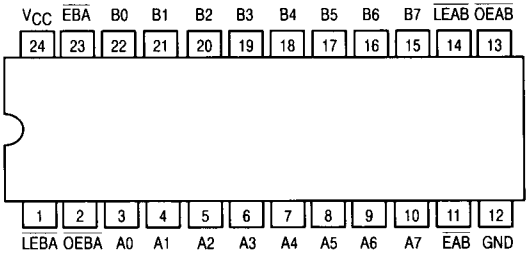


DW SUFFIX
SOIC
CASE 751E-03

ORDERING INFORMATION

MC74FXXXN	Plastic
MC74FXXXDW	SOIC

PIN ASSIGNMENT



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	74			−3.0/−15	mA
I_{OL}	Output Current — Low	74			24/64	mA

FUNCTION TABLE

Inputs				Outputs	Status
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	Data		
H	X	X	X	Z	Outputs disabled
L L	H H	L L	l h	Z Z	Outputs disabled Data latched
L L	L L	H H	l h	L H	Data latched
L L	L L	L L	L H	L H	Transparent

H = HIGH voltage level: h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA): L = LOW Voltage Level: l = LOW state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA): X = Don't care: Z = HIGH impedance state.

FUNCTIONAL DESCRIPTION

The MC74F543 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) Input must be LOW in order to enter data from A0–A7 or take data from B0–B7, as indicated in the Function Table. With $\overline{EAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both LOW, the 3-State B output buffers are active and reflects the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter			Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage			2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage					0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−0.73	−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	A0–A7	74	2.4			V	I_{OH} = −3.0 mA	V_{CC} = 4.5 V
				2.7	3.4				V_{CC} = 4.75 V
		B0–B7	74	2.0			V	I_{OH} = −15 mA	V_{CC} = 4.5 V
V_{OL}	Output LOW Voltage	A0–A7	74		0.35	0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
		B0–B7	74		0.4	0.55	V	I_{OL} = 64 mA	
I_{IH}	Input HIGH Current		I/O Pins			1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
			Control Pins			100	μA	V_{CC} = MAX, V_{IN} = 7.0 V	
						20		V_{CC} = MAX, V_{IN} = 2.7 V	
I_{IL}	Input LOW Current		$\overline{EAB}$, $\overline{EBA}$			−1.2	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
			Other Inputs			−0.6			
I_{OZH}	Off-State Output Current, High-Level Voltage Applied					70	μA	V_{CC} = MAX	V_{OUT} = 2.7 V
						1.0	mA		V_{OUT} = 5.5 V
I_{OZL}	Off-State Output Current, Low-Level Voltage Applied					−600	μA	V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		A_n Outputs	−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
			B_n Outputs	−100		−225			
I_{CC}	Total Supply Current		I_{CCH}		70	100	mA	V_{CC} = MAX	
			I_{CCL}		95	125			
			I_{CCZ}		95	125			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			74F T_A = 0 °C to +70°C, V_{CC} = +5.0 V ±10%, C_L = 50 pF		Unit
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode $\overline{A_n}$ to $\overline{B_n}$ or $\overline{B_n}$ to $\overline{A_n}$	2.0 2.0	— —	9.5 6.5	2.0 2.0	10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to $\overline{A_n}$	6.0 4.0	— —	13 9.5	6.0 4.0	14.5 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to $\overline{B_n}$	6.0 4.0	— —	13 9.5	6.0 4.0	14.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A_n}$ or $\overline{B_n}$ $\overline{EBA}$ or $\overline{EAB}$ to $\overline{A_n}$ or $\overline{B_n}$	3.0 4.0	— —	9.0 10.5	3.0 4.0	10 12	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A_n}$ or $\overline{B_n}$ $\overline{EBA}$ or $\overline{EAB}$ to $\overline{A_n}$ or $\overline{B_n}$	1.5 1.5	— —	8.0 7.5	1.5 1.5	9.0 8.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			74F T_A = 0°C to +70°C, V_{CC} = +5.0 V ±10%, C_L = 50 pF			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{s(H)}$ $t_{s(L)}$	Setup Time, HIGH or LOW $\overline{A_n}$ or $\overline{B_n}$ to $\overline{LEBA}$ or $\overline{LEAB}$	3.0 3.0	— —	— —	3.0 3.0	— —	— —	ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW $\overline{A_n}$ to $\overline{B_n}$ to $\overline{LEBA}$ or $\overline{LEAB}$	3.0 3.0	— —	— —	3.0 3.0	— —	— —	ns
$t_{w(L)}$	Latch Enable, B to A Pulse Width, LOW	6.0	—	—	7.5	—	—	ns

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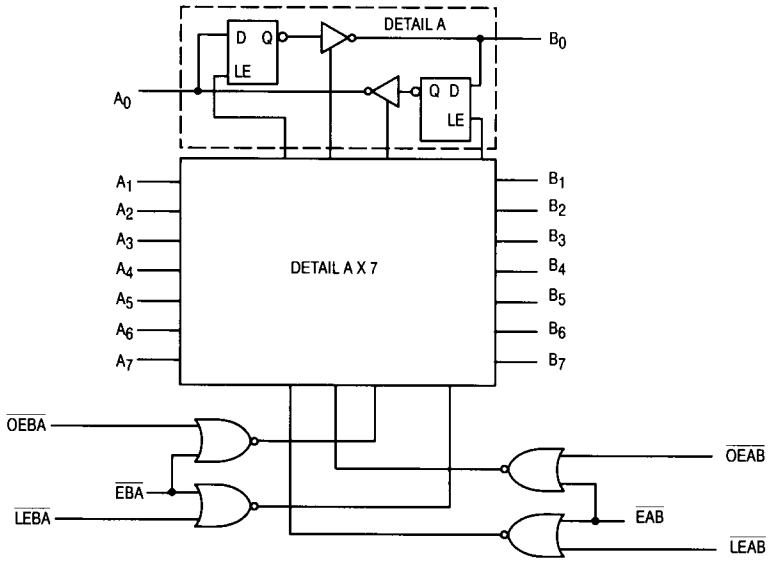
LOGIC DIAGRAM



NOTE:
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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