



64 by 4 and 64 by 5 BiCMOS TTL FIFO Buffer Memory

FEATURES

- **High Speed Shift-In and Shift-Out**
10/15/25MHz Cascadeable
40/50MHz Standalone
- **Full Featured Industry Standard Devices**
Expandable Word Widths and Depths
Dual Port RAM Architecture
Independent Asynchronous Inputs/Outputs
- **Full Military 883B Compliant**

DESCRIPTION

The SSL7401, SSL7402, SSL7403 and SSL7404 are very high performance Parallel First-In First-out (FIFO) memories with asynchronous input and output data rates, making them ideal for applications as data buffers between two digital systems of differing operating speeds. The 50MHz data rate is ideal for analog-to-digital converter buffering and high speed telecommunications and data communications controller applications. The FIFOs are organized as 64 x 4 bits and x 5 bits respectively. All four devices are available in various speeds and configurations per the ordering information chart on the last page.

The combined attributes of low power consumption and high speed are derived from Saratoga's proprietary "Self Aligned Bipolar CMOS," SABIC process technology. SABIC integrates bipolar and CMOS in the same monolithic circuit thus providing an increase in speed and density.

Data is shifted into the FIFO through the four or five bit Data Input pins ($DI_0 - DI_{3/4}$) on the rising edge of the Shift In (SI)

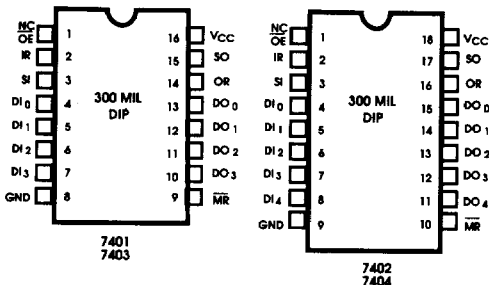
ADVANCE INFORMATION

- **Output Enable (7403 and 7404)**
- **16 and 18-pin 300 MIL DIP**
- **SABIC BiCMOS Fabrication Technology**
Fast Bubble-Through Time - 16ns
Fast Data Access Time-15ns
Fast Setup (0ns) & Hold (5ns) Times

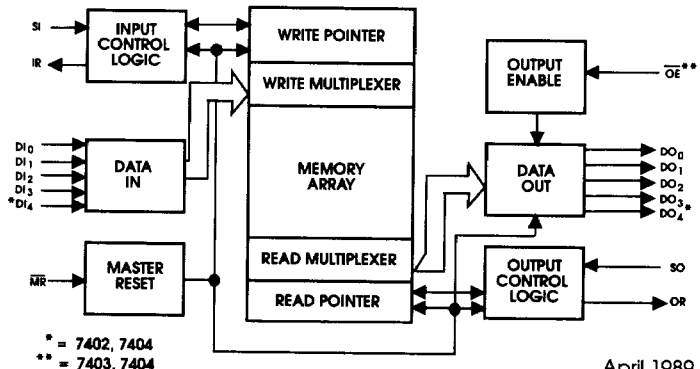
signal. The input Ready (IR) output signal indicates whether or not the FIFO is full after every HIGH to LOW SI transition. HIGH indicates the FIFO is not full and ready for more data. Data is shifted out of the FIFO in the same order as it entered, through the four or five bit Data Output pins ($DO_0 - DO_{3/4}$) when the Shift Out (SO) signal is LOW. The Output Ready (OR) signal indicates whether or not the Data Outputs are valid while SO is LOW. OR remains LOW until the data is valid. The data is not valid when the FIFO is empty or data has not propagated to the outputs.

With the Master Reset (\overline{MR}) input LOW, the FIFO is reset and the Data Output pins are driven to a logic LOW state, IR is driven HIGH and OR is driven LOW. The Output Enable (\overline{OE}) input available on the SSL7403 and SSL7404 forces the Data Output to HIGH impedance states when it is at a logic HIGH state. When it is LOW and therefore active, it is used to enable the Data Output pins. The SSL7401/3 are available in 300 MIL, 16-pin DIP and the SSL7402/4 in 300 MIL, 18-pin DIP.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



SELECTION GUIDE

		7401/2/3/4 -10	7401/2/3/4 -15	7401/2/3/4 -25	7401/2/3/4 -40*	7401/2/3/4 -50*
Maximum Shift Rate (MHz)		10	15	25	40	50
Maximum Operating Current (mA)	Commercial	60	65	75	90	TBD
	Military	60	65	75	90	TBD

*Speed grades not available for cascadeable version. Only available in Stand-Alone (S) mode (see ordering information).

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65 °C to + 150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in HIGH Z State	-0.5V to +7.0V
DC Input Voltage	-0.8V to +7.0V
Power Dissipation	1.0W
Output Current, into Outputs (LOW)	50mA
Static Discharge Voltage (per MIL-STD 883 Method 3015.2)	>2001V
Latch-Up Current	>200mA

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V _{CC}
Commercial	0 °C to +70 °C	5V ± 10%
Military	-55 °C to +125 °C	5V ± 10%

ELECTRICAL CHARACTERISTICS (Over Operating Range, unless Otherwise Noted)

PARAMETERS	DESCRIPTION	TEST CONDITIONS	SSL740X- 10, 15, 25, 40, 50		UNIT
			MIN	MAX	
V _{OH}	Output HIGH Voltage	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min, I _{OL} = 16mA		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC}	V
V _{IL}	Input LOW Voltage		-0.5	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC} , V _{CC} = max	-10	+10	μA
I _{OS}	Output Short Circuit Current (1)	V _{CC} = Max, V _{OUT} = GND		-150	mA
I _{OZ}	Output Leakage Current	$\overline{OE} = V_{IH}$, V _{CC} = max GND ≤ V _{OUT} ≤ V _{CC}	-50	50	μA
I _{CC} (2)	Power Supply Current	$\overline{OE} = V_{IL}$, V _{CC} = max Output Open, f = 40 MHz	Commercial	90	mA
			Military	90	mA

CAPACITANCE (2)

PARAMETERS	DESCRIPTION	TEST CONDITIONS	MAX	UNITS
C _{IN}	Input Capacitance	T _A = 25 °C, f = 1 MHz	5	pF
C _{OUT}	Output Capacitance	V _{CC} = 4.5V	7	pF

Notes: ¹For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
²Tested on sample basis

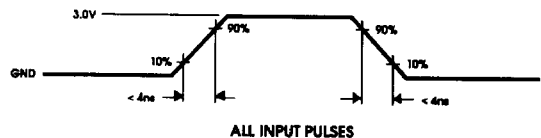
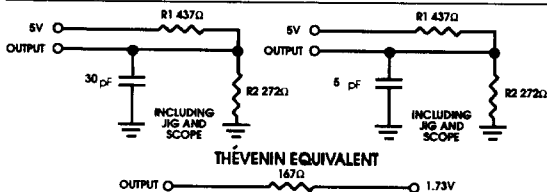


SWITCHING CHARACTERISTICS Over the Operating Range

PARAMETER	DESCRIPTION	TEST CONDITIONS	SSL740X	SSL740X	SSL740X	SSL740X	SSL740X	UNIT
			-10	-15	-25	-40*	-50*	
			MIN	MAX	MIN	MAX	MIN	MAX
f_0	Operating Frequency		10	15	25	40	50	MHz
t_{ACC}	Data Access Time	Note 5	45	35	25	17	15/17	ns
t_{PHSI}	SI HIGH Time		20	20	11	7	5	ns
t_{PLSI}	SI LOW Time	Note 5	30	25	24	14	13/14	ns
t_{SSI}	Data Setup to SI	Note 1	0	0	0	0	0	ns
t_{HSI}	Data Hold from SI	Note 1	40	30	20	7	5	ns
t_{DLIR}	Delay, SI HIGH to IR LOW	Note 5	40	35	21	18	16/18	ns
t_{DHIR}	Delay, SI LOW to IR HIGH	Note 2	45	40	28	20/22	18/22	ns
t_{PHSO}	SO HIGH Time		20	20	11	7	5	ns
t_{PLSO}	SO LOW Time	Note 5	25	25	24	14	13/14	ns
t_{DLOR}	Delay, SO HIGH to OR LOW	Note 5	40	35	19	18	16/18	ns
t_{DHOR}	Delay, SO LOW to OR HIGH	Note 5	55	40	29	21/22	19/22	ns
t_{SOR}	Data Setup to OR HIGH	Note 4	0	0	0	0	0	ns
t_{HSO}	Data Hold from SO LOW		5	5	5	5	5	ns
t_{BT}	Bubblethrough Time	Note 3, 5	5 95	5 65	5 50	5 20	5 16/17	ns
t_{SIR}	Data Setup to IR	Note 4	5	5	5	5	5	ns
t_{HIR}	Data Hold from IR	Note 4	30	30	20	10	10	ns
t_{PIR}	Input Ready Pulse HIGH	Note 4	5	5	5	5	5	ns
t_{POR}	Output Ready Pulse HIGH	Note 4	5	5	5	5	5	ns
t_{PMR}	MR Pulse Width		30	25	25	10	7	ns
t_{DSI}	MR HIGH to SI HIGH	Note 4	35	25	10	5	0	ns
t_{DOR}	MR LOW to OR LOW	Note 5	40	35	35	25	20/22	ns
t_{DIR}	MR LOW to IR HIGH	Note 5	40	35	35	25	20/22	ns
t_{LZMR}	MR LOW to Output LOW	Note 5	40	35	25	25	20/22	ns
t_{OOE}	Output Valid from OE LOW	Note 4	35	30	20	15	10	ns
t_{HZOE}	Output HIGH-Z from OE HIGH	Note 4	30	25	15	12	10	ns

- NOTES:**
- t_{SSI} will increase if the shift in signal or Data signal 0 to 3V rise time is greater than 4ns. The minimum value of $t_{SSI} + t_{HSI}$ is 5ns or the Shift In rise time.
 - Not using Full condition.
 - t_{ar} equals Shift In Low to Output Ready High after Empty condition, or Shift Out Low to Input Ready High after Full condition.
 - Sample testing only.
 - Commercial/Military.

AC TEST LOAD AND WAVEFORMS





OPERATING DESCRIPTION

CONCEPT

Unlike traditional FIFOs these devices are designed using a dual port memory, read and write pointer, and control logic. The read and write pointers are incremented by the Shift Out (SO) and Shift In (SI) respectively. The availability of an empty space to shift in data is indicated by the Input Ready (IR) signal, while the presence of data at the output is indicated by the Output Ready (OR) signal. The conventional concept of bubble through is absent. Instead the delay for input data to appear at the output is the time required to move a pointer and propagate an Output Ready (OR) signal. The Output Enable (OE) signal provides the capability to OR tie multiple FIFOs together on a common bus.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset (MR) signal. This causes the FIFO to enter an empty condition signified by the Output Ready (OR) signal being LOW at the same time the Input Ready (IR) signal is HIGH. In this condition, the data outputs ($DO_0 - DO_{3/d}$) will be in a LOW state.

SHIFTING DATA IN

Data is shifted in on the rising edge of the Shift In (SI) signal. This loads input data into the first word location of the FIFO. On the falling edge of the Shift In (SI) signal, the write pointer is moved to the next word position and the Input Ready (IR) signal goes HIGH indicating the readiness to accept new data. If the FIFO is full, the Input Ready (IR) will remain LOW until a word of data is shifted out.

SHIFTING DATA OUT

Data is shifted out of the FIFO on the falling edge of the Shift Out (SO) signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the Output Ready (OR) signal will go HIGH. If data is not present, the Output Ready (OR) signal will stay LOW indicating the FIFO is empty. Upon the rising edge of Shift Out (SO), the Output Ready (OR) signal goes LOW. Previous data remains on the output until the falling edge of Shift Out (SO).

BUBBLE THROUGH

Two bubble through conditions exist. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the Output Ready (OR) flag goes HIGH indicating valid data at the output.

The second bubble through condition occurs when the device is full. Shifting data out creates an empty location which propagates to the input. After a delay, the Input Ready (IR) flag goes HIGH. If the Shift In (SI) signal is HIGH at this time, data on the input will be shifted in.

APPLICATION OF THE 25-50MHz FIFOs

Application of the Saratoga BiCMOS FIFOs requires attention to characteristics not easily specified in a Datasheet, but necessary for reliable operation under all conditions.

When an empty FIFO is filled with initial information, at maximum 'shift in' (SI) frequency, followed by immediate shifting out of the data also at maximum 'shift out' (SO) frequency, the designer must be aware of a window of time which follows the initial rising edge of the 'output ready' (OR) signal during which the SO signal is not recognized. This condition exists only at high speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full frequency operation, but rather delays the full 25-50 MHz operation until after the window has passed.

There are several implementation techniques to manage the window so that all SO signals are recognized:

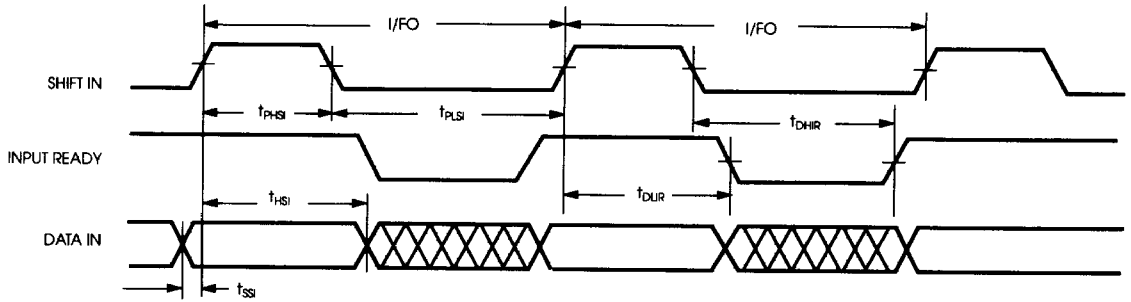
- 1) The first involves delaying SO operation such that it does not occur in the critical window. This can be accomplished by causing a fixed delay initiated by the SI signal only when the FIFO is empty to inhibit or gate the SO activity. This, however requires that the SO operation at least temporarily be synchronized with the input SI operation. In synchronous applications, this may well be possible and a valid solution.
- 2) Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is greater than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Saratoga's FIFOs do not have this limitation, any system designed in this manner will not encounter the window condition described above.
- 3) The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO from the rising edge of the initial 'output ready' (OR) signal. This however involves the requirement that this only occurs on the first occurrence of data being loaded into the FIFO from any empty condition and therefore requires the knowledge of 'input ready' (IR) and (SI) conditions as well as (SO).
- 4) Handshaking with the OR signal can be a third method of avoiding the window in question. With this technique, the rising edge of SO, or the fact that the SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken LOW again, advancing the internal pointer to the next data, until the OR signal goes LOW. This assures that the SO pulse that is initiated in the window will be automatically extended sufficient time to be recognized.
- 5) There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the OR signal is most appropriate because data is guaranteed to be stable prior to and after the OR leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

Any of the above solutions will provide a solution for correct operation of a Saratoga FIFO at 25-50 MHz. The specific implementation is left to the designer and dependent on the specific application needs.

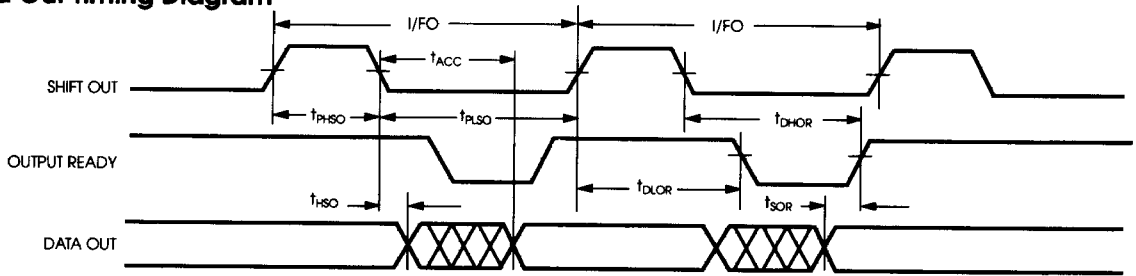


SWITCHING WAVEFORMS

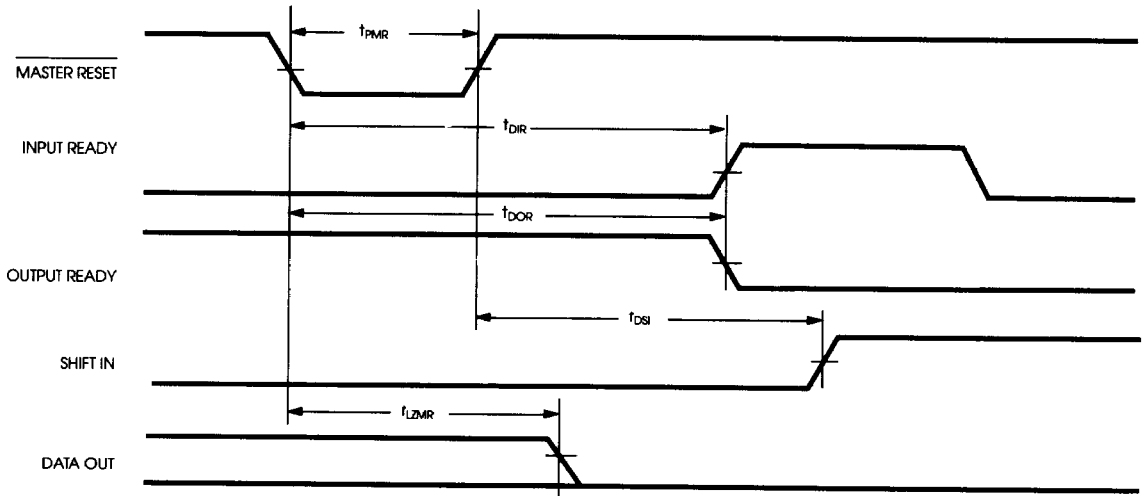
Data In Timing Diagram



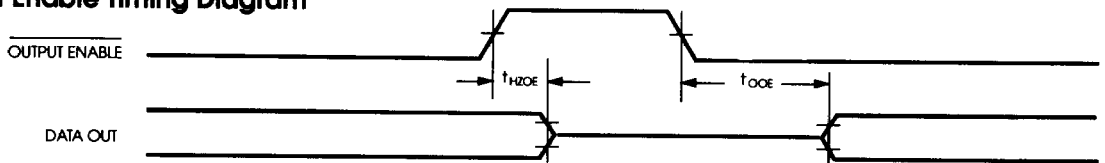
Data Out Timing Diagram



Master Reset Timing Diagram



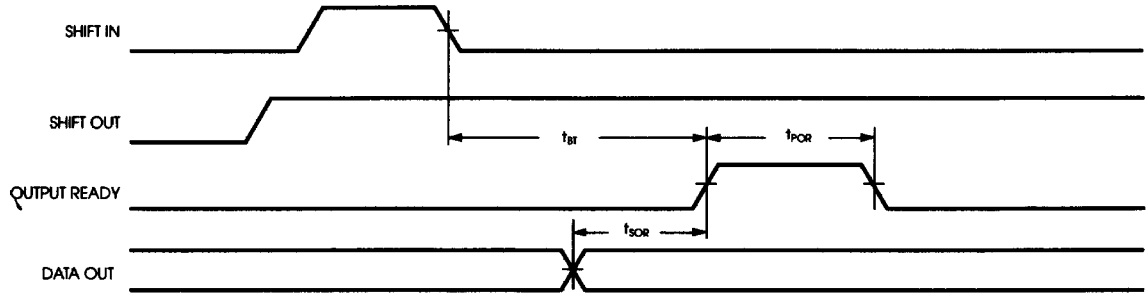
Output Enable Timing Diagram



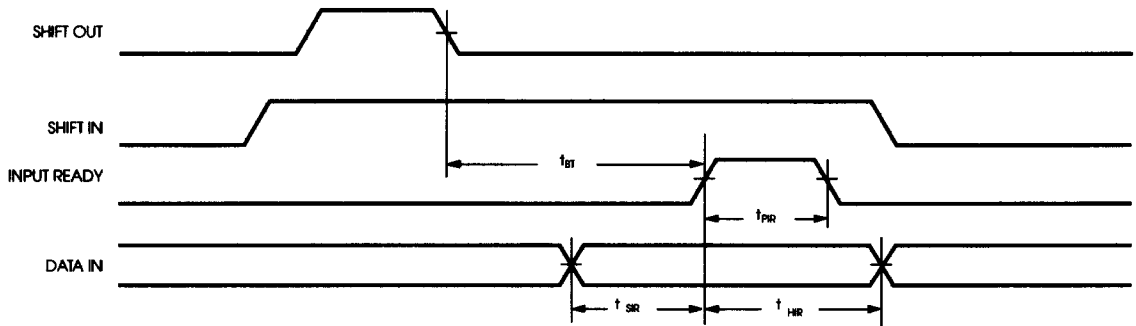


SWITCHING WAVEFORMS (CONTINUED)

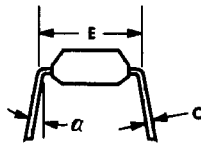
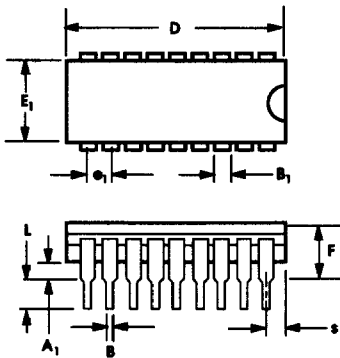
Bubblethrough Data In to Data Out Diagram (Cascadeable)



Bubblethrough, Data Out to Data In Diagram (Cascadeable)



PACKAGE DIMENSIONS

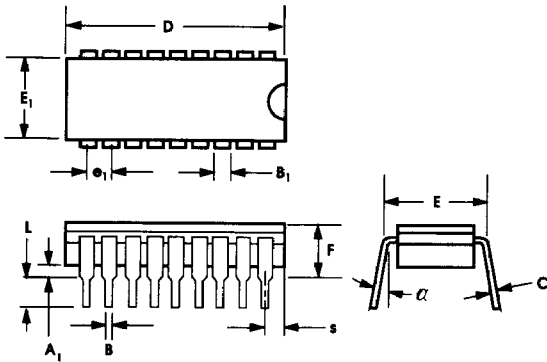


16/18 LEAD 300 MIL DIP

PARAMETER	16-PIN		18-PIN	
	MIN	MAX	MIN	MAX
A ₁	.015		.015	
B	.016	.020	.016	.020
B ₁	.045	.065	.045	.065
C	.010	.014	.008	.012
D	.740	.760	.890	.910
E	.280	.300	.280	.300
E ₁	.248	.252	.255	.265
e ₁	.100		.100	
F		.170		.170
L	.125	.145	.125	.135
s	.020	.030	.060	.070
α	0°	15°	0°	15°



PACKAGE DIMENSIONS (CONTINUED)



16/18 LEAD 300 MIL CERDIP

PARAMETER	16-PIN		18-PIN	
	MIN	MAX	MIN	MAX
A ₁	.015	.060	.015	.045
B	.014	.023	.014	.023
B ₁	.038	.065	.050	.065
C	.008	.015	.009	.015
D		.840		.920
E	.290	.320	.300	.320
E ₁	.220	.310	.285	.310
e ₁		.100		.100
F		.200		.200
L	.125	.200	.125	.200
s		.080		.080
α	0°	15°	0°	15°

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE		
			MIN	MAX	UNIT
SSL7401S-50PC	50MHz	16-Pin PDIP	0	+70	°C
SSL7401S-40PC	40				
SSL7401 -25PC	25				
SSL7401 -15PC	15				
SSL7401 -10PC	10				
SSL7401S-50CC	50MHz	16-Pin CERDIP			
SSL7401S-40CC	40				
SSL7401 -25CC	25				
SSL7401 -15CC	15				
SSL7401 -10CC	10				
SSL7401S-40CB	40MHz	16-Pin CERDIP	-55	+125	°C
SSL7401 -25CB	25				
SSL7401 -15CB	15				
SSL7401 -10CB	10				
SSL7402S-50PC	50MHz	18-Pin PDIP	0	+70	°C
SSL7402S-40PC	40				
SSL7402 -25PC	25				
SSL7402 -15PC	15				
SSL7402 -10PC	10				
SSL7402S-50CC	50MHz	18-Pin CERDIP			
SSL7402S-40CC	40				
SSL7402 -25CC	25				
SSL7402 -15CC	15				
SSL7402 -10CC	10				
SSL7402S-40CB	40MHz	18-Pin CERDIP	-55	+125	°C
SSL7402 -25CB	25				
SSL7402 -15CB	15				
SSL7402 -10CB	10				
SSL7403S-50PC	50MHz	16-Pin PDIP	0	+70	°C
SSL7403S-40PC	40				
SSL7403 -25PC	25				
SSL7403 -15PC	15				
SSL7403 -10PC	10				



ORDERING INFORMATION (CONTINUED)

PART NUMBER	SPEED	PACKAGE	TEMPERATURE RANGE		
			MIN	MAX	UNIT
SSL7403S-50CC	50MHz	16-Pin PDIP			
SSL7403S-40CC	40				
SSL7403 -25CC	25				
SSL7403 -15CC	15				
SSL7403 -10CC	10				
SSL7403S-40CB	40MHz	16-Pin Cerdip	-55	+125	°C
SSL7403 -25CB	25				
SSL7403 -15CB	15				
SSL7403 -10CB	10				
SSL7404S-50PC	50MHz	18-Pin PDIP	0	+70	°C
SSL7404S-40PC	40				
SSL7404 -25PC	25				
SSL7404 -15PC	15				
SSL7404 -10PC	10				
SSL7404S-50CC	50MHz	18-Pin Cerdip			
SSL7404S-40CC	40				
SSL7404 -25CC	25				
SSL7404 -15CC	15				
SSL7404 -10CC	10				
SSL7404S-40CB	40MHz	18-Pin PDIP	-55	+125	°C
SSL7404 -25CB	25				
SSL7404 -15CB	15				
SSL7404 -10CB	10				