

DD-03201

## 32- OR 96-CHANNEL DISCRETE-TO-DIGITAL INTERFACE "RXD3"



### DESCRIPTION

The DD-03201 is a discrete-to-digital interface device. The inputs have been designed to handle 28 V/Gnd, 28 V/Open, and Open/Gnd signals. The device can also be configured as either a 32 triple-redundant or 96 non-redundant discrete input with either a microprocessor and/or ARINC 429 output. The device can be HIRF protected by adding capacitors to the input resistor network.

The device uses comparators in a triple-redundant configuration to take a consensus of the input state and raise a flag when there is no consensus. The device's microprocessor output is an addressable 8-bit or 16-bit tri-state port, which selects channel data, status, bounce, built-in-self-test (BIST) and major fault. All are compatible with TTL logic.

### APPLICATIONS

The design specifically addresses redundancy, built-in self-test autonomy, fault isolation and tolerance at the chip level.

In the 96-channel mode the device loses the capability of taking consensus of the input states as well as mismatch. These features are triple-redundant configuration specific. All other features are still available.

These features, along with high-reliability and low cost, enable the device to serve a variety of interface requirements in aerospace applications, including flight critical, essential and non-essential functions. The optional ARINC 429 output port is particularly well-suited to data concentrator requirements.

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### FEATURES

- Universal Inputs - Configurable As:
  - 28 V/Gnd
  - Open/Gnd
  - 28 V/Open
  - Input Resistor Usage
- Built-In Self-Test
- Soft Failure Reporting
- Deferred Maintenance
- Higher MTBUR
- Optional ARINC 429 Output Port



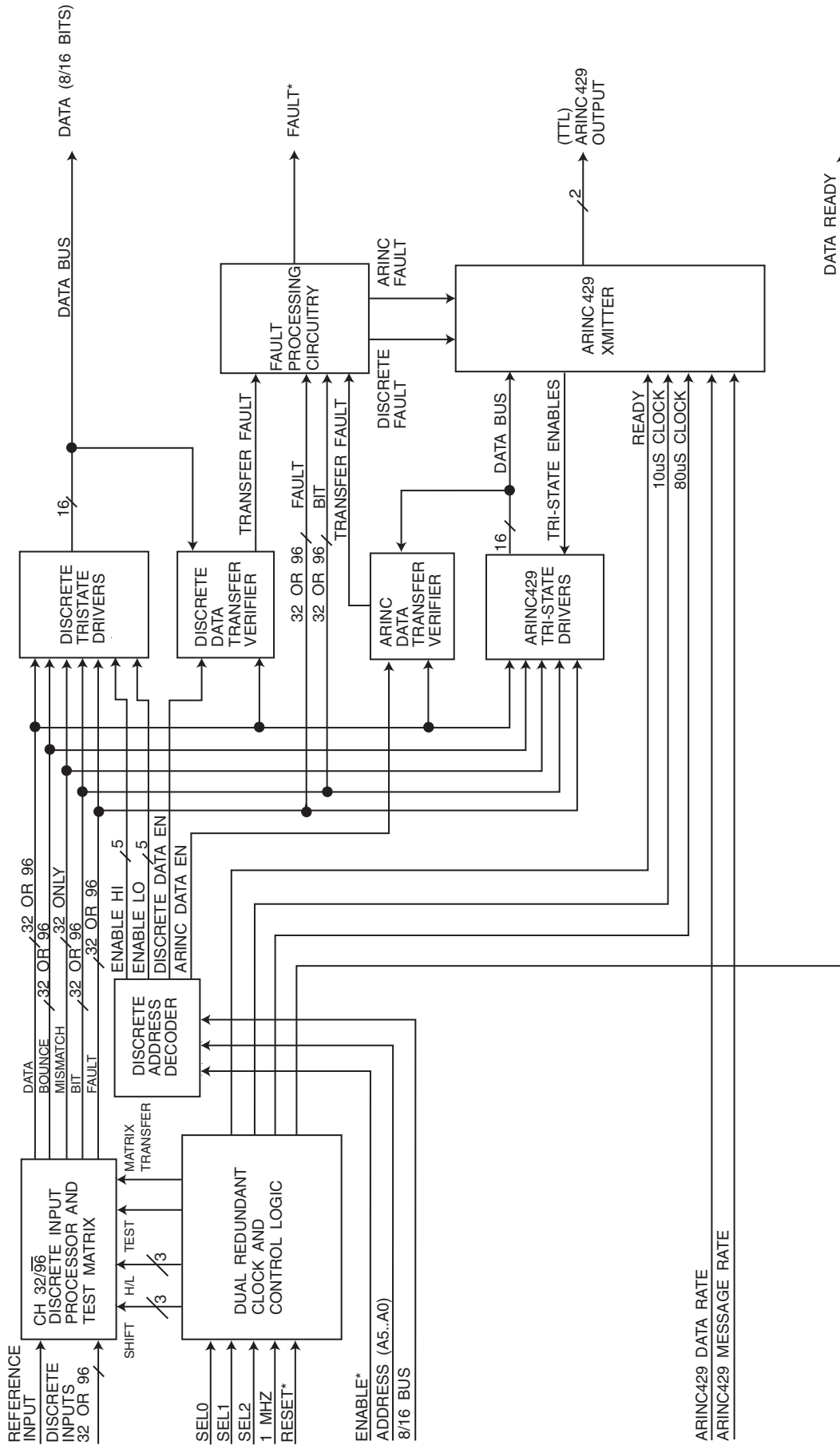
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Note: (\*) Indicates active low.

FIGURE 1. DD-03201 BLOCK DIAGRAM

**TABLE 1. DD-03201 SPECIFICATIONS**

| PARAMETER  | UNITS    | MIN  | TYP   | MAX                  |
|--|----------|--|-------|----------------------|
| <b>ABSOLUTE MAXIMUM RATINGS</b>                                    |          |  |       |                      |
| Supply Voltages (V <sub>DD</sub> )                                 | V        | -0.3   | 5.0   | 7.0                  |
| Analog Inputs  | V        | -0.3   |       | V <sub>DD</sub> +0.3 |
| Digital Inputs   | V        | -0.3   |       | V <sub>DD</sub> +0.3 |
| <b>OPERATING CONDITIONS</b>  |          |  |       |                      |
| Supply Voltages (V <sub>DD</sub> )                                 | V        | 4.5  |       | 5.5                  |
| <b>DIGITAL INPUTS/OUTPUTS</b>                                      |          |  |       |                      |
| Logic Compatibility  | TTL      |  |       |                      |
| Digital Inputs   |          |  |       |                      |
| ■ V <sub>IH</sub>  | V        | 2.0  |       |                      |
| ■ V <sub>IL</sub>  | V        |  |       | 0.8                  |
| Clock Inputs (See Note 1)  | MHz      | 0.99   | 1.00  | 1.01                 |
| Digital Outputs  |          |  |       |                      |
| ■ V <sub>OH</sub> (I <sub>OH</sub> = 4ma)                          | V        | 2.4  |       |                      |
| ■ V <sub>OH</sub> (I <sub>OH</sub> = -1ma)                         | V        | V <sub>DD</sub> -0.5                                 |       |                      |
| ■ V <sub>OL</sub> (I <sub>OL</sub> = 4ma)                          | V        |  |       | 0.4                  |
| <b>ANALOG INPUTS</b>   |          |  |       |                      |
| ■ Input currents:  |          |  |       |                      |
| Input channels   | µA       | -0.1   |       | 0.1                  |
| Reference inputs   | µA       | -1.0   |       | 1.0                  |
| Self-test inputs   | µA       | -1.0   |       | 1.0                  |
| ■ Input Offset Voltage:  |          |  |       |                      |
| Input channel to corresponding reference input                     | mV       | -15  |       | 15                   |
| ■ Input Common Mode Range:   |          |  |       |                      |
| Input channel and corresponding reference input                    | V        | V <sub>SS</sub>                                      |       | V <sub>DD</sub>      |
| <b>POWER SUPPLY REQUIREMENTS</b>                                   |          |  |       |                      |
| (Total V <sub>DD</sub> , Analog & Digital)                         |          |  |       |                      |
| I <sub>DD</sub> (V <sub>DD</sub> = +5V [Digital Outputs Unloaded]) | mA       |  | 25    | 45                   |
| <b>POWER DISSIPATION</b>   |          |  |       |                      |
| P <sub>D</sub>   | mw       |  | 125.0 | 250.0                |
| <b>THERMAL</b>   |          |  |       |                      |
| Operating Temperature  |          |  |       |                      |
| ■ Type 1   | °C       | -40  |       | 85                   |
| ■ Type 2   | °C       | -55  |       | 125                  |
| ■ Type 3   | °C       | 0  |       | 70                   |
| Storage Temp   | °C       | -65  |       | 150                  |
| Lead Temperature   |          |  |       |                      |
| (Localized, 1 sec. duration)                                       | °C       |  |       | 280                  |
| (Body, 2 sec. duration)  | °C       |  |       | 210                  |
| Junction Temperature   |          |  |       |                      |
| θ <sub>jc</sub>  | °C/W     |  | 5.0   |                      |
| θ <sub>ca</sub>  | °C/W     |  | 20.0  |                      |
| MTBF per MIL-Hbk 217 for airborne Inhabited Cargo at 64°C          |          | 96-Channel: 269,326 hrs.<br>32-Channel: 332,742 hrs. |       |                      |
| <b>PHYSICAL CHARACTERISTICS</b>                                    |          |  |       |                      |
| Size   | in. (mm) | 1.1 x 1.1<br>28 x 28                                 |       |                      |
| Weight   | oz. (g)  | 1.0<br>26.0  |       |                      |
| Moisture Sensitivity Level   |          | MSL-3  |       |                      |

Note: For the ARINC 429 option the bit rate is derived from the clock. Refer to ARINC 429 Bit Rate to avoid interference. ARINC 429-14 (January 4, 1993), paragraph 2.4.: "Timing Related Elements" contains a "Commentary" section following subparagraph 2.1.4.2 ("Low Speed Operation") that cautions against using "precisely" 100 kilobits per second.

**WHAT IS A DISCRETE?**

Advisory Circular (FAA), Airworthiness Approval of Traffic Alert and Collision Avoidance Systems (TCAS II) and Mode S Transponders, AC20-131, defines a discrete as "a separate, complete and distinct signal." In many instances these signals are binary, on or off, 28 V-based signals; they are typically Open/Gnd, 28 V/Open, or 28 V/Gnd with very low bandwidth (DC to 200 Hz).

While on the surface the translation of these signals to TTL-levels compatible with digital avionics may seem simple, RTCA DO-160C power, lighting and high-intensity-radiated-fields (HIRF) are complicating factors. Add to that the desire to have a standardized, addressable, reliable interface and the challenge becomes apparent.

Today's systems address the interface with circuits tailored for each interface comprised of R-C input filters, divider networks, diode isolation and comparators. Multichannel interface to a processor requires additional logic and latches. The resulting circuit generally lacks any built-in test capability, consumes considerable pc-board real estate (up to one sq. in. per channel), and offers no chip-level redundancy.

**FUNCTIONAL INTEGRATION**

Using the aggregated definition and functional requirements of industry, Data Device Corporation has developed a programmable 32/96-channel discrete interface with inputs capable of handling 28 V/Open, Open/Gnd and 28 V/Gnd signals. When using the 32-channel mode, the design uses comparators in a triple-redundant configuration, so that each channel will take a consensus of the input state, and raise a flag when there is no consensus (consensus fails). The device's output is a selectable 8-bit or 16-bit tri-state port, which can be addressed for channel data, status, bounce, built-in-self-test and major fault information.

This design specifically addresses built-in self-test autonomy, fault isolation and tolerance; moreover, its functional integration results in significant added reliability. A comparative look at MTBF calculated in accordance with MIL-HBK-217 for airborne inhabited cargo environments at 64°C indicates an order of magnitude improvement for an integrated approach vs. a similarly packaged discrete-component implementation. Moreover, the real estate is reduced from 32 square inches to 1.21 square inches for a 32-channel and from 64 square inches to 1.21 square inches for the 96-channel device.

Additional key features include:

**FAULT ISOLATION:** In 32-channel mode, triple-redundant comparators are physically located on three different edges of the custom chip so that an edge failure is not catastrophic.

**FAULT TOLERANCE:** In 32-channel mode, a single comparator failure is reported as a mismatch or BIT fault, but does not result in a hard-failure.

**BOUNCE:** Relays and switches, as mechanical devices, have a characteristic 'bounce' to their signal transition. It is desirable to mask this bounce by delaying the output digital transition accordingly. This sampling rate of the device can be varied to allow for debounce of relay/switch inputs. In addition, the triple sampling of a given comparator enables a consistent reading of otherwise asynchronous signals. Bounce is an addressable register that allows the user to detect bouncing or intermittent relays/switches.

**REGISTERS:** 8-bit or 16-bit selectable data or status is available via tri-state buffers for interface to any system processor.

**OPTIONAL ARINC 429 PORT:** A serial ARINC 429 output is available for data concentrator applications. This enables the transfer of data to other systems with a minimum of wiring and processor loading.

**TEST PATTERNS:** Internal Test Patterns can be selected to produce alternating '1's and '0's to verify that all address and data bits are operational. These outputs are always available, **regardless** of READY state. They must be addressed by the user (A5...A0) in accordance with TABLES 3 and 4.

**DISSIMILAR PATHS:** Errors are reported through registers and the optional ARINC 429 port as crosschecks.

**DEFERRED MAINTENANCE:** The error reporting scheme differentiates soft- and hard-failures to allow continued operation despite failures.

**INTELLIGENCE:** The device's built-in self-test, status reporting scheme and fault-tolerance/isolation significantly reduces application software requirements. FIGURE 1 illustrates the model DD-03201 functional block diagram.

## MICROPROCESSOR INTERFACE

### READ CYCLE TIMING

The DD-03201 is configured with either an 8-bit or a 16-bit microprocessor. FIGURE 2 illustrates this interface.

The read cycle(s) should be preceded by polling the device's READY bit which is located within the Status Register. The Status Register can be read at any time regardless of the state of the READY signal (pin 150) from the device.

If the READY bit is a logic "1" (this can be easily tested by a branch if negative statement) the address of the desired register, along with the negative true **ENABLE** signal, should be presented to the device. The additional data will be available within 100 nsec.

After the data is read the **ENABLE** line should be returned to a logic "1" level.

All of the data within the device is guaranteed to remain stable for at least 20  $\mu$ sec after the high-to-low transition of the READY signal (See FIGURE 3).

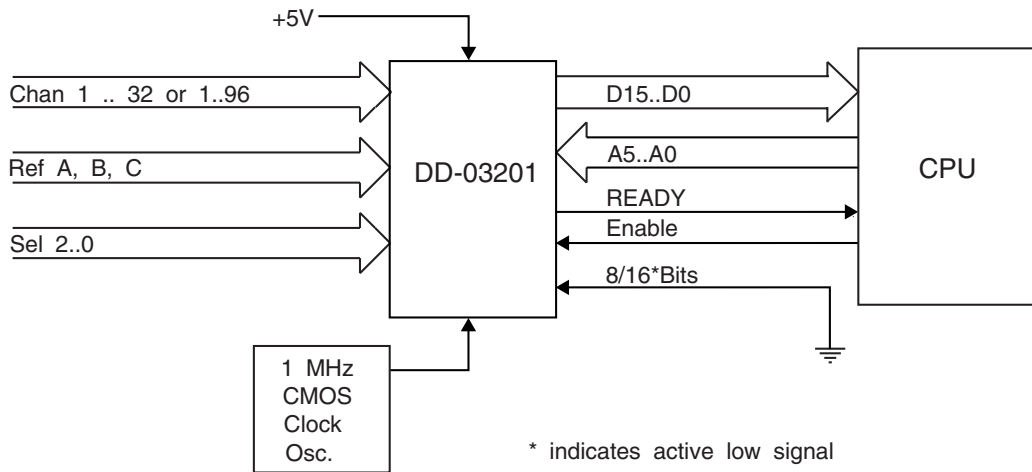
### ANALOG INPUTS

FIGURE 4 illustrates the architecture of the analog input and front-end self-test circuits. Each group of 32-channels (A, B and C groups) are identically configured, with REF\_A setting the threshold for the 'A' group of comparators, REF\_B setting the threshold for the 'B' group, etc. During the self-test portion of each cycle, the comparator inputs are switched from the NORMAL to the TEST position, an alternating 1/0 (HI/LO) pattern is applied to each group of comparators and a functional test is performed. The test is then repeated with an alternating 0/1 (LO/HI) pattern.

**INPUT CHANNELS:** (Pins 4-19, 22-37, 44-59, 62-77, 81-96 and 99-114) Configured as three groups of 32-channels each; each group is associated with its own reference and self-test inputs. The device may be connected as 96-independent channels or 32-triple-redundant channels. Refer to FIGURE 5 and FIGURE 6 for a typical example of each configuration. For 32-channel operation, "Channel 1" drives the A1, B1 and C1 inputs, "Channel 2" drives the A2, B2 and C2 inputs, and so forth. The example in FIGURE 5 shows redundant input networks that provide isolation between ASIC input pins and protect the two working channel sections in the event of a short from an ASIC input pin to ground or  $V_{DD}$  on the the third section.

**REFERENCE INPUTS:** (Pins 39, 79 and 116) Each reference input sets the threshold voltage for the corresponding group of 32 comparators.

**SELF-TEST INPUTS:** (Pins 38, 40, 78, 80, 115 and 117) High and low self-test threshold settings. These settings should be set to at least 100 mV above (HI) and 100 mV below (LO) the reference (REF) input for the corresponding group of 32 comparators.



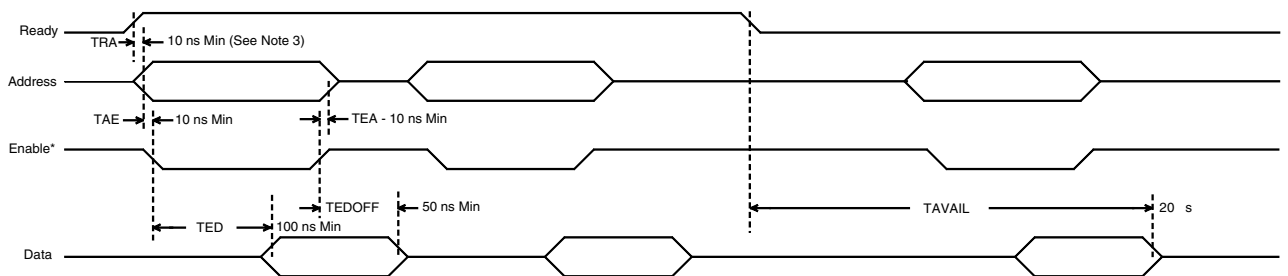
NOTE: 1) If 8/16\* Bits pin is tied to +5 Volts, then the DD-03201 is configured for 8-Bit Mode.

The following must also be modified:

- D0 tied to D8
- D1 tied to D9
- D2 tied to D10
- D3 tied to D11
- D4 tied to D12
- D5 tied to D13
- D6 tied to D14
- D7 tied to D15

2) If the ARINC 429 option is not used, then pin 156 (429STRBI) MUST be grounded for the "bounce" circuit to operate properly.

**FIGURE 2. DD-03201 TO CPU INTERFACE**



- Note:
- 1) TRA = Time Ready Address
  - 2) TAE = Time Address Enable
  - 3) TEA = Time Enable to Address
  - 4) TED = Time Enable Data
  - 5) TEDOFF = Time Enable Off - Data Off
  - 6) TAVAIL = Time Ready\* - Data Available
  - 7) (\*) Indicates active low.
  - 8) The ready "on-time" = (sample rate - 440 s)
- Sample rate is programmable via SEL0 - SEL2 (See TABLE 2)

**FIGURE 3. READ CYCLE TIMING**

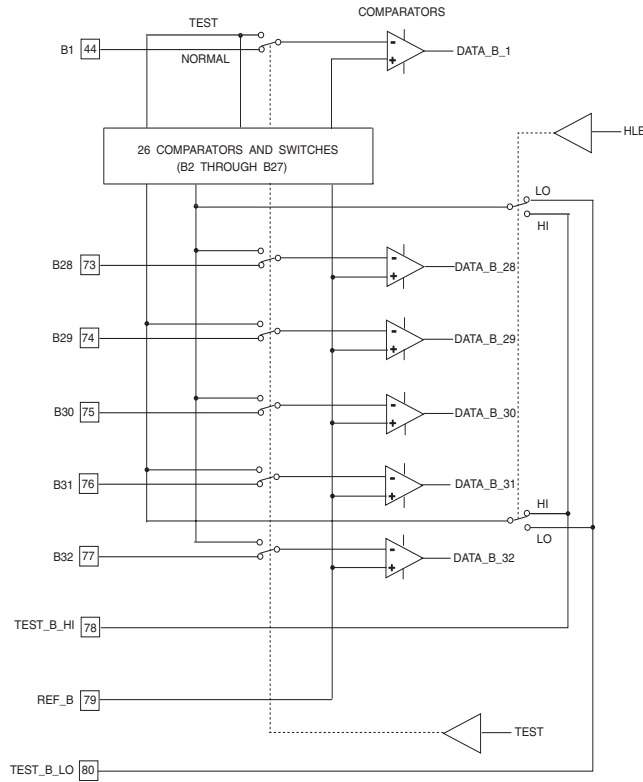


FIGURE 4. DD-03201 (ASIC) INPUT STRUCTURE

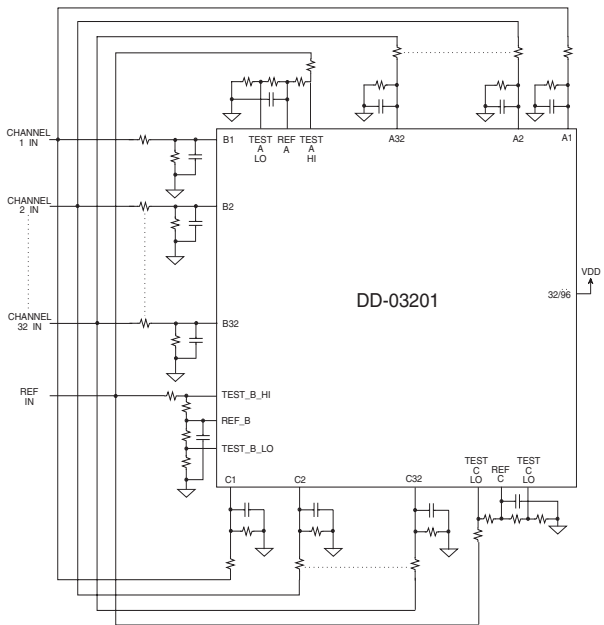


FIGURE 5. DD-03201 32-CHANNEL CONFIGURATION

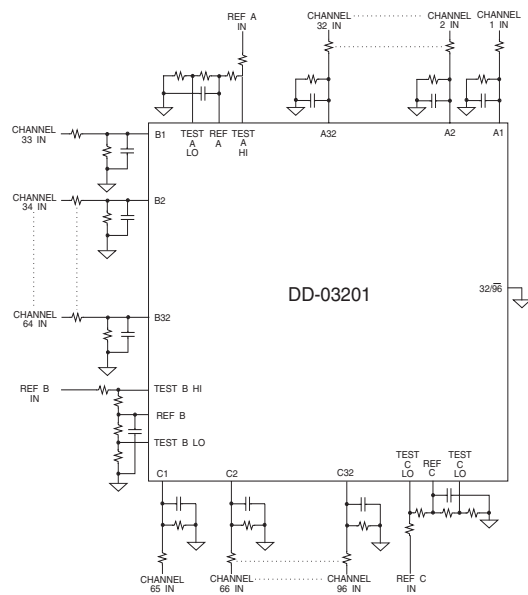


FIGURE 6. DD-03201 96-CHANNEL CONFIGURATION

## DIGITAL INPUTS

**DEBOUNCE (SEL2...SEL0):** (Pins 1-3) The Input Discrete Sampling Rate (Debounce Time) is user-programmable via the three Select lines (SEL2...SEL0) in accordance with TABLE 2. The intent of this function is to mask the bounce of the input discrete appropriate to its characteristic performance. See **BOUNCE** on page 4.

| TABLE 2. DISCRETE SAMPLING RATE |             |
|---------------------------------|-------------|
| SELECT<br>(SEL 2.. SEL 0)       | SAMPLE RATE |
| 000                             | 5 msec      |
| 001                             | 10 msec     |
| 010                             | 20 msec     |
| 011                             | 50 msec     |
| 100                             | 100 msec    |
| 101                             | 200 msec    |
| 110                             | 500 msec    |
| 111                             | 1000 msec   |

**ENABLE:** (Pin 149) The **ENABLE** line controls the tri-state drivers of the 8- or 16-bit Data Bus outputs. The tri-state Data Bus drivers are enabled when this signal is a logic "0", and are tri-stated when this signal is a logic "1". **ENABLE** is a read signal and should only be low during read cycles.

**8/16 BITS:** (Pin 119) A logic "0" selects the 16-bit data bus output and logic "1" selects the 8-bit data bus output.

**ADDRESS LINES (A5...A0):** (Pins 143-148) The six address lines (A5...A0, where A0 is the LSB) provide for the selection of the desired 8- or 16-bit data bus information in accordance with TABLE 5 and TABLE 6 (Word/Byte Modes).

**CLKA and CLKB (1MHz CLK):** (Pins 160 and 121) Dual redundant input clock paths are provided to the ASIC at two widely separated points to improve operational reliability. The 1 MHz clock should be connected to both CLKA and CLKB inputs (exact frequency and stability is important only to the serial bit rate of the ARINC 429 port, see NOTE 1, TABLE 1). Optional isolation resistors (200 ohms maximum) may be installed in series with each input to facilitate testing of the clock monitoring circuitry (see FIGURE 7). In the event of loss of CLKA (primary) input to ASIC, internal circuitry combined with external RC networks (see **A TIMER and B TIMER**) switches to the CLKB (secondary) source. Both clocks are continuously monitored for status and this information is available as separated bits in the Status Register.

**A TIMER and B TIMER:** (Pins 124 and 123) Clock monitoring and switching depends upon RC networks installed at these two pins (FIGURE 7). Each pin must have a 100 k $\Omega$ , 5% resistor to VDD and a 0.001  $\mu$ F, 20% capacitor to ground.

**FACTORY TEST INPUTS:** (Pins 41, 42, 152 and 153) The **TMUX**, **TMODE**, **FMUX** and **FMODE** input signals are used for factory testing and should be tied to logic "1" for the device to operate properly.

**RESET:** (Pin 43) The **RESET** signal is used to reset the device during factory testing. It must be connected to an external RC network (100 k $\Omega$ , 5% resistor to VDD and a 0.01  $\mu$ F, 20% capacitor to ground) to provide a Power-on-Reset for the device. If there is some reason to reset the device from external circuitry this pin can be momentarily pulled to logic "0" through an open collector device. **Do not hard wire this pin to +5V or ground.**

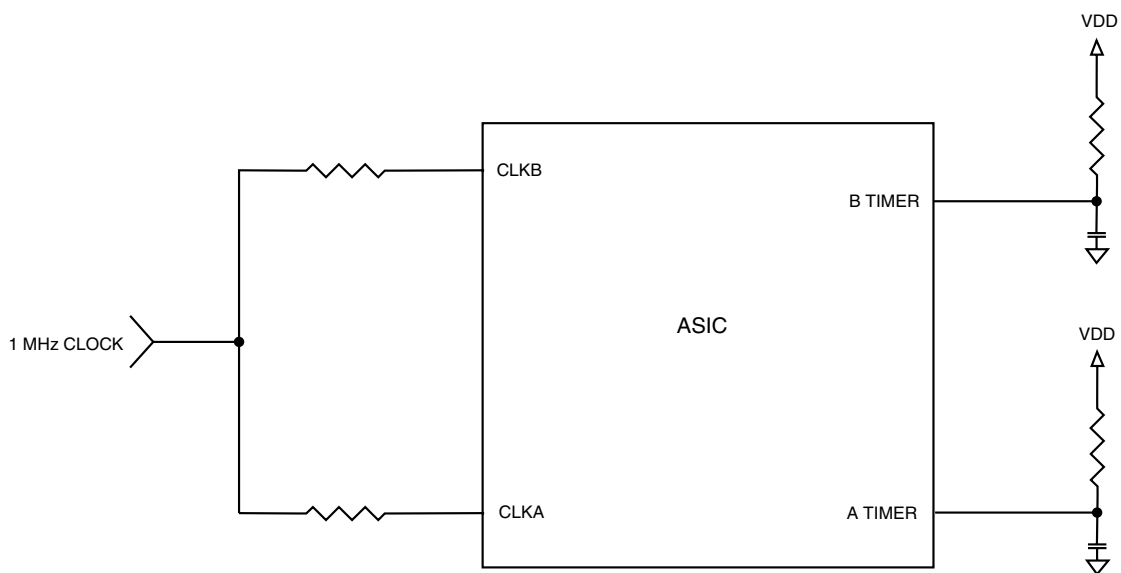


FIGURE 7. DD-03201 CLOCK INPUTS AND TIMERS

| TABLE 3. 32-CHANNEL WORD MODE (16-BIT BUS) |                          |
|--|--------------------------|
| ADDRESS (A5...A0)                          | DATA (D7...D0)           |
| 00 000X                                    | BOUNCE CH 16..CH_01      |
| 00 001X                                    | BOUNCE CH 32..CH 17      |
| 00 010X                                    | MISMATCH CH_16..CH_01    |
| 00 011X                                    | MISMATCH CH_32..CH 17    |
| 00 100X                                    | BIT CH_16..CH_01         |
| 00 101X                                    | BIT CH 32 CH_17          |
| 00 110X                                    | FAULT CH_16 CH 01        |
| 00 111X                                    | FAULT CH_32 CH 17        |
| 01 000X                                    | DATA CH 16 CH_01         |
| 01 001X                                    | DATA CH 32 CH_17         |
| 01 010X                                    | TEST PATTERN 0's and 1's |
| 01 011X                                    | STATUS REGISTER          |
| 01 100X                                    | FACTORY TEST WORD 1      |
| 01 101X                                    | FACTORY TEST WORD 2      |
| 01 110X                                    | FACTORY TEST WORD 3      |
| 01 111X                                    | FACTORY TEST WORD 4      |
| 10 000X                                    | NOT USED                 |
| 10 001X                                    | NOT USED                 |
| 10 010X                                    | NOT USED                 |
| 10 011X                                    | NOT USED                 |
| 10 100X                                    | NOT USED                 |
| 10 101X                                    | TEST PATTERN 1's and 0's |
| 10 110X                                    | NOT USED                 |
| 10 111X                                    | :                        |
| 11 111X                                    | NOT USED                 |

| TABLE 4. 32-CHANNEL BYTE MODE (8-BIT BUS) |                          |
|---|--------------------------|
| ADDRESS (A5...A0)                         | DATA (D7...D0)           |
| 00 0000                                   | BOUNCE CH_08 CH_01       |
| 00 0001                                   | BOUNCE CH_16 CH_09       |
| 00 0010                                   | BOUNCE CH_24 CH_17       |
| 00 0011                                   | BOUNCE CH 32 CH 25       |
| 00 0100                                   | MISMATCH CH_08 CH_01     |
| 00 0101                                   | MISMATCH CH_16 CH_09     |
| 00 0110                                   | MISMATCH CH_24 CH_17     |
| 00 0111                                   | MISMATCH CH_32 CH_25     |
| 00 1000                                   | BIT CH_08 CH_01          |
| 00 1001                                   | BIT CH_16 CH 09          |
| 00 1010                                   | BIT CH_24 CH_17          |
| 00 1011                                   | BIT CH_32 CH_25          |
| 00 1100                                   | FAULT CH_08 CH_01        |
| 00 1101                                   | FAULT CH_16 CH_09        |
| 00 1110                                   | FAULT CH_24 CH_17        |
| 00 1111                                   | FAULT CH_32 CH_25        |
| 01 0000                                   | DATA CH_08 CH_01         |
| 01 0001                                   | DATA CH_16 CH_09         |
| 01 0010                                   | DATA CH_24 CH_17         |
| 01 0011                                   | DATA CH_32 CH_25         |
| 01 0100                                   | TEST PATTERN 0's and 1's |
| 01 0100                                   | TEST PATTERN 0's and 1's |
| 01 0110                                   | STATUS REGISTER LO       |
| 01 0111                                   | STATUS REGISTER HI       |
| 01 1000                                   | FACTORY TEST WORD 1 LO   |
| 01 1001                                   | FACTORY TEST WORD 1 HI   |
| 01 1010                                   | FACTORY TEST WORD 2 LO   |
| 01 1011                                   | FACTORY TEST WORD 2 HI   |
| 01 1100                                   | FACTORY TEST WORD 3 LO   |
| 01 1101                                   | FACTORY TEST WORD 3 HI   |
| 01 1110                                   | FACTORY TEST WORD 4 LO   |
| 01 1111                                   | FACTORY TEST WORD 4 HI   |
| 10 0000                                   | NOT USED                 |
| 10 0001                                   | NOT USED                 |
| 10 0010                                   | NOT USED                 |
| 10 0011                                   | NOT USED                 |
| 10 0100                                   | NOT USED                 |
| 10 0101                                   | NOT USED                 |
| 10 0110                                   | NOT USED                 |
| 10 0111                                   | NOT USED                 |
| 10 1000                                   | NOT USED                 |
| 10 1001                                   | NOT USED                 |
| 10 1010                                   | TEST PATTERN 1's and 0's |
| 10 1011                                   | TEST PATTERN 1's and 0's |
| 10 1100                                   | NOT USED                 |
| 10 1101                                   | :                        |
| 11 1111                                   | NOT USED                 |

**NOTES FOR TABLES 3 AND 4.**

- Note 1: A true BOUNCE bit indicates that the input signal of the associated channel changed in an alternating fashion, i.e., OFF-ON-OFF or ON-OFF-ON in three successive samples at the selected sampled rate.
- Note 2: A MISMATCH bit that is true indicates that one of the triple-redundant inputs of the associated channel did not agree with the other two for three consecutive samples of the input i.e., there was a lack of consensus for the three inputs. A MISMATCH indication is a SOFT FAULT condition indicating that there is a problem with the channel but the associated output data can be believed because of the internal voting taking place.
- Note 3: A BIT indication for any channel signifies that the associated channel has failed the Built-In-Test sequence which is performed prior to every input sample taken. These signals are reset at the start of each Built-In-Test sequence, and will be set if any of the tests in the sequence fail. A BIT indication is a HARD FAULT condition indicating that the Built-in-Test has failed one or more of the voltage tests.
- Note 4: A FAULT bit that is true indicates that the associated channel has a major problem and the associated data should not be believed. A FAULT is a HARD FAULT condition.
- Note 5: A DATA bit indicates the triple-redundant vote or unanimous consensus of the input discrete state for the associated channel over the last two data samples taken.
- Note 6: The two available TEST PATTERNS contain an alternating string of 1's and 0's, and 0's and 1's, which can be used to verify that all of the data bits are operational, i.e., there are no stuck bits. The two test patterns have been located at addresses of alternating address bits so that the address decoder bits are tested at the same time.

See Notes at left.

**TABLE 5. 96-CHANNEL WORD MODE (16-BIT BUS)**

| ADDRESS (A5...A0) | DATA (D7...D0)           |
|-------------------|--------------------------|
| 00 000X           | BOUNCE CH_16..CH_01      |
| 00 001X           | BOUNCE CH_32..CH_17      |
| 00 010X           | BOUNCE CH_48..CH_33      |
| 00 011X           | BOUNCE CH_64..CH_49      |
| 00 100X           | BOUNCE CH_80..CH_65      |
| 00 101X           | BOUNCE CH_96..CH_81      |
| 00 110X           | FAULT CH_16..CH_01       |
| 00 111X           | FAULT CH_32..CH_17       |
| 01 000X           | FAULT CH_48..CH_33       |
| 01 001X           | FAULT CH_64..CH_49       |
| 01 010X           | TEST PATTERN 0's and 1's |
| 01 011X           | FAULT CH_80..CH_65       |
| 01 100X           | FAULT CH_96..CH_81       |
| 01 101X           | DATA CH_16..CH_01        |
| 01 110X           | DATA CH_32..CH_17        |
| 01 111X           | DATA CH_48..CH_33        |
| 10 000X           | DATA CH_64..CH_49        |
| 10 001X           | DATA CH_80..CH_65        |
| 10 010X           | DATA CH_96..CH_81        |
| 10 011X           | NOT USED                 |
| 10 100X           | STATUS REGISTER          |
| 10 101X           | TEST PATTERN 1's and 0's |
| 10 110X           | FACTORY TEST WORD 1      |
| 10 111X           | FACTORY TEST WORD 2      |
| 11 000X           | FACTORY TEST WORD 3      |
| 11 001X           | FACTORY TEST WORD 4      |
| 11 010X           | NOT USED                 |
| 11 011X           | :                        |
| 11 111X           | NOT USED                 |

**NOTES FOR TABLES 5 AND 6:**

Note 1: A true BOUNCE bit indicates that the input signal of the associated channel changed in an alternating fashion i.e. OFF-ON-OFF or ON-OFF-ON in three consecutive samples at the selected sample rate.

Note 2: A FAULT bit that is true indicates that the associated channel has a major problem and the associated data should not be believed. A FAULT indication is a HARD FAULT condition.

Note 3: A DATA bit indicates the input discrete state for the associated channel over two out of the last three samples taken.

Note 4: The two available TEST PATTERNS contain an alternating string of '1's and '0's and '0's and '1's, which can be used to verify that all of the data bits are operational, i.e., there are no stuck bits. The two test patterns have been located at addresses of alternating address bits so that the address decoder bits are tested at the same time.

**TABLE 6. 96-CHANNEL BYTE MODE (8-BIT BUS)**

| ADDRESS (A5...A0) | DATA (D7...D0)           |
|-------------------|--------------------------|
| 00 0000           | BOUNCE CH_08..CH_01      |
| 00 0001           | BOUNCE CH_16..CH_09      |
| 00 0010           | BOUNCE CH_24..CH_17      |
| 00 0011           | BOUNCE CH_32..CH_25      |
| 00 0100           | BOUNCE CH_40..CH_33      |
| 00 0101           | BOUNCE_48 CH_41          |
| 00 0110           | BOUNCE_56..CH_49         |
| 00 0111           | BOUNCE_64 CH_57          |
| 00 1000           | BOUNCE 73..CH_65         |
| 00 1001           | BOUNCE 80 CH_74          |
| 00 1010           | BOUNCE 88..CH_81         |
| 00 1011           | BOUNCE 96 CH_89          |
| 00 1100           | FAULT CH_08..CH_01       |
| 00 1101           | FAULT CH_16 CH_09        |
| 00 1110           | FAULT CH_24..CH_17       |
| 00 1111           | FAULT CH_32..CH_25       |
| 01 0000           | FAULT CH_40..CH_33       |
| 01 0001           | FAULT CH_48..CH_41       |
| 01 0010           | FAULT CH_56..CH_49       |
| 01 0011           | FAULT CH_64..CH_57       |
| 01 0100           | TEST PATTERN 0's and 1's |
| 01 0101           | TEST PATTERN 0's and 1's |
| 01 0110           | FAULT CH_73..CH_65       |
| 01 0111           | FAULT CH_80..CH_74       |
| 01 1000           | FAULT CH_88..CH_81       |
| 01 1001           | FAULT CH_96..CH_89       |
| 01 1010           | DATA CH_08..CH_01        |
| 01 1011           | DATA CH_16..CH_09        |
| 01 1100           | DATA CH_24..CH_17        |
| 01 1101           | DATA CH_32..CH_25        |
| 01 1110           | DATA CH_40..CH_33        |
| 01 1111           | DATA CH_48..CH_41        |
| 10 0000           | DATA CH_56..CH_49        |
| 10 0001           | DATA CH_64..CH_57        |
| 10 0010           | DATA CH_72..CH_65        |
| 10 0011           | DATA CH_80..CH_73        |
| 10 0100           | DATA CH_88..CH_81        |
| 00 1010           | DATA CH_96..CH_89        |
| 10 0110           | NOT USED                 |
| 10 0111           | NOT USED                 |
| 10 1000           | STATUS REGISTER LO       |
| 10 1001           | STATUS REGISTER HI       |
| 10 1010           | TEST PATTERN 1's and 0's |
| 10 1011           | TEST PATTERN 1's and 0's |
| 10 1100           | TEST WORD 1 LO           |
| 10 1101           | TEST WORD 1 HI           |
| 10 1110           | TEST WORD 2 LO           |

See Notes at left.

## OUTPUTS

**DATA (D15...D0):** (Pins 125-140) 8-bit byte or 16-bit byte word information is available on the Data Bus depending on the logic state of the BUS Select line as described above. In the Byte mode the upper and lower Bytes are enabled separately so that bit 0 can be hard wired to bit 8, bit 1 to bit 9 etc., thereby providing an 8-bit data bus.

It is important that the 8-bit mode be selected if these data bits are wired together, otherwise corrupted data will result. The available data can be found under ADDRESS LINES (A5...A0).

**FAULT:** (Pin 151) The **FAULT** flag was designed to serve as an interrupt to the microprocessor when a HARD or SOFT error has been detected within the device (See BIT and FAULT notes in TABLE 4). If this signal is asserted (logic "0") the Status Register should be read to determine the nature of the fault. Thereafter more detailed information can be found in the associated addressable registers. The Fault Flag will remain at a logic "0" for as long as the fault condition persists. FIGURE 8 and FIGURE 9 illustrate the fault logic tree for the 32-channel and the 96-channel respectively.

**Note:** Depending on the exact nature of the fault, the Fault Flag may return to logic "0" during the Built-In-Test interval (when the READY signal is at logic "0") if there is a persistent fault condition.

### FAULT CONDITIONS:

FAULT is logic "0" for any of the following fault conditions. The reason for the fault can be obtained from the status register which is accessible **regardless** of READY state. TABLE 7 shows the contents of the status register.

The status register is latched and cleared automatically when read. However, individual channel faults will be cleared upon the next sample taken by the internal sequencer. The time needed to read an individual channel fault before it could get cleared is based on the sample rate chosen by the user. Worst case would be 5ms.

A definition of each bit is as follows:

**BIT FAULT:** A logic "1" for this bit indicates that one of the channels has failed the Built-In-Test sequence. The offending channel(s) can be determined by reading the associated BIT data words.

**DISCRETE FAULT:** A logic "1" for this bit indicates that one of the channels detected a HARD failure during the Built-In-Test sequence, or that the discrete input data word did not transfer to the data bus output properly when it was read. If a HARD fault was detected the offending channel can be determined by reading the associated FAULT data registers. If it was generated by a transfer error the DISCRETE TRANSFER FAULT bit in this status register will be set to logic "1".

**ARINC FAULT:** A logic "1" for this bit indicates that one of the channels detected a HARD failure during Built-In-Test sequence,

or that the discrete input word did not transfer to the ARINC transmitter section properly.

If a HARD fault was detected the offending channel can be determined by reading the associated FAULT data registers. If it was generated by a transfer error then no FAULT bits will be set to logic "1".†

**ARINC READY:** A logic "0" for this bit indicates that an ARINC transmission is currently in progress. A logic "1" indicates that no ARINC transmission is in progress.†

**CLOCK\_A FAULT:** A logic "1" for this bit indicates that the primary 1 MHz clock is currently defective and that the device is running off the secondary 1 MHz clock. †

**CLOCK\_B FAULT:** A logic "1" for this bit indicates that the secondary 1 MHz clock is currently defective and cannot be used as a backup.

**NO CLOCK:** A logic "1" for this bit indicates that there is no 1 MHz clock being supplied to the device (or that both have failed).

**DISCRETE TRANSFER FAULT:** A logic "1" for this bit indicates that the discrete data word(s) did not transfer properly during the associated microprocessor read cycle, i.e., the word present on the data bus did not agree with internal data. The most likely cause of this type of fault condition is a collision on the data bus during the read cycle.

**Note:** This condition is only monitored for the discrete data words, not for all of the available data.

**READY:** A logic "1" for this bit indicates that all of the available data is stable and can be read. A logic "0" indicates that the device is in Built-In-Test mode, or taking a sample of discrete input data lines.

The signal should be polled directly by reading the status word prior to performing any read cycles. The internal data is guaranteed to be stable for 20 µsec after the logic "1" to logic "0" transition (READY to NOT READY) of this signal. Therefore, it should not be necessary to repoll the signal after the read.

**TABLE 7. STATUS REGISTER WORD BIT MAP**

| BIT      | SIGNAL    | BIT      | SIGNAL                  |
|----------|-----------|----------|-------------------------|
| 15 (MSB) | READY     | 07       | DISCRETE TRANSFER FAULT |
| 14       | LOGIC LOW | 06       | NO CLOCK                |
| 13       | LOGIC LOW | 05       | CLOCK_B FAULT           |
| 12       | LOGIC LOW | 04       | CLOCK_A FAULT           |
| 11       | LOGIC LOW | 03       | ARINC READY             |
| 10       | LOGIC LOW | 02       | ARINC FAULT             |
| 09       | LOGIC LOW | 01       | DISCRETE FAULT          |
| 08       | LOGIC LOW | 00 (LSB) | BIT FAULT               |

Note: All bits available regardless of ready-state.

† This signal is only meaningful for the ARINC 429 device option.



**ARINC 429 PORT (OPTIONAL)**

DD-03201XX-XX4 indicates the inclusion of the ARINC 429 data output. This option enables the transmission of discrete data via serial ARINC 429 (CMOS levels) output lines. The following features and pins apply:

**ARINC 429 DATA RATE (429DRATE):** (Pin 159) A logic “1” (or a no-connect) for this input selects the ARINC 429 Low Speed data rate of 12.5 kHz. A logic “0” selects the High Speed data rate of 100 kHz.†

**ARINC 429 MESSAGE RATE (429MRATE):** (Pin 158) The message rate of the ARINC output is selectable at either a fixed 100 msec rate or at the selected sampling rate of the input discrettes. A logic “1” selects the input sampling rate as the message rate, and a logic “0” selects the fixed 100 msec message rate.

**Note:** Table 8 takes both the transmit speed and amount of data to be sent into account and arrives at a maximum supported sampling rate for that combination of operating parameters. The ARINC message will be truncated if a rate that is faster than the maximum sampling rate indicated below is selected.

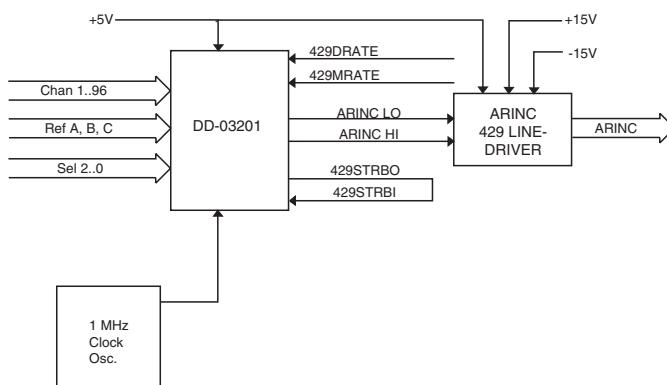
**429 STROBE IN (429STRBI):** (Pin 156) This pin is utilized in the special case where the device is being used as a remote ARINC 429 serial port and is not connected to a local microprocessor. When the device is being used in this specific configuration the associated 429 Strobe Out should be connected to this pin. In other cases this pin **must** be grounded.

**Related Information:** Because the BOUNCE data is momentary, it is latched within the device. This information is normally reset by a READ to the associated BOUNCE data words. In the instance where there is no microprocessor, and therefore no READS to the BOUNCE data, this connection provides a mechanism to reset the source of the BOUNCE information (just after it is transferred to the ARINC transmitter section) at the start of each ARINC message.†

**429 STROBE OUT (429STRBO):** (Pin 157) This signal is used in conjunction with the “429 Strobe In” described in the preceding paragraph. It is a 500 nsec positive pulse which occurs at the start of each 429 message. For further information concerning the use of this signal see 429 STROBE IN (429STRBI).†

**TABLE 8. MAXIMUM SUPPORTED SAMPLING RATE**

| SPEED MODE      | # OF INPUT CHANNELS | # OF ARINC LABELS | APPROX TIME TO TRANSMIT ARINC MESSAGE (IN MSEC) | FASTEST SUPPORTED DISCRETE SAMPLING RATE ( IN MSEC) |    |    |    |     |
|-----------------|---------------------|-------------------|---|---|----|----|----|-----|
|                 |                     |                   |   | 5   | 10 | 20 | 50 | 100 |
| High (100k bps) | 96                  | 20                | 7.2   |   | X  |    |    |     |
| Low (12.5k bps) | 96                  | 20                | 57.6  |   |    |    |    | X   |
| High (100k bps) | 32                  | 12                | 4.3   | X   |    |    |    |     |
| Low (12.5k bps) | 32                  | 12                | 34.6  |   |    |    | X  |     |



NOTE: 1) 429 MRATE and DRATE can either be tied to gnd or +5V (Refer to Page 12)

2) If the ARINC 429 option is not used, then pin 156 (429STRBI) MUST be grounded for the "bounce" circuit to operate properly.

**FIGURE 10. DD-03201 TO ARINC 429 INTERFACE**

† This signal is only significant for the ARINC 429 device option.





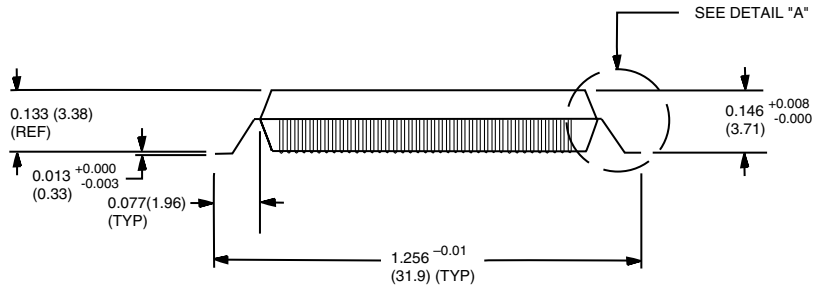
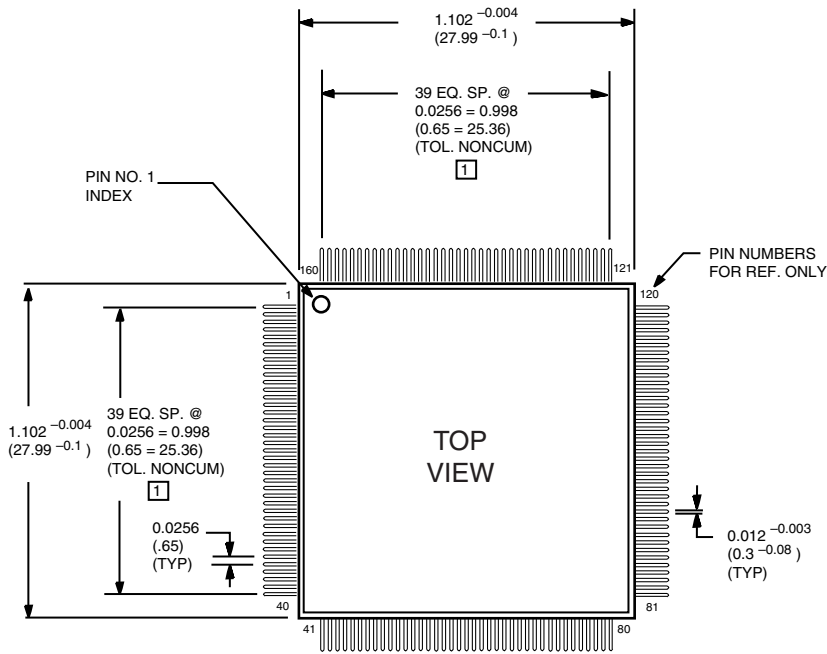
**TABLE 10. DD-03201 PIN FUNCTIONS**

| PIN NUMBER | FUNCTION           | PIN NUMBER | FUNCTION           | PIN NUMBER | FUNCTION           |
|------------|--------------------|------------|--------------------|------------|--------------------|
| 1          | SEL0               | 55         | CH44               | 109        | CH70               |
| 2          | SEL1               | 56         | CH45               | 110        | CH69               |
| 3          | SEL2               | 57         | CH46               | 111        | CH68               |
| 4          | CH1                | 58         | CH47               | 112        | CH67               |
| 5          | CH2                | 59         | CH48               | 113        | CH66               |
| 6          | CH3                | 60         | VddB (Note 4, 8)   | 114        | CH65               |
| 7          | CH4                | 61         | Vss2 (Note 6, 9)   | 115        | TEST C HI (Note 1) |
| 8          | CH5                | 62         | CH49               | 116        | REF C (Note 1)     |
| 9          | CH6                | 63         | CH50               | 117        | TEST C LO (Note 1) |
| 10         | CH7                | 64         | CH51               | 118        | Vdd (Note 5, 8)    |
| 11         | CH8                | 65         | CH52               | 119        | BITS 8/16*         |
| 12         | CH9                | 66         | CH53               | 120        | CH32/96*           |
| 13         | CH10               | 67         | CH54               | 121        | CLKB (1MHZ CLK)**  |
| 14         | CH11               | 68         | CH55               | 122        | Vss (Note 7, 9)    |
| 15         | CH12               | 69         | CH56               | 123        | B TIMER (Note 2)   |
| 16         | CH13               | 70         | CH57               | 124        | A TIMER (Note 2)   |
| 17         | CH14               | 71         | CH58               | 125        | D15                |
| 18         | CH15               | 72         | CH59               | 126        | D14                |
| 19         | CH16               | 73         | CH60               | 127        | D13                |
| 20         | VddA (Note 4, 8)   | 74         | CH61               | 128        | D12                |
| 21         | Vss1 (Note 6, 9)   | 75         | CH62               | 129        | D11                |
| 22         | CH17               | 76         | CH63               | 130        | D10                |
| 23         | CH18               | 77         | CH64               | 131        | D9                 |
| 24         | CH19               | 78         | TEST B HI (Note 1) | 132        | D8                 |
| 25         | CH20               | 79         | REF B (Note 1)     | 133        | D7                 |
| 26         | CH21               | 80         | TEST B LO (Note 1) | 134        | D6                 |
| 27         | CH22               | 81         | CH96               | 135        | D5                 |
| 28         | CH23               | 82         | CH95               | 136        | D4                 |
| 29         | CH24               | 83         | CH94               | 137        | D3                 |
| 30         | CH25               | 84         | CH93               | 138        | D2                 |
| 31         | CH26               | 85         | CH92               | 139        | D1                 |
| 32         | CH27               | 86         | CH91               | 140        | D0                 |
| 33         | CH28               | 87         | CH90               | 141        | VssDIG (Note 7, 9) |
| 34         | CH29               | 88         | CH89               | 142        | VddDIG (Note 5, 8) |
| 35         | CH30               | 89         | CH88               | 143        | ADDR5              |
| 36         | CH31               | 90         | CH87               | 144        | ADDR4              |
| 37         | CH32               | 91         | CH86               | 145        | ADDR3              |
| 38         | TEST A HI (Note 1) | 92         | CH85               | 146        | ADDR2              |
| 39         | REF A (Note 1)     | 93         | CH84               | 147        | ADDR1              |
| 40         | TEST A LO (Note 1) | 94         | CH83               | 148        | ADDR0              |
| 41         | TMODE*             | 95         | CH82               | 149        | ENABLE*            |
| 42         | TMUX*              | 96         | CH81               | 150        | READY              |
| 43         | RESET*             | 97         | VddC (Note 4, 8)   | 151        | FAULT*             |
| 44         | CH33               | 98         | Vss3 (Note 6, 9)   | 152        | FMUX*              |
| 45         | CH34               | 99         | CH80               | 153        | FMODE*             |
| 46         | CH35               | 100        | CH79               | 154        | ARINC LO           |
| 47         | CH36               | 101        | CH78               | 155        | ARINC HI           |
| 48         | CH37               | 102        | CH77               | 156        | 429STRBI           |
| 49         | CH38               | 103        | CH76               | 157        | 429STRBO           |
| 50         | CH39               | 104        | CH75               | 158        | 429MRATE           |
| 51         | CH40               | 105        | CH74               | 159        | 429DRATE           |
| 52         | CH41               | 106        | CH73               | 160        | CLKA (1MHZ CLK)**  |
| 53         | CH42               | 107        | CH72               |            |                    |
| 54         | CH43               | 108        | CH71               |            |                    |

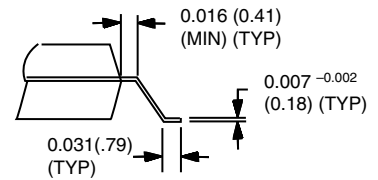
Notes:

1. Refer to Analog Inputs section and FIGURES 4, 5 and 6.
2. Refer to A Timer and B Timer section and FIGURE 7.
3. (\*) Indicates an active low signal.
4. Analog Vdd input.
5. Digital Vdd input.

6. Analog Gnd.
7. Digital Gnd.
8. Analog Vdd and Digital Vdd inputs must be tied to the same local supply potential.
9. Analog GND and Digital GND inputs must be tied to the same local ground potential.
10. (\*\*) Refer to CLKA and CLKB section and FIGURE 7.



**DETAIL "A"**  
NTS



- Notes:  
 1. LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN  $\pm 0.010$  ( $-0.25$ ).  
 2. DIMENSIONS IN INCHES (MILLIMETERS).

**FIGURE 11. DD-03201 MECHANICAL OUTLINE (PLASTIC PACKAGE)**

**ORDERING INFORMATION**

**DD-03201FP-200**

- ARINC Port Option:**  
0 = Without ARINC 429 Output  
4 = With ARINC 429 Output
- Screening:**  
0 = Standard DDC Procedures
- Temperature Range:**  
2 = -40°C to + 85°C
- ASIC Package Type:**  
P = Plastic
- Package Style:**  
F = Surface Mount

These products contain tin-lead solder finish as applicable to solder dip requirements.

**OTHER APPLICABLE DOCUMENTS**

RTCA/DO-160C: Environmental Conditions and Test Procedures for Airborne Equipment.

| STANDARD DDC PROCESSING<br>FOR PLASTIC MONOLITHIC PRODUCTS |                |              |
|--|----------------|--------------|
| TEST   | MIL-STD-883    |              |
|  | METHOD(S)      | CONDITION(S) |
| INSPECTION / WORKMANSHIP                                   | 2017, and 2032 | —            |
| ELECTRICAL TEST  | DDC ATP        | —            |

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