Triple Port ATM PHY for 25.6 and 51.2 Mbps with 8-bit Utopia 2

PRELIMINARY
IDT77V1053

Features

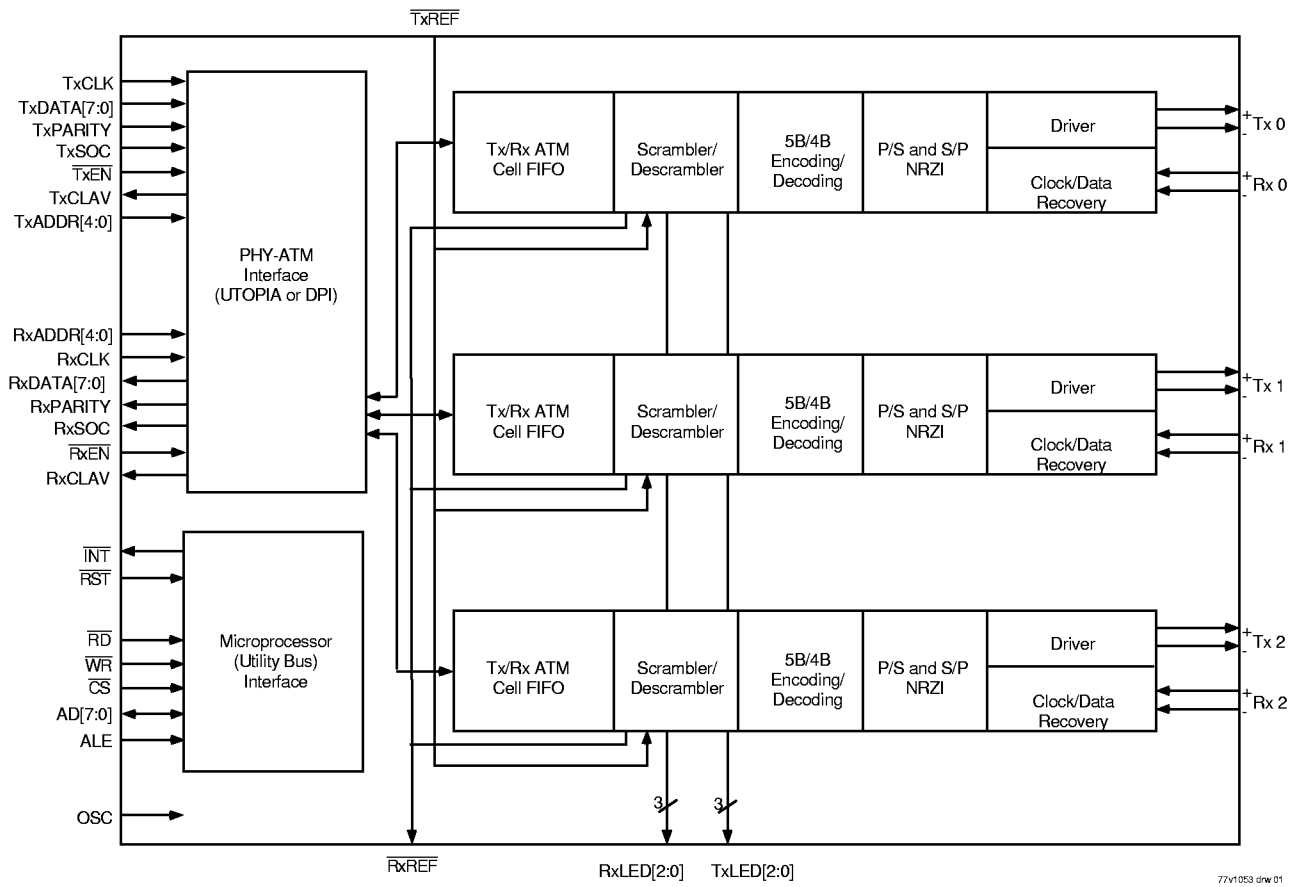
- Performs the PHY-Transmission Convergence (TC) and Physical Media Dependent (PMD) Sublayer functions for three 25.6 Mbps ATM channels
- Compliant to ATM Forum (af-phy-040.000) and ITU-T I.432.5 specifications for 25.6 Mbps physical interface
- Also operates at 51.2Mbps
- 8-bit UTOPIA Level 2 Interface
- 3-Cell Transmit & Receive FIFOs
- LED Interface for status signalling
- Supports UTP Category 3 physical media
- Interfaces to standard magnetics
- Low-Power CMOS
- 3.3V supply with 5V tolerant inputs
- 128-pin TQFP Package (14 x 20 mm)

Description

The IDT77V1053 is a member of IDT's family of products supporting Asynchronous Transfer Mode (ATM) data communications and networking. The IDT77V1053 implements the physical layer for 25.6 Mbps ATM, connecting three serial copper links (UTP Category 3) to one ATM layer device such as a SAR or a switch ASIC. The IDT77V1053 also operates at 51.2 Mbps, and is well suited to backplane driving applications. The 77V1053 utilizes an 8-bit UTOPIA Level 2 interface on the cell side.

The IDT77V1053 is fabricated using IDT's state-of-the-art CMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

Functional Block Diagram



SEPTEMBER 1999

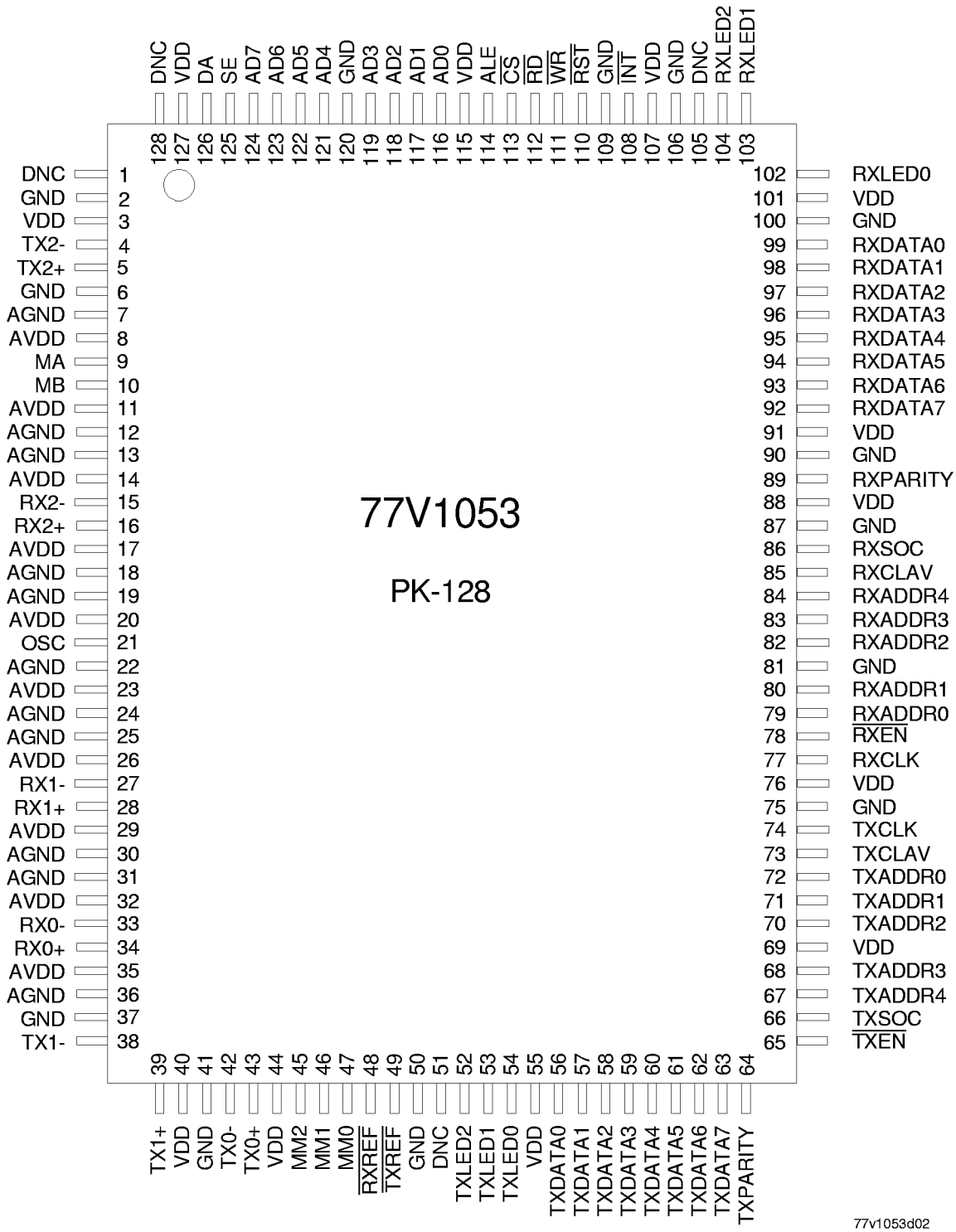


Figure 1. Pin Assignments

Table 1. Signal Descriptions

LINE SIDE SIGNALS

SIGNAL NAME	PIN NUMBER	I/O	SIGNAL DESCRIPTION
RX0+,-	34, 33	In	Port 0 positive and negative receive differential input pair.
RX1+,-	28, 27	In	Port 1 positive and negative receive differential input pair.
RX2+,-	16, 15	In	Port 2 positive and negative receive differential input pair.
TX0+,-	43, 42	Out	Port 0 positive and negative transmit differential output pair.
TX1+,-	39, 38	Out	Port 1 positive and negative transmit differential output pair.
TX2+,-	5, 4	Out	Port 2 positive and negative transmit differential output pair.

UTILITY BUS SIGNALS

SIGNAL NAME	PIN NUMBER	I/O	SIGNAL DESCRIPTION
AD[7:0]	124, 123, 122, 121, 119, 118, 117, 116	In/Out	Utility bus address/data bus. The address input is sampled on the falling edge of ALE. Data is output on this bus when a read is performed. Input data is sampled at the completion of a write operation.
ALE	114	In	Utility bus address latch enable. Asynchronous input. An address on the AD bus is sampled on the falling edge of ALE. ALE must be low when the AD bus is being used for data.
$\overline{CS}$	113	In	Utility bus asynchronous chip select. $\overline{CS}$ must be asserted to read or write an internal register. It may remain asserted at all times if desired.
$\overline{RD}$	112	In	Utility bus read enable. Active low asynchronous input. After latching an address, a read is performed by deasserting $\overline{WR}$ and asserting $\overline{RD}$ and $\overline{CS}$.
$\overline{WR}$	111	In	Utility bus write enable. Active low asynchronous input. After latching an address, a write is performed by deasserting $\overline{RD}$, placing data on the AD bus, and asserting $\overline{WR}$ and $\overline{CS}$. Data is sampled when $\overline{WR}$ or $\overline{CS}$ is deasserted.

MISCELLANEOUS SIGNALS

SIGNAL NAME	PIN NUMBER	I/O	SIGNAL DESCRIPTION
DA	126	In	Reserved signal. This input must be connected to logic low.
DNC	1, 51, 105, 128	Out	Do Not Connect. Do not connect these pins to anything external to the chip. They must remain open.
$\overline{INT}$	108	Out	Interrupt. $\overline{INT}$ is an open-drain output, driven low to indicate an interrupt. Once low, $\overline{INT}$ remains low until the interrupt status in the appropriate interrupt Status Register is read. Interrupt sources are programmable via the interrupt Mask Registers.
MA	9	In	Reserved signal. This input should be connected to logic low.
MB	10	In	Reserved signal. This input should be connected to logic high.
MM0	47	In	Reserved signal. This input must be connected to logic high.
MM1	46	In	Reserved signal. This input must be connected to logic low.
MM2	45	In	Reserved signal. This input must be connected to logic high.
OSC	21	In	TTL line rate clock source, driven by a 100 ppm oscillator. 32 MHz for 25.6 Mbps; 64 MHz for 51.2 Mbps.
$\overline{RST}$	110	In	Reset. Active low asynchronous input resets all control logic, counters and FIFOs. A reset must be performed after power up prior to normal operation of the part.
RXLED[2:0]	104, 103, 102	Out	Receive LED drivers. Driven low for 2^{23} cycles of OSC, beginning with RXSOC when that port receives a good (non-null and non-errored) cell. Drives 8 mA both high and low. One per port.
$\overline{RXREF}$	48	Out	Receive Reference. Active low, synchronous to OSC. $\overline{RXREF}$ pulses low for a programmable number of clock cycles when an x_8 command byte is received. Register 0x40 is programmed to indicate which port is referenced.

77v1053 tbl 01

Table 1. Signal Descriptions (con't.)

SIGNAL NAME	PIN NUMBER	I/O	SIGNAL DESCRIPTION
SE	125	In	Reserved signal. This input must be connected to logic low.
TXLED[2:0]	52, 53, 54	Out	Ports 2 thru 0 Transmit LED driver. Goes low for 2^{23} cycles of OSC, beginning with TXSOC when this port receives a cell for transmission. 8 mA drive current both high and low. One per port.
$\overline{\text{TXREF}}$	49	In	Transmit Reference. Synchronous to OSC. At the falling edge of $\overline{\text{TXREF}}$, an X_8 command byte is inserted into the transmit data stream. Logic for this signal is programmed in register 0x40. Typical application is WAN timing.

POWER SUPPLY SIGNALS

SIGNAL NAME	PIN NUMBER	I/O	SIGNAL DESCRIPTION
AGND	7, 12, 13, 18, 19, 22, 24, 25, 30, 31, 36	—	Analog ground. AGND supply a ground reference to the analog portion of the ship, which sources a more constant current than the digital portion.
AV_{DD}	8, 11, 14, 17, 20, 23, 26, 29, 32, 35	—	Analog power supply 3.3 ± 0.3V AVDD supply power to the analog portion of the chip, which draws a more constant current than the digital portion.
GND	2, 6, 37, 41, 50, 75, 81, 87, 90, 100, 106, 109, 120	—	Digital Ground.
V_{DD}	3, 40, 44, 55, 69, 76, 88, 91, 101, 107, 115, 127	—	Digital power supply. 3.3 ± 0.3V.

8-BIT UTOPIA 2 SIGNALS

SIGNAL NAME	PIN NUMBER	I/O	SIGNAL DESCRIPTION
RXADDR[4:0]	84, 83, 82, 80, 79	In	Utopia 2 Receive Address Bus. This bus is used in polling and selecting the receive port. The port addresses are defined in bits [4:0] of the Enhanced Control Registers.
RXCLAV	85	Out	Utopia 2 Receive Cell Available. Indicates the cell available status of the addressed port. It is asserted when a full cell is available for retrieval from the receive FIFO. When non of the four ports is addressed. RXCLAV is high impedance.
RXCLK	77	In	Utopia 2 Receive Clock. This is a free running clock input.
RXDATA[7:0]	92, 93, 94, 95, 96, 97, 98, 99	Out	Utopia 2 Receive Data. When one of the four ports is selected, the 77V1053 transfers received cells to an ATM device across this bus. Also see RXPARITY.
$\overline{\text{RXEN}}$	78	In	Utopia 2 Receive Enable. Driven by an ATM device to indicate its ability to receive data across the RXDATA bus.
RXPARITY	89	Out	Utopia 2 Receive Data Parity. Odd parity over RXDATA[7:0].
RXSOC	86	Out	Utopia 2 Receive Start of Cell. Asserted coincident with the first word of data for each cell on RXDATA.
TXADDR[4:0]	67, 68, 70, 71, 72	In	Utopia 2 Transmit Address Bus. This bus is used in polling and selecting the transmit port. The port addresses are defined in bits [4:0] of the Enhanced Control Registers.
TXCLAV	73	Out	Utopia 2 Transmit Cell Available. Indicates the availability of room in the transmit FIFO of the addressed port for a full cell. When none of the four ports is addressed, TXCLAV is high impedance.
TXCLK	74	In	Utopia Transmit Clock. This is a free running clock input.

77v1053 tbl 02

Table 1. Signal Descriptions (con't.)

SIGNAL NAME	PIN NUMBER	I/O	SIGNAL DESCRIPTION
TXDATA[7:0]	63, 62, 61, 60, 59, 58, 57, 56	In	Utopia 2 Transmit Data. An ATM device transfers cells across this bus to the 77V1053 for transmission. Also see TXPARITY.
$\overline{\text{TXEN}}$	65	In	Utopia 2 Transmit Enable. Driven by an ATM device to indicate it is transmitting data across the TXDATA bus.
TXPARITY	64	In	Utopia 2 Transmit Data Parity. Odd parity across TXDATA[7:0]. Parity is checked and errors are indicated in the Interrupt Status Registers, as enabled in the Master Control Registers. No other action is taken in the event of an error. Tie high or low if unused.
TXSOC	66	In	Utopia 2 Transmit Start of Cell. Asserted coincident with the first word of data for each cell on TXDATA.

77v1053 tbl 03

77V1053 Overview

The 77V1053 is a three-port implementation of the physical layer standard for 25.6Mbps ATM network communications as defined by ATM Forum document af-phy-040.000 and ITU-T I.432.5. The physical layer is divided into a Physical Media Dependent sub layer (PMD) and Transmission Convergence (TC) sub layer. The PMD sub layer includes the functions for the transmitter, receiver and clock recovery for operation across 100 meters of category 3 unshielded twisted pair (UTP) cable. This is referred to as the Line Side Interface. The TC sub layer defines the line coding, scrambling, data framing and synchronization.

On the cell side, the 77V1053 connects to an ATM layer device (such as a switch core or SAR) through an 8-bit Utopia Level 2 interface.

The 77V1053 is based on the 77105, and maintains significant register compatibility with it. The 77V1053, however, has additional register features, and also duplicates most of its registers to provide significant independence between the three ports.

Access to these status and control registers is through the utility bus. This is an 8-bit muxed address and data bus, controlled by a conventional asynchronous read/write handshake.

Additional pins permit insertion and extraction of an 8kHz timing marker, and provide LED indication of receive and transmit status.

OPERATION AT 51.2 Mbps

In addition to operation at the standard rate of 25.6 Mbps, the 77V1053 is also specified to operate at 51.2 Mbps. Except for the doubled bit rate, all other aspects of operation are identical to the 25.6 Mbps mode.

The rate is determined by the frequency of the clock applied to the OSC input pin. OSC is 32 MHz for the 25.6 Mbps line rate, and 64 MHz for the 51.2 Mbps line rate. All ports operate at the same frequency.

See page 17 for recommended line magnetics. Magnetics for 51.2 Mbps operation have a higher bandwidth than magnetics optimized for 25.6 Mbps.

Functional Description

TRANSMISSION CONVERGENCE (TC) SUB LAYER

Introduction

The TC sub layer defines the line coding, scrambling, data framing and synchronization. Under control of a switch interface or Segmentation and Reassembly (SAR) unit, the 25.6Mbps ATM PHY accepts a 53-byte ATM cell, scrambles the data, appends a command byte to the beginning of the cell, and encodes the entire 53 bytes before transmission. These data transformations ensure that the signal is evenly distributed across the frequency spectrum. In addition, the serialized bit stream is NRZI coded. An 8kHz timing sync pulse may be used for isochronous communications.

Data Structure and Framing

Each 53-byte ATM cell is preceded with a command byte. This byte is distinguished by an escape symbol followed by one of 17 encoded symbols. Together, this byte forms one of seventeen possible command bytes. Three command bytes are defined:

1. **X_X** (read: 'escape' symbol followed by another 'escape'): Start-of-cell with scrambler/descrambler reset.
2. **X_4** ('escape' followed by '4'): Start-of-cell without scrambler/descrambler reset.
3. **X_8** ('escape' followed by '8'): 8kHz timing marker. This command byte is generated when the 8kHz sync pulse is detected, and has priority over all line activity (data or command bytes). It is transmitted immediately when the sync pulse is detected. When this occurs during a cell transmission, the data transfer is temporarily interrupted on an octet boundary, and the X_8 command byte is inserted. This condition is the only allowed interrupt in an otherwise contiguous transfer.

Below is an illustration of the cell structure and command byte usage:

{X_X} {53-byte ATM cell} {X_4} {53-byte ATM {X_8} cell} ...

In the above example, the first ATM cell is preceded by the X_X start-of-cell command byte which resets both the transmitter-scrambler and receiver-descrambler pseudo-random nibble generators (PRNG) to their initial states. The following cell illustrates the insertion of a start-of-cell command without scrambler/descrambler reset. During this cell's transmission, an 8kHz timing sync pulse triggers insertion of the X_8 8kHz timing marker command byte.

Functional Block Diagram (con't.)

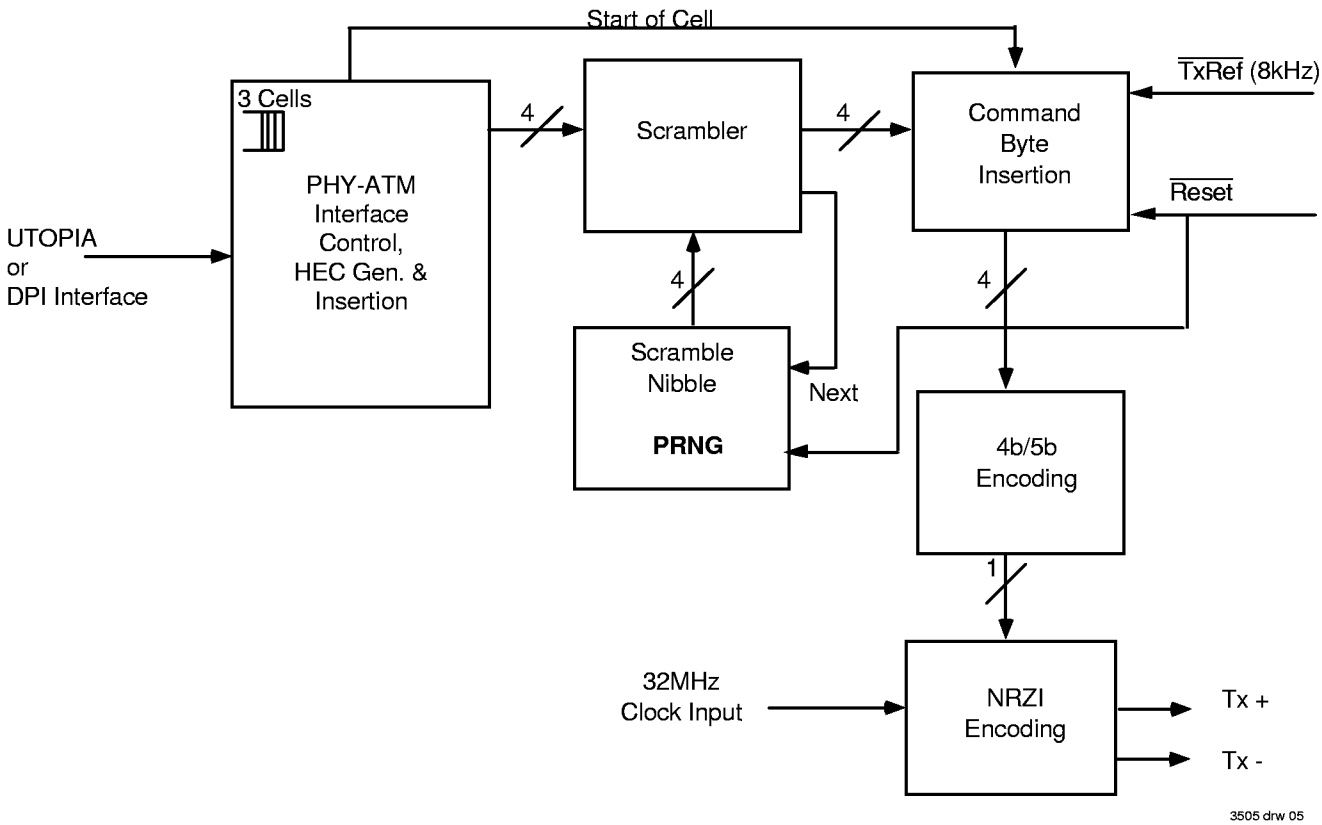


Figure 2. TC Transmit Block Diagram

Transmission Description

Refer to the TC Transmit Block Diagram on the previous page. Cell transmission begins with the PHY-ATM Interface. An ATM layer device transfers a cell into the 77V1053 across the Utopia transmit bus. This cell enters a 3-cell deep transmit FIFO. Once a complete cell is in the FIFO, transmission begins by passing the cell, four bits (MSB first) at a time to the 'Scrambler'.

The 'Scrambler' takes each nibble of data and exclusive-ORs them against the 4 high order bits (X(t), X(t-1), X(t-2), X(t-3)) of a 10 bit pseudo-random nibble generator (PRNG). Its function is to provide the appropriate frequency distribution for the signal across the line.

The PRNG is clocked every time a nibble is processed, regardless of whether the processed nibble is part of a data or command byte. Note however that only data nibbles are scrambled. The entire command byte (X _C) is NOT scrambled before it's encoded (see diagram for illustration). The PRNG is based upon the following polynomial:

$$X^{10} + X^7 + 1$$

With this polynomial, the four output data bits (D3, D2, D1, D0) will be generated from the following equations:

D3 = d3 xor X(t-3)
D2 = d2 xor X(t-2)
D1 = d1 xor X(t-1)
D0 = d0 xor X(t)

The following nibble is scrambled with X(t+4), X(t+3), X(t+2), and X(t+1).

A scrambler lock between the transmitter and receiver occurs each time an X_X command is sent. An X_X command is initiated only at the beginning of a cell transfer after the PRNG has cycled through all of its states (2^{10} - 1 = 1023 states). The first valid ATM data cell transmitted after power on will also be accompanied with an X_X command byte. Each time an X_X command byte is sent, the first nibble after the last escape (X) nibble is XOR'd with 1111b (PRNG = 3FFx).

Because a timing marker command (X_8) may occur at any time, the possibility of a reset PRNG start-of-cell command and a timing marker command occurring consecutively does exist (e.g. X_X_X_8). In this case, the detection of the last two consecutive escape (X) nibbles will cause the PRNG to reset to its initial 3FFx state. Therefore, the PRNG is clocked only after the first nibble of the second consecutive escape pair.

Once the data nibbles have been scrambled using the PRNG, the nibbles are further encoded using a 4b/5b process. The 4b/5b scheme ensures that an appropriate number of signal transitions occur on the line. A total of seventeen 5-bit symbols are used to represent the sixteen 4-bit data nibbles and the one escape (X) nibble. The table below lists the 4-bit data with their corresponding 5-bit symbols:

Data	Symbol
0000	10101
0100	00111
1000	10010
1100	10111

Data	Symbol
0001	01001
0101	01101
1001	11001
1101	11101

Data	Symbol
0010	01010
0110	01110
1010	11010
1110	11110

Data	Symbol
0011	01011
0111	01111
1011	11011
1111	11111

ESC(X) = 00010

3505 drw 05a

This encode/decode implementation has several very desirable properties. Among them is the fact that the output data bits can be represented by a set of relatively simple symbols;

- Run length is limited to <= 5;
- Disparity never exceeds +/- 1.

On the receiver, the decoder determines from the received symbols whether a timing marker command (X_8) or a start-of-cell command was sent (X_X or X_4). If a start-of-cell command is detected, the next 53 bytes received are decoded and forwarded to the descrambler. (See TC Receive Block Diagram, Figure 3).

The output of the 4b/5b encoder provides serial data to the NRZI encoder. The NRZI code transitions the wire voltage each time a '1' bit is sent. This, together with the previous encoding schemes guarantees that long run lengths of either '0' or '1's are prevented. Each symbol is shifted out with its most significant bit sent first.

When no cells are available to transmit, the 77V1053 keeps the line active by continuing to transmit valid symbols. But it does not transmit another start-of-cell command until it has another cell for transmission. The 77V1053 never generates idle cells.

Transmit HEC Byte Calculation/Insertion

Byte #5 of each ATM cell, the HEC (Header Error Control) is calculated automatically across the first 4 bytes of the cell header, depending upon the setting of bit 5 of registers 0x03, 0x13 and 0x23. This byte is then either inserted as a replacement of the fifth byte transferred to the PHY by the external system, or the cell is transmitted as received. A third operating mode provides for insertion of "Bad" HEC codes which may aid in communication diagnostics. These modes are controlled by the LED Driver and HEC Status/Control Registers.

Receiver Description

The receiver side of the TC sublayer operates like the transmitter, but in reverse. The data is NRZI decoded before each symbol is reassembled. The symbols are then sent to the 5b/4b decoder, followed by the Command Byte Interpreter, De-Scrambler, and finally through a FIFO to the UTOPIA interface to an ATM Layer device.

ATM CELL FORMAT

Bit 7	Bit 0
Header Byte 1	
Header Byte 2	
Header Byte 3	
Header Byte 4	
UDF	
Payload Byte 1	
⋮	
Payload Byte 48	

3505 drw 52

UDF = User Defined Field (or HEC)

Note that although the IDT77V1053 can detect symbol and HEC errors, it does not attempt to correct them.

Upon reset or the re-connect, each port's receiver is typically not symbol-synchronized. When not symbol-synchronized, the receiver will indicate a significant number of bad symbols, and will deassert the Good Signal Bit as described below. Synchronization is established immediately once that port receives an Escape symbol, usually as part of the start-of-cell command byte preceding the first received cell.

The IDT77V1053 monitors line conditions and can provide an interrupt if the line is deemed 'bad'. The Interrupt Status Registers (registers 0x01, 0x11 and 0x21) contain a Good Signal Bit (bit 6, set to 0 = Bad signal initially) which shows the status of the line per the following algorithm:

To declare 'Good Signal' (from "Bad" to "Good"):

There is an up-down counter that counts from 7 to 0 and is initially set to 7. When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and no "bad symbol" has been received, the counter decreases by one. However, if at least one "bad symbol" is detected during these 1,024 clocks, the counter is increased by one, to a maximum of 7. The Good Signal Bit is set to 1 when this counter reaches 0. The Good Signal Bit could be set to 1 as quickly as 1,433 symbols (204.8 x 7) if no bad symbols have been received.

Functional Block Diagram (con't.)

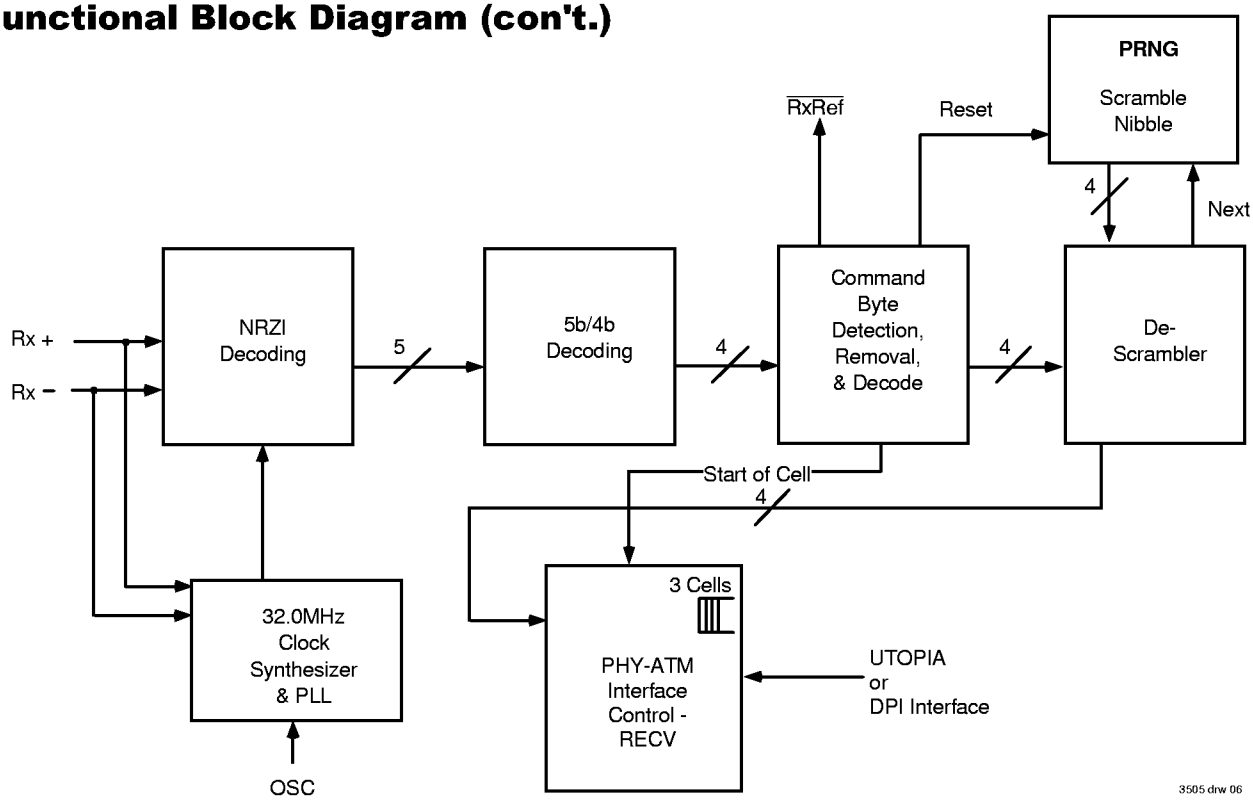


Figure 3. TC Receive Block Diagram

To declare 'Bad Signal' (from "Good" to "Bad"):

The same up-down counter counts from 0 to 7 (being at 0 to provide a "Good" status). When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and there is at least one "bad symbol", the counter increases by one. If it detects all "good symbols" and no "bad symbols" in the next time period, the counter decreases by one. The "Bad Signal" is declared when the counter reaches 7. The Good Signal Bit could be set to 0 as quickly as 1,433 symbols (204.8 x 7) if at least one "bad symbol" is detected in each of seven consecutive groups of 204.8 symbols.

8kHz Timing Marker

The 8kHz timing marker, described earlier, is a completely optional feature which is essential for some applications requiring synchronization for voice or video, and unnecessary for other applications. The figure below shows the options available for generating and receiving the 8kHz timing marker.

The source of the marker is programmable in the $\overline{\text{RXREF}}$ and $\overline{\text{TXREF}}$ Control Register (0x40). Each port is individually programmable to either a local source or a looped remote source. The local source is $\overline{\text{TXREF}}$, which is an 8kHz clock of virtually any duty cycle. When unused, $\overline{\text{TXREF}}$ should be tied high. Also note that it is not limited to 8kHz, should a different frequency be desired. When looped, a received X_8 command byte causes one to be generated on the transmit side.

A received X_8 command byte causes the 77V1053 to issue a negative pulse on $\overline{\text{RXREF}}$. The source channel of the marker is programmable.

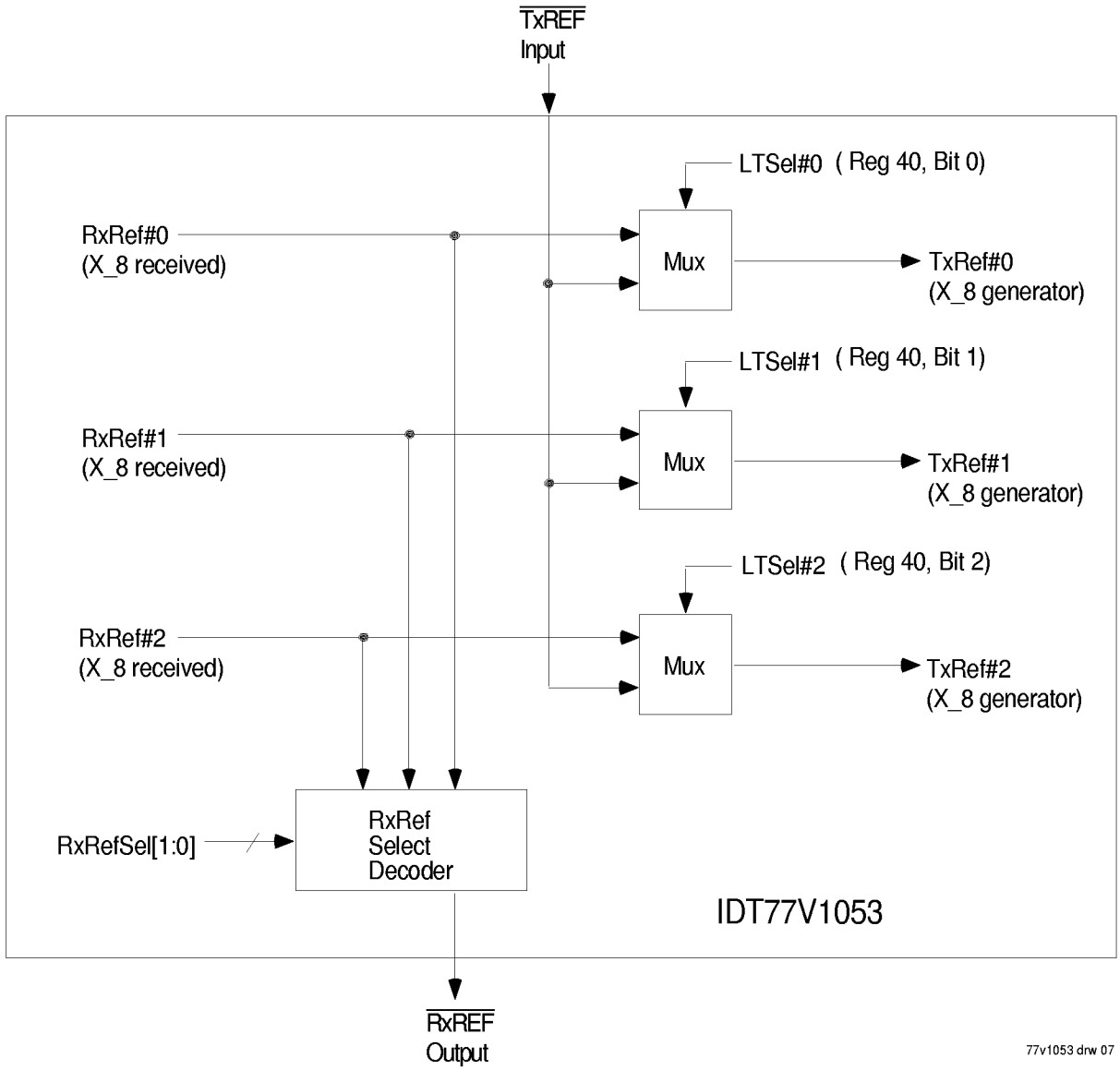


Figure 4. $\overline{\text{RXREF}}$ and $\overline{\text{TXREF}}$ Block Diagram

PHY-ATM INTERFACE

UTOPIA is a Physical Layer to ATM Layer interface standardized by the ATM Forum. It transfers ATM cells and has separate transmit and receive channels and specific handshaking protocols. UTOPIA Level 2 has dedicated address signals for both the transmit and receive directions that allow the ATM layer device to specify with which of the four PHY channels it is communicating. It is defined in ATM Forum document af-phy-0039.

Note that the 77V1053 supports only the "Operation with 1 TxClav and 1 Rx Clav" multi-phy scheme. The optional Direct Status Indication and Multiplexed Status Polling multi-phy schemes are not directly supported.

There is a single 8-bit data bus in the transmit (ATM-to-PHY) direction, and a single 8-bit data bus in the receive (PHY-to-ATM) direction. In addition to the data bus, each direction also includes a single optional parity bit, an address bus, and several handshaking signals. The UTOPIA address of each channel is determined by bits 4 to 0 in the Enhanced Control Registers. Please note that the transmit bus and the receive bus operate completely independently. The Utopia signals are summarized below:

TXDATA[7:0]	ATM to PHY
TXPARITY	ATM to PHY
TXSOC	ATM to PHY
TXADDR[4:0]	ATM to PHY
$\overline{\text{TXEN}}$	ATM to PHY
TXCLAV	PHY to ATM
TXCLK	ATM to PHY
RXDATA[7:0]	PHY to ATM
RXPARITY	PHY to ATM
RXSOC	PHY to ATM
RXADDR[4:0]	ATM to PHY
$\overline{\text{RXEN}}$	ATM to PHY
RXCLAV	PHY to ATM
RXCLK	ATM to PHY

The ATM device starts by polling the PHY ports on the Utopia bus to determine if any of them has room to accept a cell for transmission (TXCLAV), or has a receive cell available to pass on to the ATM device (RXCLAV). To poll, the ATM device drives an address (TXADDR or RXADDR) then observes TXCLAV or RXCLAV on the next cycle of TXCLK or RXCLK. A port must tri-state TXCLAV and RXCLAV except when it is addressed.

If TXCLAV or RXCLAV is asserted, the ATM device may select that port, then transfer a cell to or from it. Selection of a port is performed by driving the address of the desired port while $\overline{\text{TXEN}}$ or $\overline{\text{RXEN}}$ is high, then driving $\overline{\text{TXEN}}$ or $\overline{\text{RXEN}}$ low. When $\overline{\text{TXEN}}$ is driven low, TXSOC (start of cell) is driven high to indicate that the first byte of the cell are being driven on TXDATA. The ATM device may chose to temporarily suspend transfer of the cell by deasserting $\overline{\text{TXEN}}$. Otherwise, $\overline{\text{TXEN}}$ remains asserted as the next byte is driven onto TXDATA with each cycle of TXCLK.

In the receive direction, the ATM device selects a port if it wished to receive the cell that the port is holding. It does this by asserting $\overline{\text{RXEN}}$. The PHY then transfers the data 8 bits each clock cycle, as determined by $\overline{\text{RXEN}}$. As in the transmit direction, the ATM device may suspend transfer by deasserting $\overline{\text{RXEN}}$ at any time. Note that the PHY asserts RXSOC coincident with the first byte of each cell.

TXPARITY and RXPARITY are parity bits for the corresponding 8-bit data fields. Odd parity is used.

The following figures may be referenced for Utopia Level 2 bus examples.

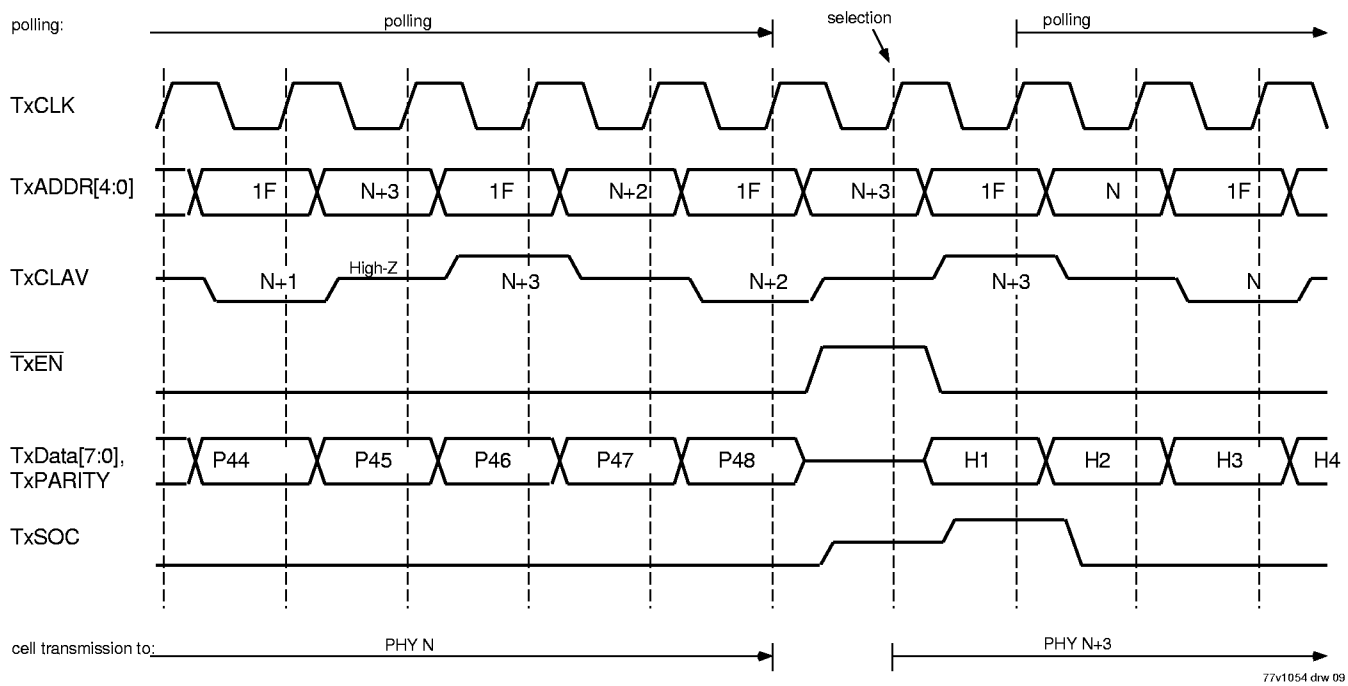


Figure 5. Utopia 2 Transmit Handshake - Back to Back Cells

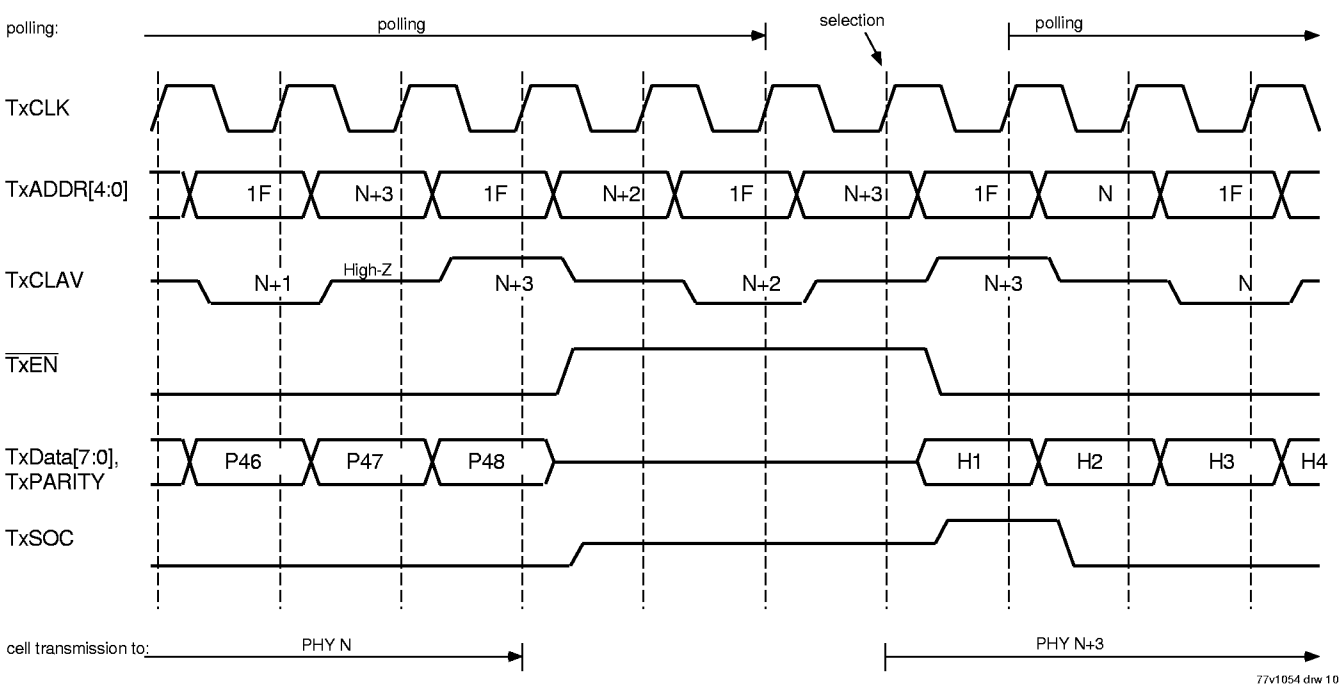


Figure 6. Utopia 2 Transmit Handshake - Delay Between Cells

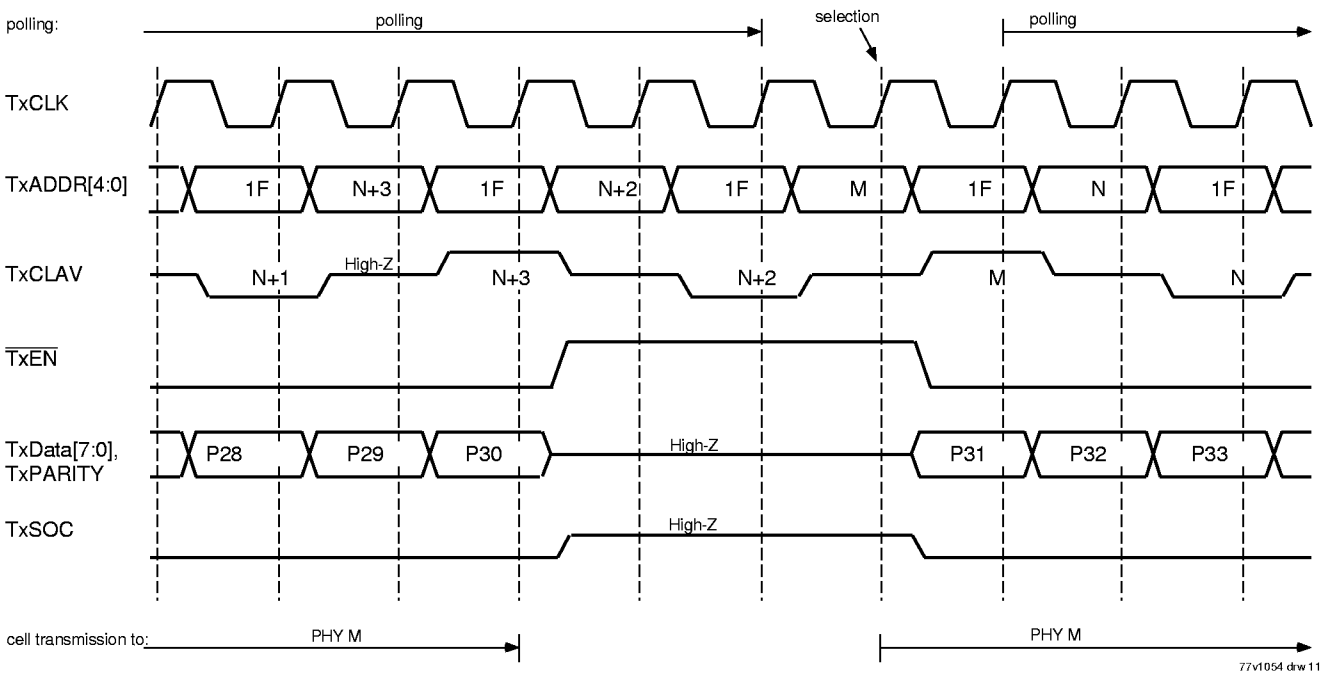


Figure 7. Utopia 2 Transmit Handshake - Transmission Suspended

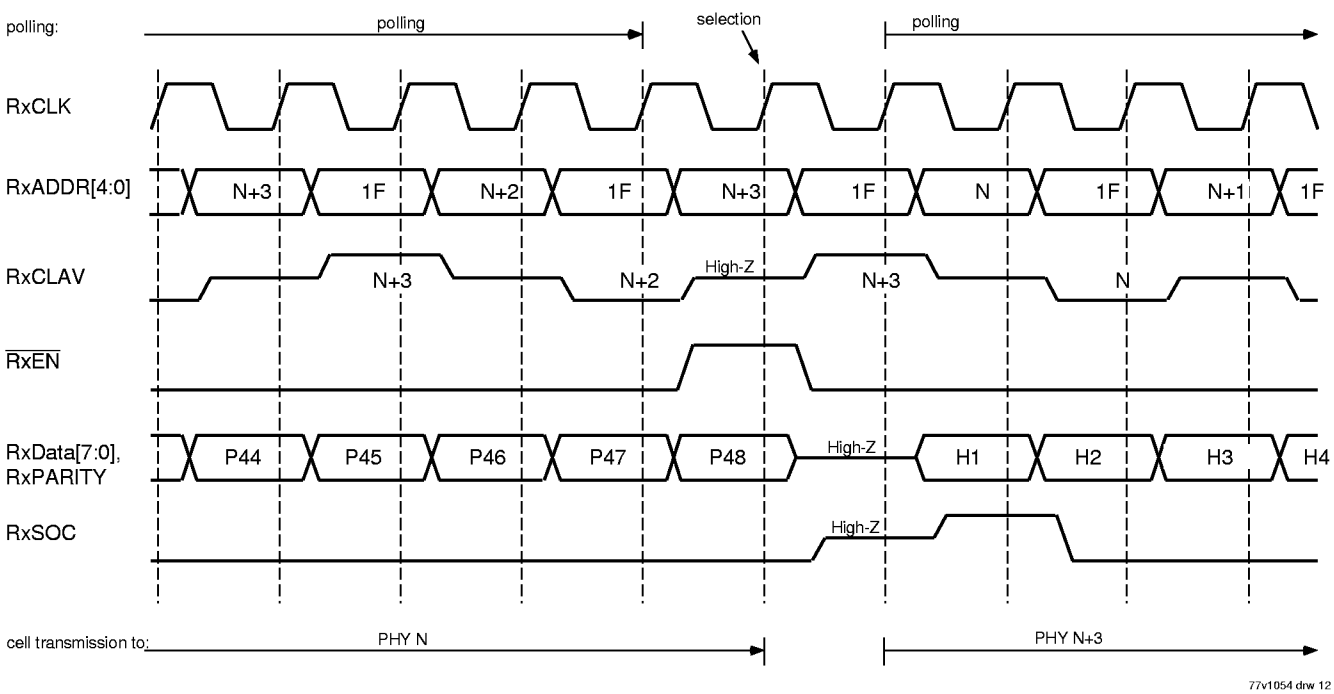


Figure 8. Utopia 2 Receive Handshake - Back to Back Cells

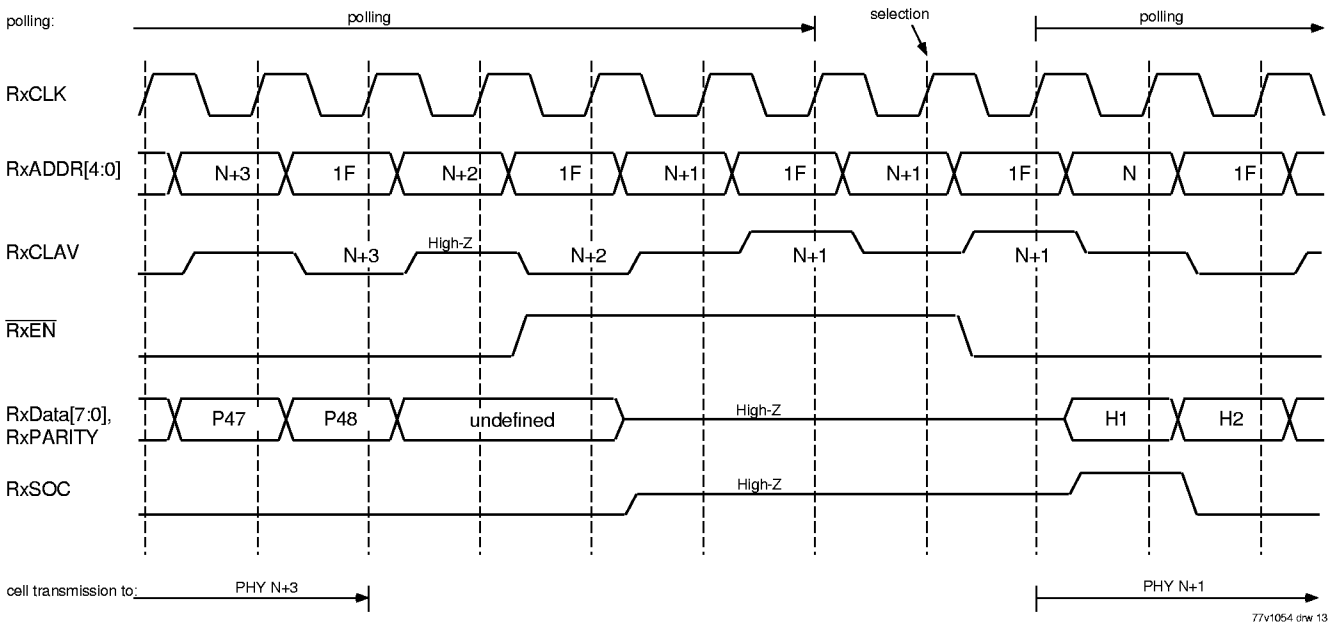


Figure 9. Utopia 2 Receive Handshake - Delay Between Cells

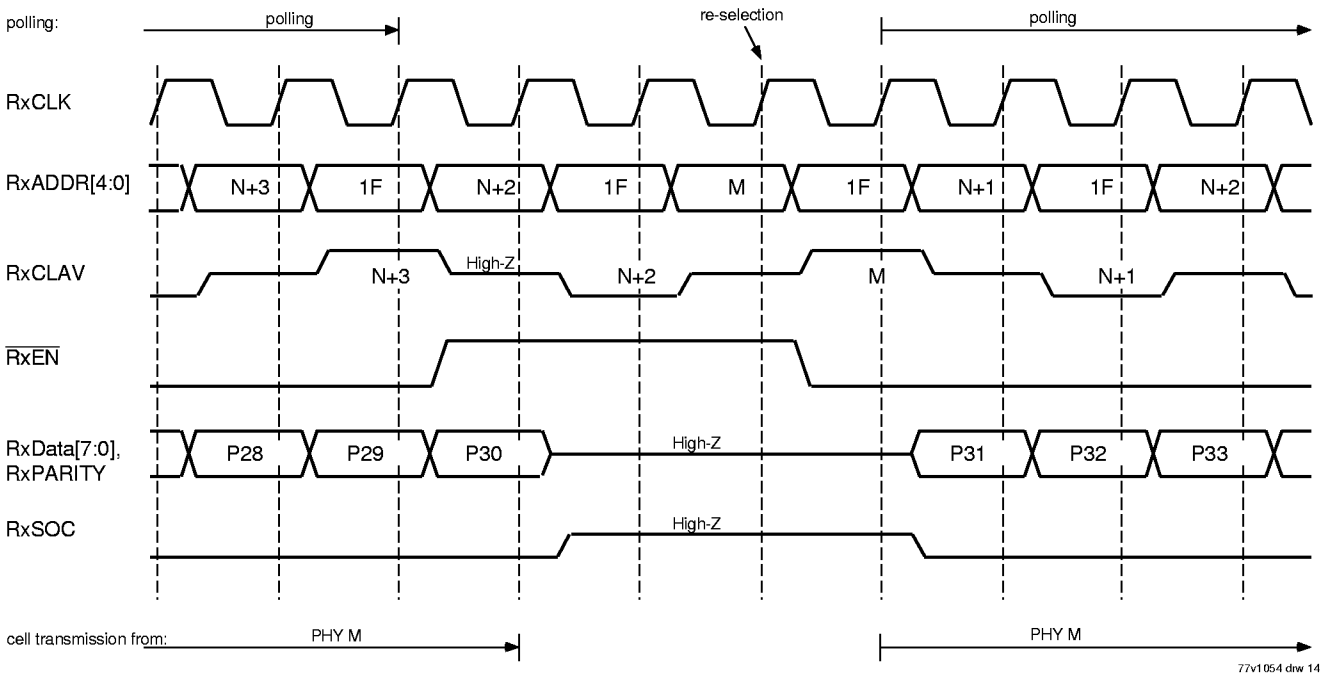


Figure 10. Utopia 2 Receive Handshake - Suspended Transfer of Data

Control and Status Interface

UTILITY BUS

The Utility Bus is a byte-wide interface that provides access to the registers within the IDT77V1053. These registers are used to select desired operating characteristics and functions, and to communicate status to external systems.

The Utility Bus is implemented using a multiplexed address and data bus (AD[7:0]) where the register address is latched via the Address Latch Enable (ALE) signal.

The Utility Bus interface is comprised of the following pins:

AD[7:0], ALE, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$

Read Operation

Refer to the Utility Bus timing waveforms in Figures 18 - 19. A register read is performed as follows:

1. Initial condition:
   - $\overline{RD}$, $\overline{WR}$, $\overline{CS}$ not asserted (logic 1)
   - ALE not asserted (logic 0)
2. Set up register address:
   - place desired register address on AD[7:0]
   - set ALE to logic 1;
   - latch this address by setting ALE to logic 0.
3. Read register data:
   - Remove register address data from AD[7:0]
   - assert $\overline{CS}$ by setting to logic 0;
   - assert $\overline{RD}$ by setting to logic 0
   - wait minimum pulse width time (see AC specifications)

Write Operation

A register write is performed as described below:

1. Initial condition:
   - $\overline{RD}$, $\overline{WR}$, $\overline{CS}$ not asserted (logic 1)
   - ALE not asserted (logic 0)
2. Set up register address:
   - place desired register address on AD[7:0]
   - set ALE to logic 1;
   - latch this address by setting ALE to logic 0.
3. Write data:
   - place data on AD[7:0]
   - assert $\overline{CS}$ by setting to logic 0;
   - assert $\overline{WR}$ (logic 0) for minimum time (according to timing specification); reset $\overline{WR}$ to logic 1 to complete register write cycle.

INTERRUPT OPERATIONS

The IDT77V1053 provides a variety of selectable interrupt and signalling conditions which are useful both during 'normal' operation, and as diagnostic aids. Refer to the Status and Control Register List section.

Overall interrupt control is provided via bit 0 of the Master Control Registers. When this bit is cleared (set to 0), interrupt signalling is prevented on the respective port. The Interrupt Mask Registers allow individual masking of different interrupt sources. Additional interrupt signal control is provided by bit 5 of the Master Control Registers. When this bit is set (=1), receive cell errors will be flagged via interrupt signalling and all other interrupt conditions are masked. These errors include:

- Bad receive HEC
- Short (fewer than 53 bytes) cells
- Received cell symbol error

Normal interrupt operations are performed by setting bit 0 and clearing bit 5 in the Master Control Registers. $\overline{INT}$ (pin 108) will go to a low state when an interrupt condition is detected. The external system should then interrogate the 77V1053 to determine which one (or more) conditions caused this flag, and reset the interrupt for further occurrences. This is accomplished by reading the Interrupt Status Registers. Decoding the bits in these bytes will tell which error condition caused the interrupt. Reading these registers also:

- clears the (sticky) interrupt status bits in the registers that are read
- resets $\overline{INT}$

This leaves the interrupt system ready to signal an alarm for further problems.

LED CONTROL AND SIGNALLING

The LED outputs provide bi-directional LED drive capability of 8 mA. As an example, the RxLED outputs are described in the truth table:

STATE	PIN VOLTAGE
Cells being received	Low
Cells not being received	High

3505 tbl 10

As illustrated in the following drawing, this could be connected to provide for a two-LED condition indicator. These could also be different colors to provide simple status indication at a glance. (The minimum value for R should be 330Ω).

TxLED Truth Table

STATE	PIN VOLTAGE
Cells being transmitted	Low
Cells not being transmitted	High

3505 tbl 11

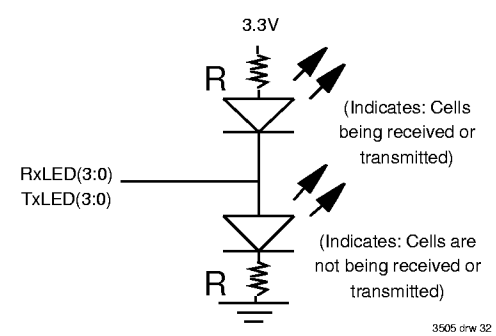


Figure 11.

DIAGNOSTIC FUNCTIONS

1. LOOPBACK

There are two loopback modes supported by the 77V1053. The loopback mode is controlled via bits 1 and 0 of the Diagnostic Control Registers:

Bit 1	Bit 0	MODE
0	0	Normal operating mode
1	0	PHY Loopback
1	1	Line Loopback

3505 tbl 12

Normal Mode

This mode, Figure 12, supports normal operating conditions: data to be transmitted is transferred to the TC, where it is queued and formatted for transmission by the PMD. Receive data from the PMD is decoded along with its clock for transfer to the receiving "upstream system".

PHY Loopback

As Figure 13 illustrates below, this loopback mode provides a connection within the PHY from the transmit PHY-ATM interface to the PHY-ATM receive interface. Note that while this mode is operating, no data is forwarded to or received from the line interface.

Line Loopback

Figure 14 might also be called “remote loopback” since it provides for a means to test the overall system, including the line. Since this mode will probably be entered under direction from another system (at a remote location), receive data is also decoded and transferred to the upstream system to allow it to listen for commands. A common example would be a command asking the upstream system to direct the TC to leave this loopback state, and resume normal operations.

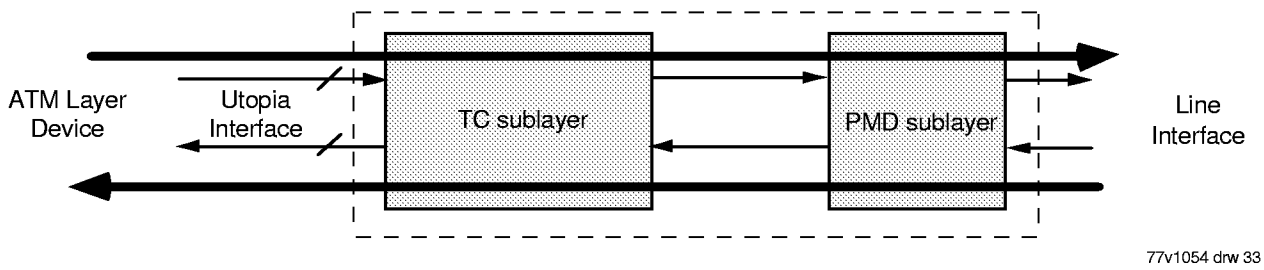


Figure 12. Normal Mode

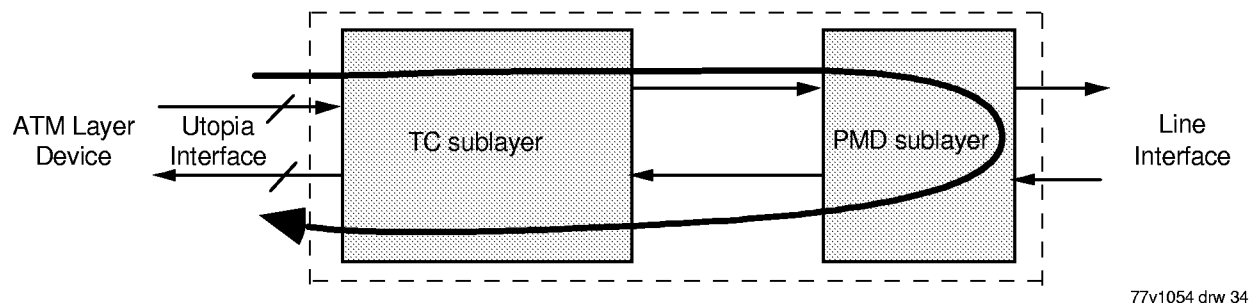


Figure 13. PHY Loopback

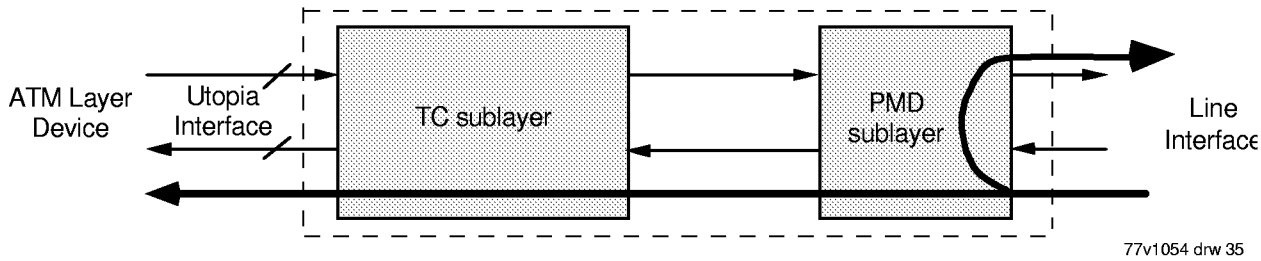


Figure 14. Line Loopback

2. COUNTERS

Several condition counters are provided to assist external systems (e.g. software drivers) in evaluating communications conditions. It is anticipated that these counters will be polled from time to time (user selectable) to evaluate performance. A separate set of registers exists for each channel of the PHY.

- Symbol Error Counters
  - 8 bits
  - counts all invalid 5-bit symbols received
- Transmit Cell Counters
  - 16 bits
  - counts all transmitted cells
- Receive Cell Counters
  - 16 bits
  - counts all received cells, excluding idle cells and HEC errored cells
- Receive HEC Error Counters
  - 5 bits
  - counts all HEC errors received

The TxCell and RxCell counters are sized (16 bits) to provide a full cell count (without roll over) if the counter is read once/second. The Symbol Error counter and HEC Error counter were given sufficient size to indicate exact counts for low error-rate conditions. If these counters overflow, a gross condition is occurring, where additional counter resolution does not provide additional diagnostic benefit.

Reading Counters

1. Decide which counter value is desired. Write to the Counter Select Register(s) (0x06, 0x16 and 0x26) to the bit location corresponding to the desired counter. This loads the High and Low Byte Counter Registers with the selected counter's value, and resets this counter to zero.

NOTE: Only one counter may be enabled at any time in each of the Counter Select Registers.

2. Read the Counter Registers (0x04, 0x14 or 0x24 (low byte)) and (0x05, 0x15 or 0x25 (high byte)) to get the value.

Further reads may be accomplished in the same manner by writing to the Counter Select Registers.

Line Side (Serial) Interface

Each of the threeports has two pins for differential serial transmission, and two pins for differential serial receiving.

PHY TO MAGNETICS INTERFACE

A standard connection to 100Ω and 120Ω unshielded twisted pair cabling is shown in Figure 15. Note that the transmit signal is somewhat attenuated in order to meet the launch amplitude specified by the standards. The receive circuitry is designed to attenuate low frequencies in order to compensate for the high frequency attenuation of the cable.

Also, the receive circuitry biases the positive and negative RX inputs to slightly different voltages. This is done so that the receiver does not receive false signals in the absence of a real signal. This can be important because the 77V1053 does not disable error detection or interrupts when an input signal is not present.

When connecting to UTP at 51.2 Mbps, it is necessary to use magnetics with sufficient bandwidth. Such a device can also operate satisfactorily at 25.6 Mbps.

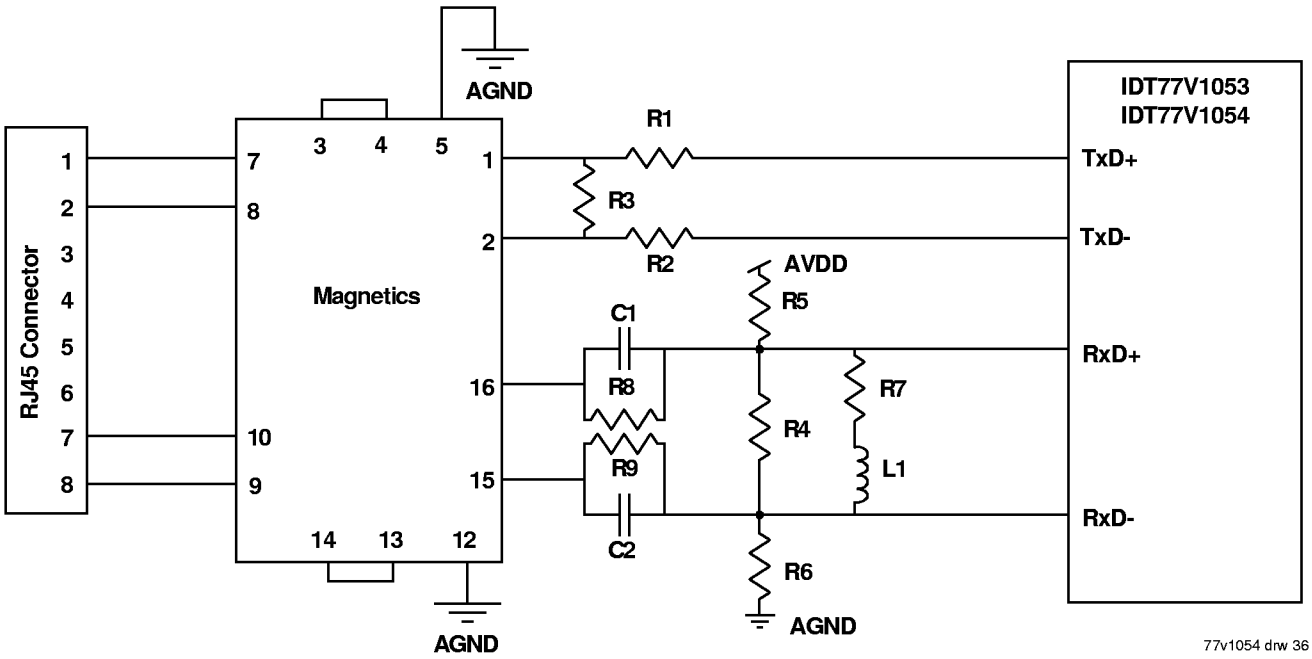


Figure 15. Recommended Connection to Magnetics

Table 3
Analog Component Values

Component	Value	Tolerance
R1	47Ω	±5%
R2	47Ω	±5%
R3	620Ω	±5%
R4	110Ω	±5%
R5	2700Ω	+5%
R6	2700Ω	±5%
R7	82Ω	±5%
R8	33Ω	±5%
R9	33Ω	±5%
C1	470pF	±20%
C2	470pF	±20%
L1	3.3µH	±20%

3505 tbl 13

Magnetics Modules for 25.6 Mbps

Pulse PE-67583 or R4005 (619) 674-8100
Valor SF1153
TDK TLA-6M103 (847) 803-6100

Magnetics Modules for 51.2 Mbps

Pulse R4005 (619) 674-8100

Status and Control Register List

The 77V1053 has 28 registers that are accessible through the utility bus. Each of the threeports has 9 registers dedicated to that port. There is only one register (0x40) which is not port specific.
For those register bits which control operation of the Utopia interface, the operation of the Utopia interface is determined by the registers corresponding to the port which is selected at that particular time. For consistent operation, the Utopia control bits should be programmed the same for all three ports, except for the Utopia 2 port addresses in the Enhanced Control Registers.

Register Name	Register Address			
	Port 0	Port 1	Port 2	All Ports
Master Control Registers	0x00	0x10	0x20	
Interrupt Status Registers	0x01	0x11	0x21	
Diagnostic Control Registers	0x02	0x12	0x22	
LED Driver and HEC Status/control	0x03	0x13	0x23	
Low Byte Counter Register [7:0]	0x04	0x14	0x24	
High Byte Counter Register [15:8]	0x05	0x15	0x25	
Counter Registers Read Select	0x06	0x16	0x26	
Interrupt Mask Registers	0x07	0x17	0x27	
Enhanced Control Registers	0x08	0x18	0x28	
$\overline{\text{RxREF}}$ and $\overline{\text{TxREF}}$ Control Register				0x40

4781 tbl 14

Nomenclature
"Reserved" register bits, if written, should always be written "0"
R/W = register may be read and written via the utility bus
R-only or W-only = register is read-only or write-only
sticky = register bit is cleared after the register containing it is read; all sticky bits are read-only
"0" = 'cleared' or 'not set'
"1" = 'set'

Master Control Registers

Addresses: 0x00, 0x10, 0x20

Bit	Type	Initial State	Function
7	R/W	0	**Reserved**
6	R/W	1 = discard errored cells	**Discard Receive Error Cells** On receipt of any cell with an error (e.g. short cell, invalid command mnemonic, receive HEC error (if enabled)), this cell will be discarded adn will not enter the receive FIFO.
5	R/W	0 = all interrupts	**Enable Cell Error Interrupts Only** If Bit 0 in this register is set (Interrupts Enabled), setting of this bit enables only "Received Cell Error" (as defined in bit 6) to trigger interrupt line.
4	R/W	0 = disabled	**Transmit Data Parity Check** Directs TC to check parity of TxDATA against parity bit located in TXPARITY.
3	R/W	1 = discard idle cells	**Discard Received Idle Cells** Directs TC to discard received idle (VPI/VCI = 0) cells from PMD without signalling external systems.
2	R/W	0 = not halted	**Halt Tx** Halts transmission of data from TC to PMD and forces the TxD outputs to the "0" state.
1	R/W	0	**Reserved**
0	R/W	1 = enable interrupts	**Enable Interrupt Pin (Interrupt Mask Bit)** Enables interrupt output pin (pin 108). If cleared, pin is always high and interrupt is masked. If set, an interrupt will be signaled by setting the interrupt pin to "0". It doesn't affect the Interrupt Status Registers.

77v1053 tbl 15

Interrupt Status Registers

Addresses: 0x01, 0x11, 0x21

Bit	Type	Initial State	Function
7		Reserved	
6	R	0 = Bad Signal	**Good Signal Bit** See definitions on pages 8 and 9. 1 - Good Signal 0 - Bad Signal
5	sticky	0	**HEC error cell received** Set when a HEC error is detected on received cell.
4	sticky	0	**"Short Cell" Received** Interrupt signal which flags received cells with fewer than 53 bytes. This condition is detected when receiving Start-of-Cell command bytes with fewer than 53 bytes between them.
3	sticky	0	**Transmit Parity Error** If Bit 4 of Register 0x00 / 0x10 / 0x20 is set (Transmit Data Parity Check), this interrupt flags a transmit data parity error condition. Odd parity is used.
2	sticky	0	**Receive Signal Condition change** This interrupt is set when the received 'signal' changes either from 'bad to good' or from 'good to bad'.
1	sticky	0	**Received Synbol Error** Set when an undefined 5-bit symbol is received.
0	sticky	0	**Receive FIFO Overflow** Interrupt which indicates when the receive FIFO has filled and cannot accept additional data.

77v1053 tbl 16

Diagnostic Control Registers

Addresses: 0x02, 0x12, 0x22

Bit	Type	Initial State	Function
7	R/W	0 = normal	**Force TxCLAV deassert** This feature can be used during line loopback mode to prevent cells from being passed across the Utopia bus for transmission.
6	R/W	0	**Reserved**
5	R/W	1	**Reserved**
4	R/W	0 = normal	**RFLUSH = Clear Receive FIFO** This signal is used to tell the TC to flush (clear) all data in the receive FIFO. The TC signals this completion by clearing this bit.
3	R/W	0 = normal	**Insert Transmit Payload Error** Tells TC to insert cell payload errors in transmitted cells. This can be used to test error detection and recovery systems at destination station, or, under loopback control, at the local receiving station. This payload error is accomplished by flipping bit 0 of the last cell payload byte.
2	R/W	0 = normal	**Insert Transmit HEC Error** Tells TC to insert HEC error in Byte 5 of cell. This can be used to test error detection and recovery systems in downstream switches, or, under loopback control, the local receiving station. The HEC error is accomplished by flipping bit 0 of the HEC byte.
1,0	R/W	00 = normal	**Loopback Control** **bit # 1 0** 0 0 Normal mode (receive from network) 1 0 PHY Loopback 1 1 Line Loopback

77v1053 tbl 17

LED Driver and HEC Status/Control Registers

Addresses: 0x03, 0x13, 0x23

Bit	Type	Initial State	Function
7		0	Reserved
6	R/W	0 = enable checking	**Disable Receive HEC Checking (HEC Enable)** When not set, the HEC is calculated on first 4 bytes of received cell, and compared against the 5th byte. When set (= 1), the HEC byte is not checked.
5	R/W	0 = enable calculate & replace	**Disable Xmit HEC Calculate & Replace** When set, the 5th header byte of cells queued for transmit is not replaced with the HEC calculated across the first four bytes of that cell.
4,3	R/W	00 = 1 cycle	**$\overline{\text{RxREF}}$ Pulse Width Select** bit # 4 3 0 0 RxREF active for 1 OSC cycle 0 1 RxREF active for 2 OSC cycles 1 0 RxREF active for 4 OSC cycles 1 1 RxREF active for 8 OSC cycles
2	R	1 = empty	**FIFO Status** 1 = TxFIFO empty 0 = TxFIFO not empty
1	R	0	**TxLED Status** 1 = Cell Received 0 = Cell NOT Received
0	R	0	**RxLED Status** 1 = Cell Received 0 = Cell NOT Received

4781 tbl 18

Low Byte Counter Registers [7:0]

Addresses: 0x04, 0x14, 0x24

Bit	Type	Initial State	Function
[7:0]	R	0x00	Provides low-byte of counter value selected via registers 0x06, 0x16 and 0x26.

4781 tbl 19

High Byte Counter Registers [15:8]

Addresses: 0x05, 0x15, 0x25

Bit	Type	Initial State	Function
[7:0]	R	0x00	Provides high-byte of counter value selected via registers 0x06, 0x16 and 0x26.

4781 tbl 20

Counter Select Registers

Addresses: 0x06, 0x16, 0x26

Bit	Type	Initial State	Function
7	—	—	Reserved.
6	—	—	Reserved.
5	—	—	Reserved.
4	—	—	Reserved.
3	W	0	Symbol Error Counter.
2	W	0	TxCell Counter.
1	W	0	RxCell Counter.
0	W	0	Receive HEC Error Counter.

4781 tbl 21

NOTE: For proper operation, only one bit may be set in a Counter Select Register at any time.

Interrupt Mask Registers

Addresses: 0x07, 0x17, 0x27

Bit	Type	Initial State	Function
7		0	Reserved.
6		0	Reserved.
5	R/W	0 = interrupt enabled	HEC Error Cell.
4	R/W	0 = interrupt enabled	Short Cut Error.
3	R/W	0 = interrupt enabled	Transmit Parity Error.
2	R/W	0 = interrupt enabled	Receive Signal Condition Change.
1	R/W	0 = interrupt enabled	Received Cell Symbol Error.
0	R/W	0 = interrupt enabled	Receive FIFO Overflow.

4781 tbl 22

NOTE:
1. When set to "1", these bits mask the corresponding interrupts going to the interrupt pin ($\overline{INT}$). When set to "0", the interrupts are unmasked. These interrupts correspond to the interrupt status bits in the Interrupt Status Registers.

Enhanced Control Registers

Addresses: 0x08, 0x18, 0x28

Bit	Type	Initial State	Function
7	W	0 = not reset	**Individual Port Software Reset** 1 = Reset. This bit is self-clearing; it isn't necessary to write "0" to exit reset.
6	R/W	0 = OSC	**Transmit Line Clock (or Loop Timing Mode)** When set to 0, the OSC input is used as the transmit line clock. When set to 1, the recovered receive clock is used as the transmit line clock.
5	R/W	0	**Reserved**
4-0	R/W	Port 0 (Reg 0x08): 00000 Port 1 (Reg 0x18): 00001 Port 2 (Reg 0x28): 00010	**Utopia 2 Port Address** When operating in Utopia 2 Mode, these register bits determine the Utopia 2 port address

77v1053 tbl 23

$\overline{RxREF}$ and $\overline{TxREF}$ Control Register

Addresses: 0x40

Bit	Type	Initial State	Function
7,6	R/W	0 = $\overline{RxREF0}$ (Port 0)	**RxREF Source Select** Selects which of the four ports (0 to 3) is the source of $\overline{RxREF}$.
5	W	0 = not reset	**Master Software Reset** 1 = Reset. This bit is self-clearing; it isn't necessary to write "0" to exit reset.
4-3		00	**Reserved**
2-0	R/W	0000 = not looped	**RxREF to TxREF Loop Select** When set to 0, $\overline{TxREF}$ is used to generate X_8 timing marker commands. When set to 1, $\overline{TxREF}$ input is ignored, and received X_8 timing commands are looped back and added to the transmit stream of that same port. See Figure 4. bit 2: port 2 bit 1: port 1 bit 0: port 0

77v1053 tbl 24

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +5.5	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +120	°C
I_{OUT}	DC Output Current	50	mA

3505 tbl 25

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND, AGND	VDD, AVDD
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

3505 tbl 27

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Digital Supply Voltage	3.0	3.3	3.6	V
GND	Digital Ground Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	5.25	V
VIL	Input Low Voltage	-0.3	—	0.8	V
AVDD	Analog Supply Voltage	3.0	3.3	3.6	V
AGND	Analog Ground Voltage	0	0	0	V
VDIF	VDD - AVDD	-0.5	0	0.5	V

3505 tbl 26

Capacitance (T_A = +25°C, f = 1MHz)

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	10	pF
C_{IO}(1)	I/O Capacitance	V_{OUT} = 0V	10	pF

3505 tbl 28

NOTES:
1. Characterized values, not currently tested.

DC Electrical Characteristics (All Pins except TX+/- and RX+/-)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	Gnd ≤ VIN ≤ VDD	-5	5	µA
I_{LO}	I/O (as input) Leakage Current	Gnd ≤ VIN≤ VDD	-10	10	µA
V_{OH1}(1)	Output Logic "1" Voltage	I_{OH} = -2mA, VDD = min.	2.4	—	V
V_{OH2}(2)	Output Logic "1" Voltage	I_{OH} = -8mA, VDD = min.	2.4	—	V
V_{OL}(3)	Output Logic "0" Voltage	I_{OL} = 8mA, VDD = min.	—	0.4	V
I_{DD1}(4,5)	Digital Power Supply Current - VDD	OSC = 32 MHz, all outputs unloaded	—	140	mA
I_{DD2}(5)	Analog Power Supply Current - AVDD	OSC = 32 MHz, all outputs unloaded	—	140	mA

3505 tbl 29

NOTES:
1. For AD[7:0] pins only.
2. For all output pins except AD[7:0], $\overline{INT}$ and TX+/-.
3. For all output pins except TX+/-.
4. Add 15mA for each TX+/- pair that is driving a load
5. Total supply current is the sum of IDD1 and IDD2.

DC Electrical Characteristics (TX+/- Output Pins Only)

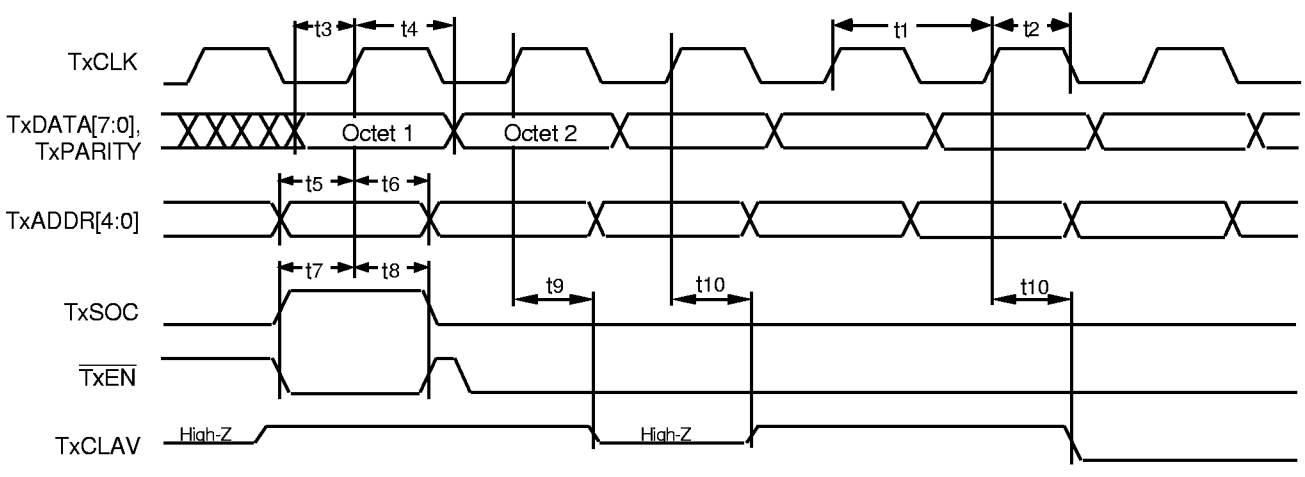
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output Logic High Voltage	I_{OH} = -20mA	VDD - 0.5V	—	V
V_{OL}	Output Logic Low Voltage	I_{OL} = 20mA	—	0.5	V

3505 tbl 30

UTOPIA Level 2 Bus Timing Parameters

Symbol	Parameter	Min.	Max.	Unit
t1	TxCLK Frequency	0.2	50	MHz
t2	TxCLK Duty Cycle (% of t1)	40	60	%
t3	TxDATA[7:0], TxPARITY Setup Time to TxCLK	7	—	ns
t4	TxDATA[7:0], TxPARITY Hold Time to TxCLK	2	—	ns
t5	TxADDR[4:0], Setup Time to TxCLK	7	—	ns
t6	TxADDR[4:0}, Hold Time to TxCLK	2	—	ns
t7	TxSOC, $\overline{\text{TxEN}}$ Setup Time to TxCLK	7	—	ns
t8	TxSOC, $\overline{\text{TxEN}}$ Hold Time to TxCLK	2	—	ns
t9	TxCLK to TxCLAV High-Z	2	10	ns
t10	TxCLK to TxCLAV Low-Z (min) and Valid (max)	2	14	ns
t12	RxCLK Frequency	0.2	50	MHz
t13	RxCLK Duty Cycle (% of t12)	40	60	%
t14	$\overline{\text{RxEN}}$ Setup Time to RxCLK	7	—	ns
t15	$\overline{\text{RxEN}}$ Hold Time to RxCLK	2	—	ns
t16	RxADDR[4:0] Setup Time to RxCLK	7	—	ns
t17	RxADDR[4:0] Hold Time to RxCLK	2	—	ns
t18	RxCLK to RxCLAV High-Z	2	14	ns
t19	RxCLK to RxCLAV Low-Z (min) and Valid (max)	2	10	ns
t20	RxCLK to RxSOC High-Z	2	10	ns
t21	RxCLK to RxSOC Low-Z (min) and Valid (max)	2	14	ns
t22	RxCLK to RxDATA, RxPARITY High-Z	2	10	ns
t23	RxCLK to RxDATA, RxPARITY Low-Z (min) and Valid (max)	2	14	ns

77v1054 tbl 31



77v1054 drw 37

Figure 16. UTOPIA Level 2 Transmit

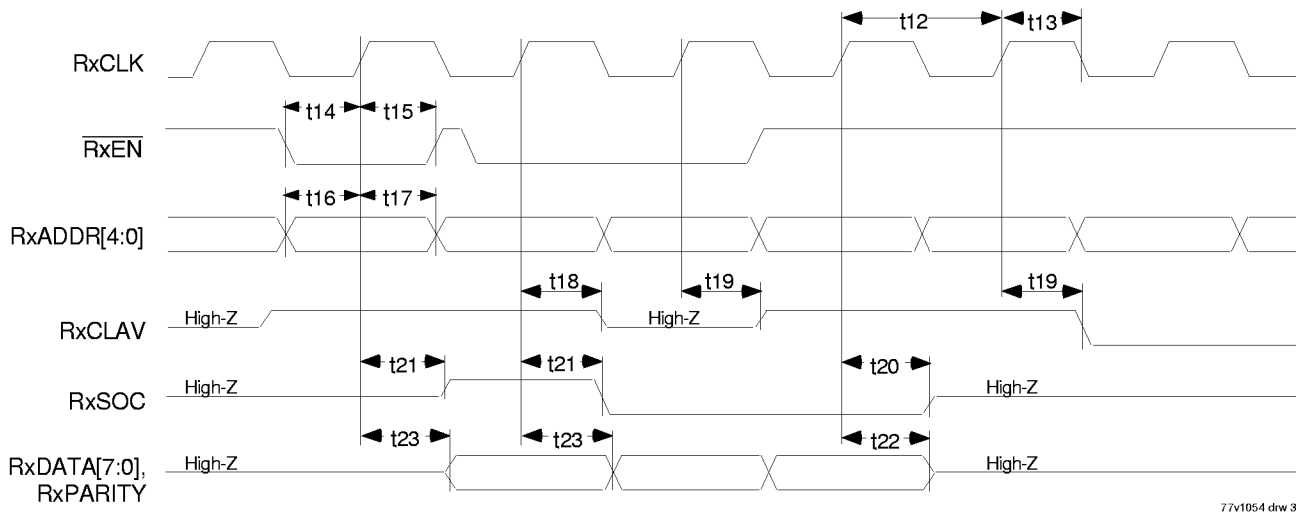


Figure 17. UTOPIA Level 2 Receive

Utility Bus Read Cycle

Name	Min	Max	Unit	Description
Tas	10	—	ns	Address setup to ALE
Tcsrd	0	—	ns	Chip select to read enable
Tah	5	—	ns	Address hold to ALE
Tapw	10	—	ns	ALE min pulse width
Ttria	—	0	ns	Address tri-state to $\overline{RD}$ assert
Trdpw	20	—	ns	Min. $\overline{RD}$ pulse width
Tdh	0	—	ns	Data Valid hold time
Tch	0	—	ns	$\overline{RD}$ deassert to $\overline{CS}$ deassert
Ttrid	—	10	ns	$\overline{RD}$ deassert to data tri-state
Trd	5	18	ns	Read Data access
Tar	5	—	ns	ALE low to start of read
Trdd	0	—	ns	Start of read to Data low-Z

3505 tbl 34

Utility Bus Write Cycle

Name	Min	Max	Unit	Description
Tapw	10	—	ns	ALE min pulse widt
Tas	10	—	ns	Address set up to ALE
Tah	5	—	ns	Address hold time to ALE
Tacswr	0	—	ns	$\overline{CS}$ Assert to $\overline{WR}$
Twrpw	20	—	ns	Min. $\overline{WR}$ pulse width
Tdws	20	—	ns	Write Data set up
Tdwh	10	—	ns	Write Data hold time
Tch	0	—	ns	$\overline{WR}$ deassert to $\overline{CS}$ deassert
Taw	20	—	ns	ALE low to end of write

3505 tbl 35

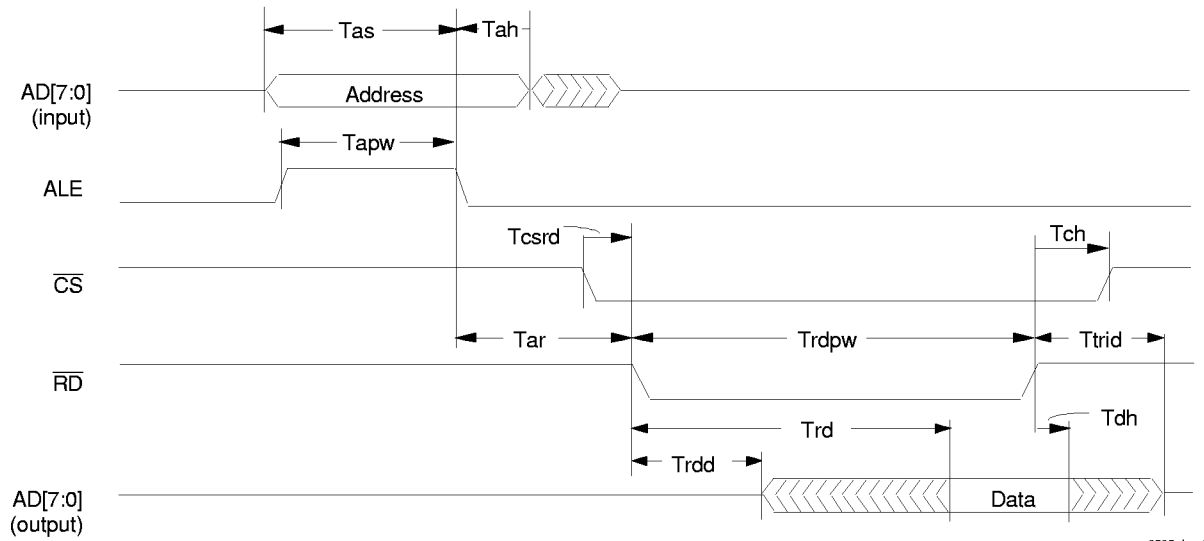


Figure 18. Utility Bus Read Cycle

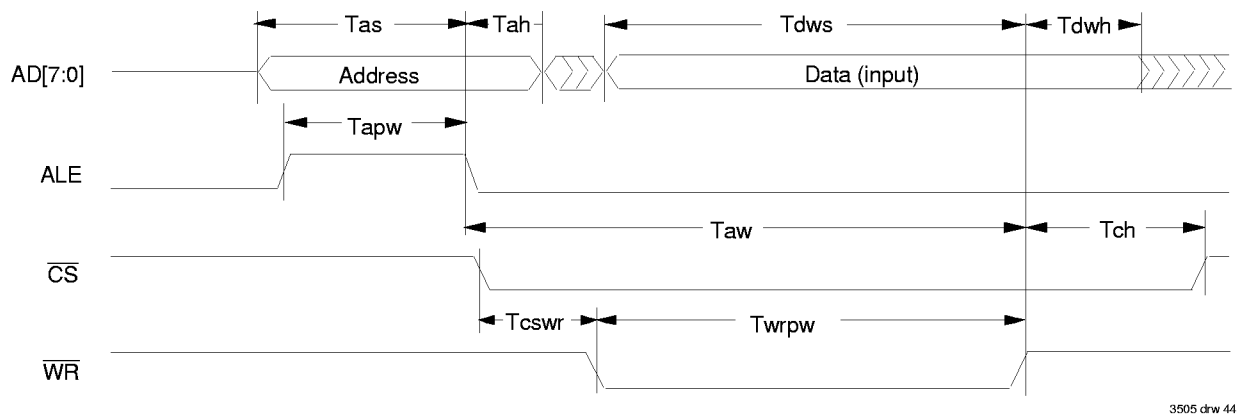


Figure 19. Utility Bus Write Cycle

OSC, $\overline{\text{RXREF}}$, $\overline{\text{TXREF}}$ and Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tcyc	OSC cycle period (25.6 Mbps) (51.2 Mbps)	30 15	31.25 15.625	33 16.5	ns ns
Tch	OSC high time	40	—	60	%
Tcl	OSC low time	40	—	60	%
Tcc	OSC cycle to cycle period variation	—	—	1	%
Trrpd(1)	OSC to $\overline{\text{RXREF}}$ Propagation Delay	1	—	30	ns
Ttrh	$\overline{\text{TXREF}}$ High Time	35	—	—	ns
Ttrl	$\overline{\text{TXREF}}$ Low Time	35	—	—	ns
Trspw(2)	Minimum $\overline{\text{RST}}$ Pulse Width	two TxCLK cycles two RxCLK cycles two OSC cycles	—	—	—

77v1054 tbl 36

NOTES:
1. The width of the $\overline{\text{RXREF}}$ pulse is programmable in the LED Driver and HEC Status/Control Registers.
2. The minimum $\overline{\text{RESET}}$ Pulse Width is either two RxCLK cycles, two TxCLK cycles or two OSC cycles, whichever is greater.

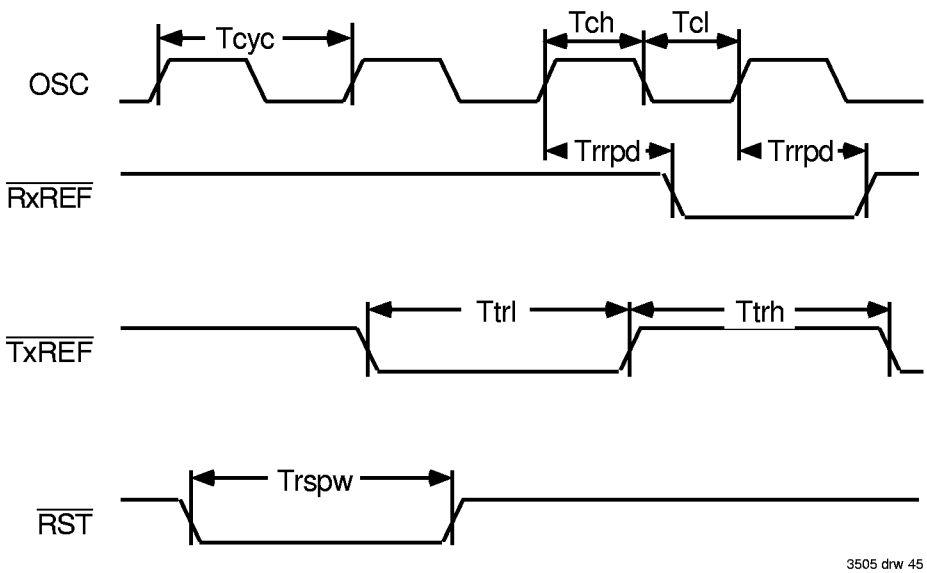


Figure 20. OSC, $\overline{\text{RXREF}}$, $\overline{\text{TXREF}}$ and Reset Timing

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 21

77v1054 tbl 37

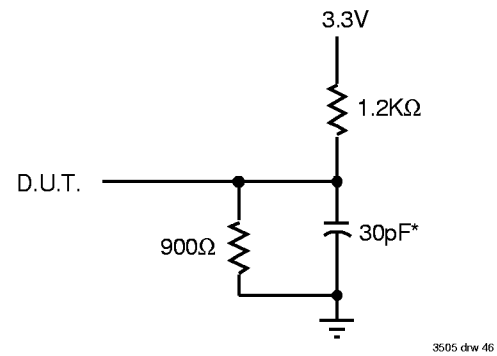


Figure 21. Output Load

* Includes jig and scope capacitances.

A note about Figures 22 and 23: The ATM Forum and ITU-T standards for 25 Mbps ATM define "Network" and "User" interfaces. They are identical except that transmit and receive are switched between the two. A Network device can be connected directly to a User device with a straight-through cable. User-to-User or Network-to-Network connections require a cable with 1-to-7 and 2-to-8 crossovers.

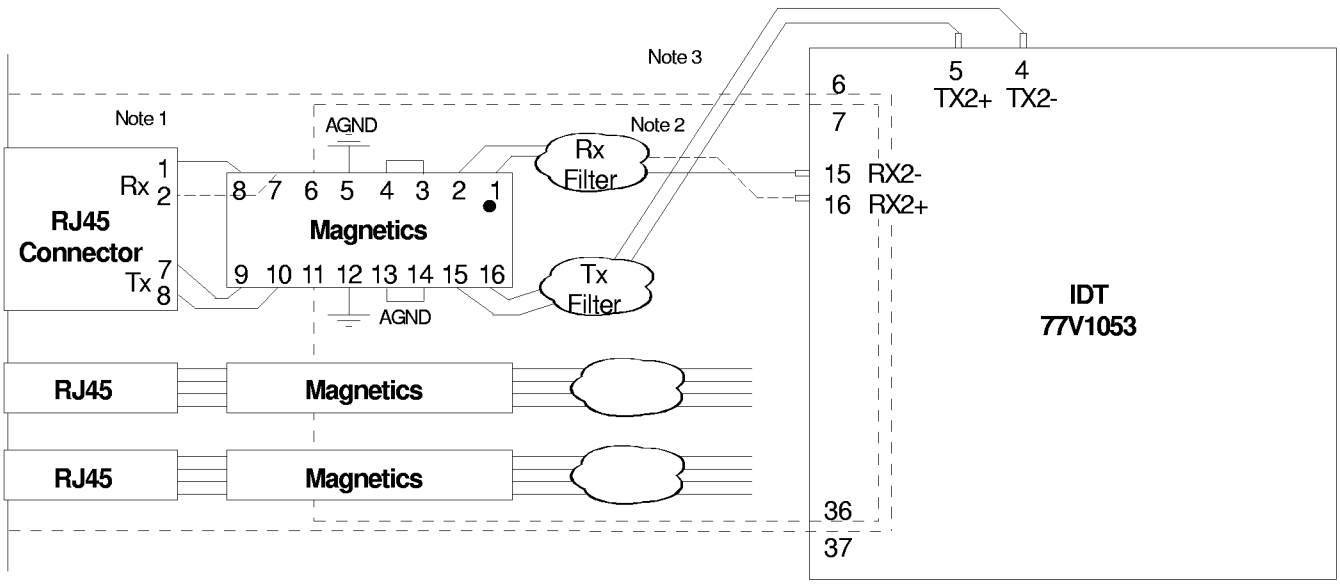


Figure 22. PC Board Layout for ATM Network

NOTES:
1. No power or ground plane inside this area.
2. Analog power plane inside this area.
3. Digital power plane inside this area.
4. A single ground plane should extend over the area covered by the analog and digital power planes, without breaks.
5. All analog signal traces should avoid 90° corners.

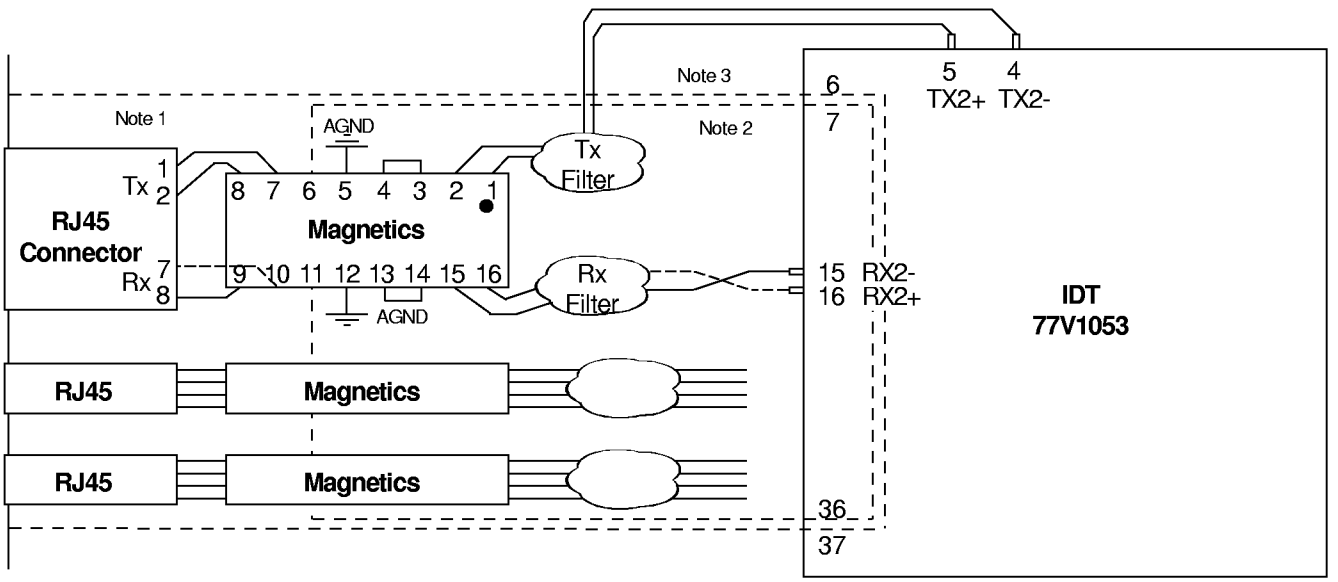
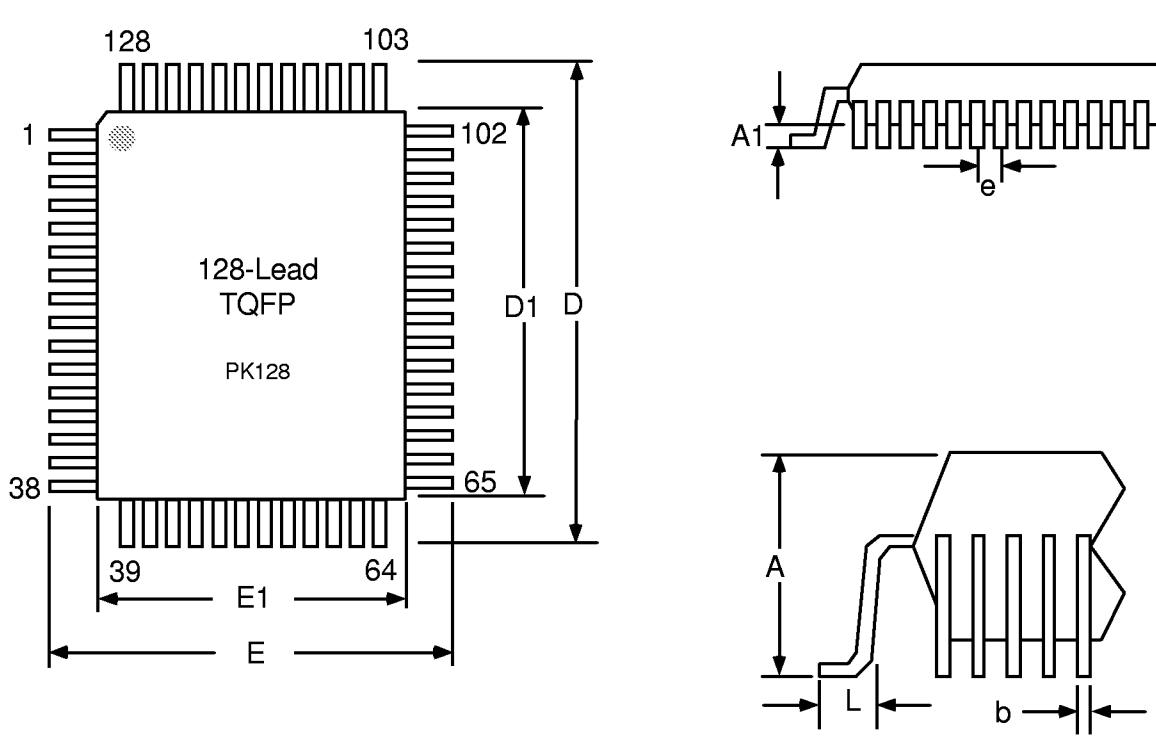


Figure 23. PC Board Layout for ATM User

NOTES:
1. No power or ground plane inside this area.
2. Analog power plane inside this area.
3. Digital power plane inside this area.
4. A single ground plane should extend over the area covered by the analog and digital power planes, without breaks.
5. All analog signal traces should avoid 90° corners.

Package Dimensions

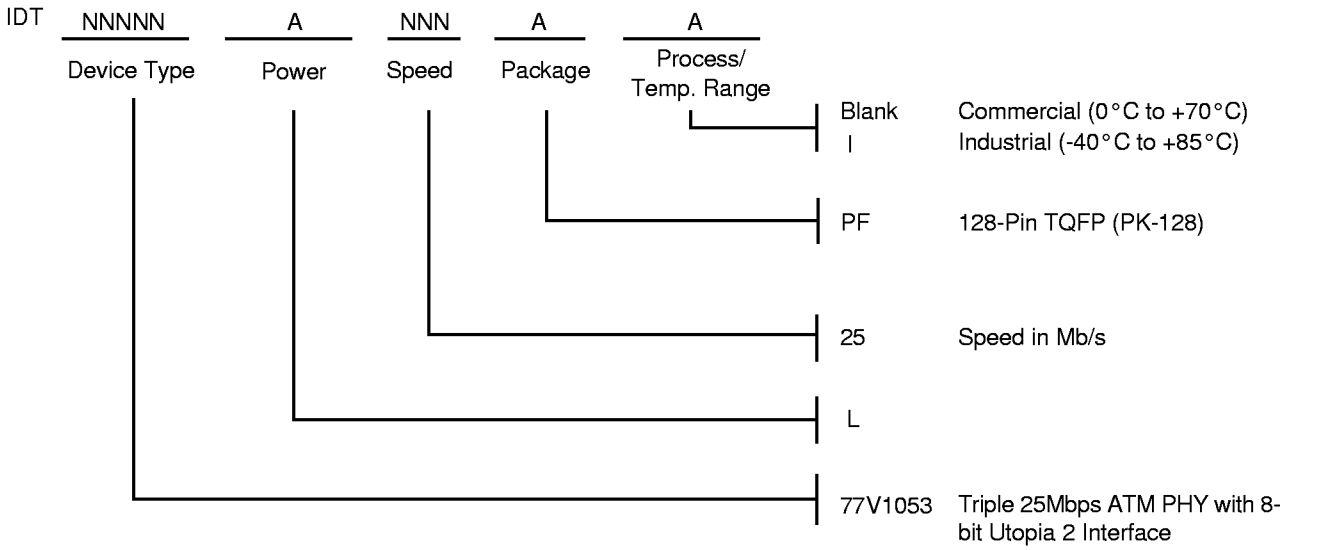


SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	-	22.00	-
D1	-	20.00	-
E	-	16.00	-
E1	-	14.00	-
L	0.45	-	0.75
e	-	0.50	-
b	0.17	0.22	0.27

Dimensions are in millimeters

77v1054 drw 49

Ordering Information



77v1053 drw 50

Preliminary Datasheet: Definition

"PRELIMINARY' datasheets contain descriptions for products soon to be, or recently released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

Datasheet Document History

9/13/99 PRELIMINARY. Initial Release.

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-5166
fax: 408-492-8674
www.idt.com

for Tech Support:
408-953-2529
atmhelp@idt.com