DATA SHEET

OKI TELECOMMUNICATIONS PRODUCTS

ML7041
Audio CODEC

September 2000

Oki Semiconductor

CONTENT

Oki Semiconductor

ML7041

Audio CODEC

GENERAL DESCRIPTION

The ML7041 is a single channel, low-voltage linear Codec targeting the digital handset market including CDMA and TDMA applications. The ML7041 sets a new standard for functionality by incorporating all major peripheral handset features, including speaker driver, tone generator, and voice detection circuits. The ML7041, a third generation Oki linear Codec, offers an improved feature set by incorporating a robust amplifier circuit capability on-chip to drive the latest cutting-edge, low-impedance dynamic speakers commonly used in handsets.

The ML7041 applies an Oki application-specific DSP architecture to improve the filtering performance and generate telephony tones. Applying an optimized DSP core on-chip allows sigma-delta post-equalization processing, which improves signal-to-noise while lowering power consumption.

The ML7041 design concept is based on an advanced Oki 0.45-um double-poly CMOS process providing sufficiently low transistor threshold voltages to allow 2.4-V operation to maximize a handset's battery life.

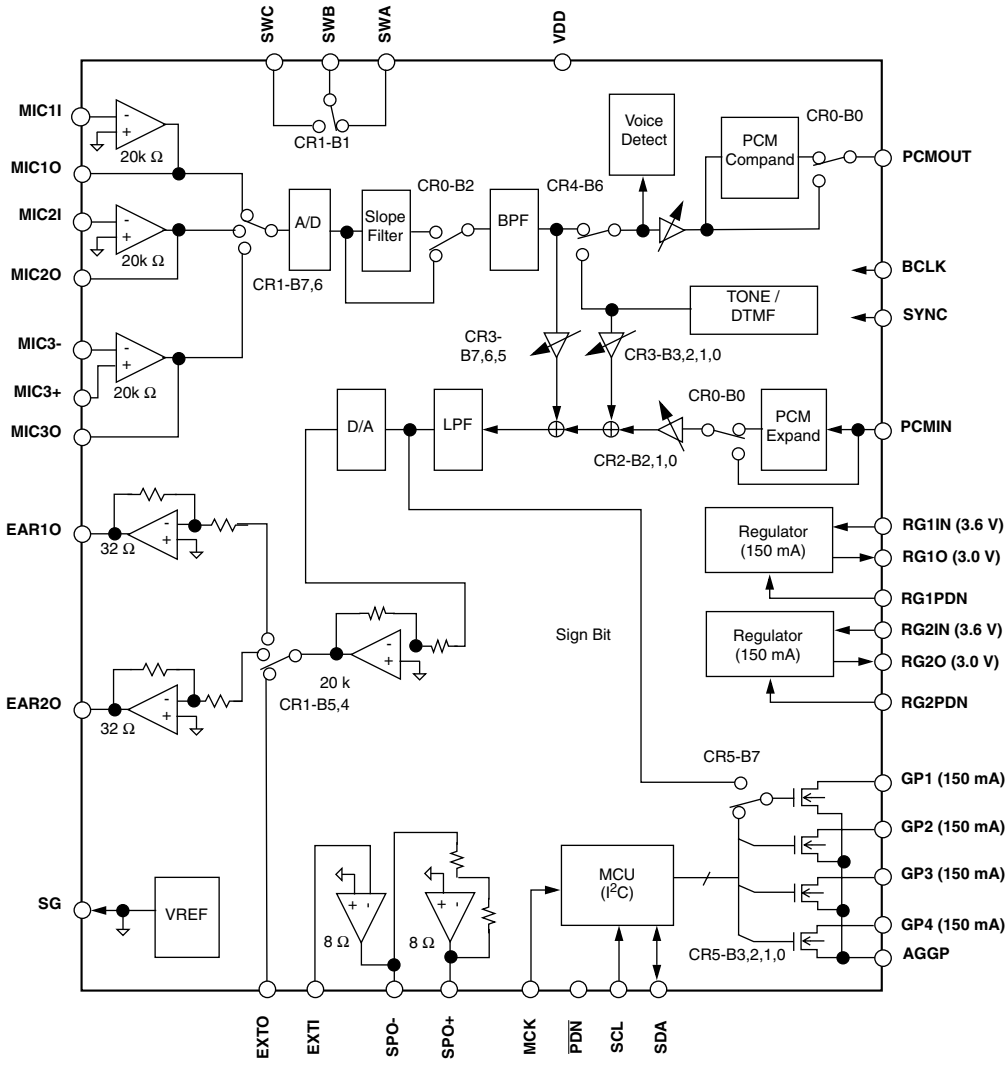
Oki's linear CODEC provides a flexible user interface for two microphone, one headset, two general-purpose inputs and a speaker output with on-chip adjustable gain control. The ML7041 will unburden the external, baseband DSP engine by generating all common telephony tones such as DTMF, side, and information tones. An added feature is the new integrated transmit voice detection scheme (VOX) which no longer requires firmware support on the CDMA chipset.

FEATURES

- Single 3-V Power Supply Operation: VDD: 2.4 V to 3.3 V for increased battery life
- Coding format: PCM μ-law/PCM A-law/14-bit linear mode selectable, provides flexibility
- PCM interface timing: Long frame and short frame synchronous timing simplifies interface
- Transmit/receive full-duplex operation
- Serial PCM transmission data rate: 64 kbps to 2048 kbps
- Low Power Consumption
    - Operating Mode: 15 mW typ. (VDD=3.0 V)
    - Power-Down Mode: 3 μW typ. (VDD=3.0 V)
- Master Clock Frequency: 2.048 MHz
- Integrated high-gain Analog Output Stage: 100 mW (differential) amplifier output for driving receiver speaker
    - Capable of driving an 8-W load.
- Integrated Analog Output Stage: 6.6 mW (single-ended) amplifier output for driving earphones speaker
    - Capable of driving a 32-W load.
- Built-in dual low-dropout regulator (150 mAx2) supports microphone and headset
- Built-in quad general purpose driver (150 mAx4) supports hands-free and other connections

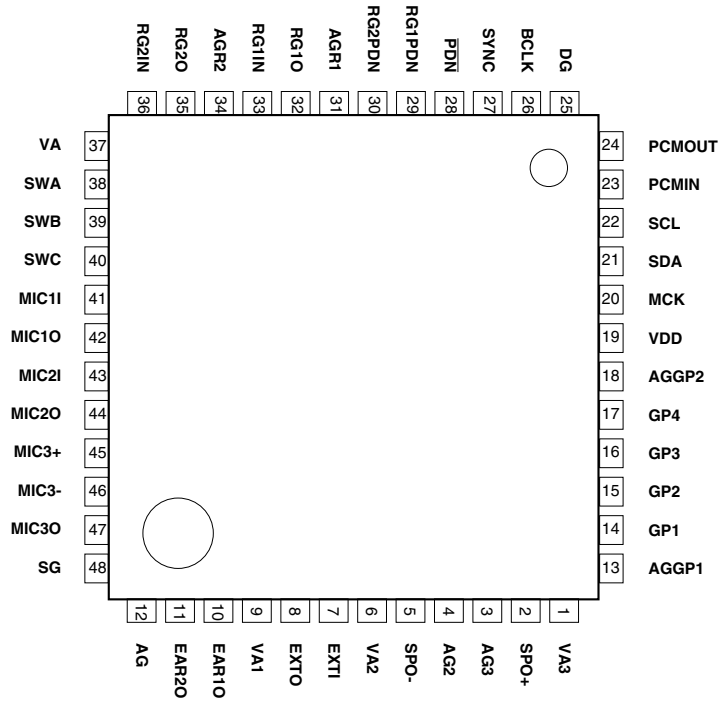
- Transmit/receive mute, transmit/receive programmable gain control
- Built-in side tone path eliminates external ICs
- Built-in DTMF tone generator eliminates external DSP
- Selectable transmit slope filter allows frequency fine tuning
- Popular I^2C interface to popular processors lowers pin counts
- Built-in transmit voice signal detector provides VOX functionality
- Package: 48-pin plastic TQFP (TQFP48-P-0707-050-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

TQFP48-P-0707-050-K



PIN LIST

Pin	Symbol	Type	Description	Under Powerdown State
1	AG	-	Analog ground (0 V)	-
2	EAR2O	O	Receive side voice amplifier output	High impedance
3	EAR1O	O	Receive side voice amplifier output	High impedance
4	VA1	-	Analog power supply (3.0 V)	-
5	EXTO	O	Receive side voice amplifier output	High impedance
6	EXTI	I	Receive side voice amplifier input	-
7	VA2	-	Analog power supply 2 (3.0 V)	-
8	SPO-	O	Receive side voice amplifier output-	High impedance
9	AG2	-	Analog ground 2 (0 V)	-
10	AG3	-	Analog ground 3 (0 V)	-
11	SPO+	O	Receive side voice amplifier output+	High impedance
12	VA3	-	Analog power supply 3 (3.0 V)	-
13	AGGP1	-	Ground1 for general purpose port (0 V)	-
14	GP1	O	General purpose port 1 output (Open Drain)	High impedance
15	GP2	O	General purpose port 2 output (Open Drain)	High impedance
16	GP3	O	General purpose port 3 output (Open Drain)	High impedance
17	GP4	O	General purpose port 4 output (Open Drain)	High impedance
18	AGGP2	-	Ground2 for general purpose port (0 V)	-
19	VDD	-	Digital power supply (3.0 V)	-
20	MCK	I	Master clock input (2.048 MHz)	-
21	SDA	IO	I^2C data input/output	High impedance
22	SCL	I	I^2C shift clock input	-
23	PCMIN	I	Receive side PCM signal input	-
24	PCMOUT	O	Transmit side PCM signal output	'H'
25	DG	-	Digital ground (0 V)	-
26	BCLK	I	PCM data shift clock input	-
27	SYNC	I	PCM data shift sync signal input	-
28	$\overline{PDN}$	I	Power down control input	-
29	RG1PDN	I	Power down input for regulator 1	-
30	RG2PDN	I	Power down input for regulator 2	-
31	AGR1	-	Ground for regulator 1 (0 V)	-
32	RG1O	O	Regulator 1 output	'L' (RG1PDN=L)
33	RG1IN	I	Regulator 1 input	-
34	AGR2	-	Ground for regulator 2 (0 V)	-
35	RG2O	O	Regulator 2 output	'L' (RG2PDN=L)
36	RG2IN	I	Regulator 2 input	-
37	VA	-	Analog power supply (3.0 V)	-
38	SWA	IO	Analog switch A	-
39	SWB	IO	Analog switch B	-
40	SWC	IO	Analog switch C	-
41	MIC1I	I	Transmit side amplifier inverting input	-
42	MIC1O	O	Transmit side amplifier output	High impedance

Pin	Symbol	Type	Description	Under Powerdown State
43	MIC2I	I	Transmit side amplifier inverting input	-
44	MIC2O	O	Transmit side amplifier output	High impedance
45	MIC3+	I	Transmit side amplifier non-inverting input	-
46	MIC3-	I	Transmit side amplifier inverting input	-
47	MIC3O	O	Transmit side amplifier output	High impedance
48	SG	O	Analog signal ground (1.4 V)	'L'

PIN FUNCTIONAL DESCRIPTION

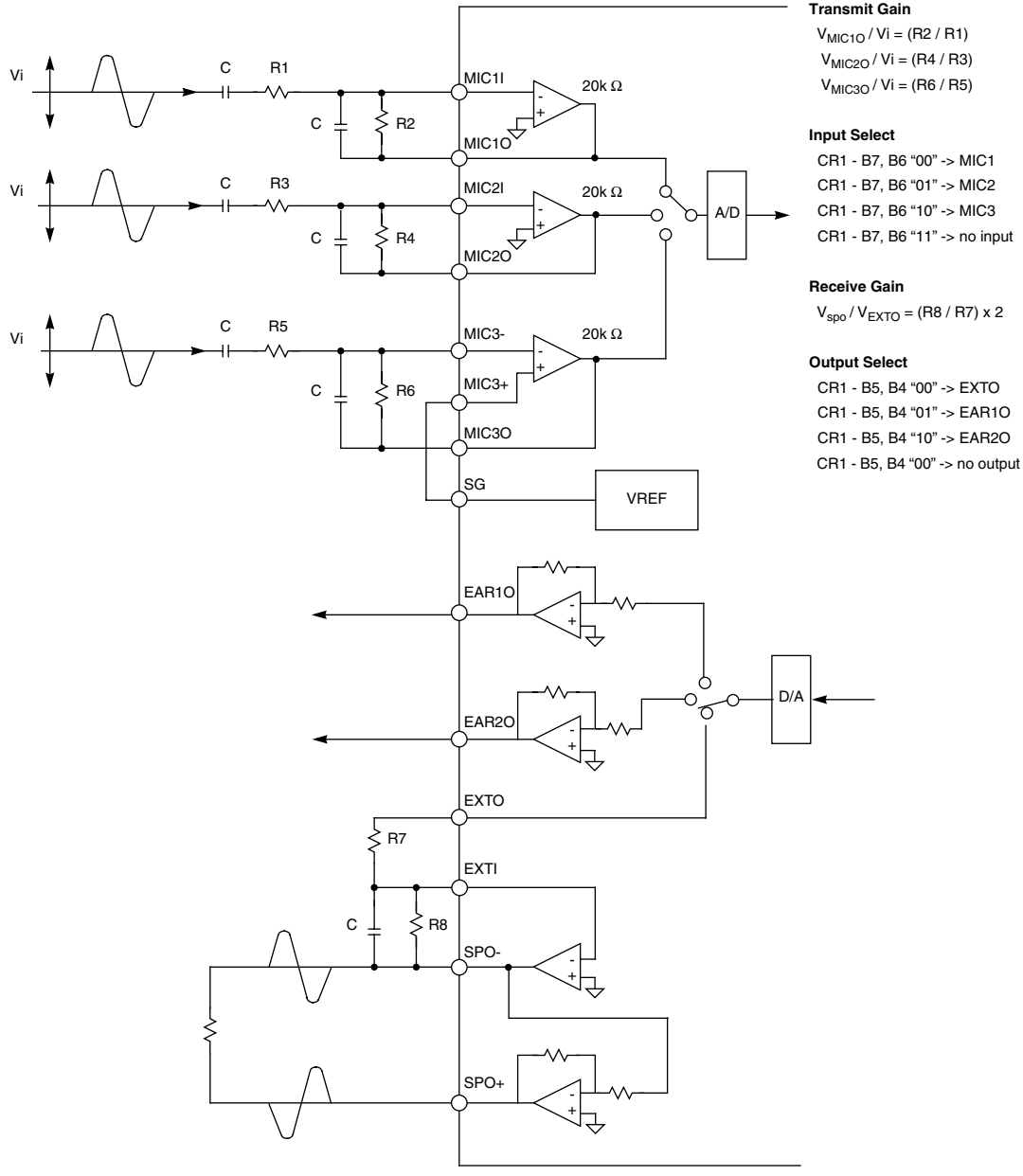


Figure 1. Analog Interface

MIC1I, MIC1O, MIC2I, MIC2O, MIC3-, MIC3+, MIC3-

Transmit analog inputs and the output for transmit gain adjustment.

MIC1I, MIC2I, and MIC3- connect to inverting input of the internal transmit amplifier. MIC3+ connects to non-inverting input of the internal transmit amplifier. MIC1O, MIC2O, and MIC3O connect to the internal transmit amplifier output. These input signals are controlled by control register CR1-B7, B6.

Refer to Figure 1 on page 8 for gain adjustment.

EAR1O, EAR2O, EXTO, EXTI, SPO-, SPO+

Receive analog output and the output for receive gain adjustment. EAR1O, EAR2O are the receive filter outputs. EAR1O, EAR2O can directly drive 32 W load.

EXTO is the receive filter output for the voice signal. SPO+ and SPO- are differential analog signal outputs which can directly drive 8W load. Refer to Figure 1 on page 8 above.

SG

Analog signal ground.

The output voltage of this pin is approximately 1.4 V. Put the bypass capacitors 0.1 µF ceramic type between this pin and AG to get the specified noise characteristics. During power-down, this output voltage is 0 V.

SWA, SWB, SWC

Used for internal analog switch. The pin SWB connects to the pin SWA or the pin SWC. This is controlled by CR1-B1.

RG1PDN, RG1IN, RG1O

Used for Regulator 1. The RG1PDN pin is power down input. When set to logic "0" the regulator 1 changes to the power down state. Since the power down is controlled by a logical OR with CR5-B4 of the control register, set CR5-B4 to logic "0" when using this pin. The RG1IN pin is input to the regulator 1. The RG1O pin is output from the regulator 1.

RG2PDN, RG2IN, RG2O

Used for Regulator 2. The RG2PDN pin is power down input. When set to logic "0" the regulator 2 changes to the power down state. Since the power down is controlled by a logical OR with CR5-B5 of the control register, set CR5-B5 to logic "0" when using this pin. The RG2IN pin is input to the regulator 2. The RG2O pin is output from the regulator 2.

GP1, GP2, GP3, GP4

General purpose Driver output. Each pin is controlled by CR5-B1 through CR5-B4.

VDD, VA, VA1, VA2, VA3

+3 V power supply for analog. VDD is the digital power supply.VA, VA1, VA2 and VA3 is the analog power supply. Since these pins are separated in the device, connect them as close as possible on the PCB.

DG, AG, AG1, AG2, AG3, AGR1, AGR2, AGGP1, AGGP2

Ground. DG is the digital system ground. AG, AG1, AG2, AG3, AGR1, AGR2, AGGP1 and AGGP2 is the analog system ground. Since these pins are separated in the device, connect them as close as possible on the PCB.

$\overline{\text{PDN}}$

Power down and reset control input.

When set to digital "0", the system changes to the power down state and control register is reset. Since the power down mode is controlled by a logical OR with CR0-B5 of the control register, set CR0-B5 to logic "0" when using this pin. The reset pulse width must be 200 ns or more.

Be sure to reset the control registers after turning on the power.

MCK

Master clock input.

The frequency must be 2.048 MHz. MCK can be asynchronous with SYNC and BCLK.

BCLK

Shift clock input for the PCM data.

The frequency is set in the range of 64 kHz to 2048 kHz.

SYNC

Transmit and receive PCM data 8 kHz synchronous signal input.

Synchronize this signal with BCLK signal. Figure 2 on page 11.

PCMOUT

Transmit PCM data output.

This PCM output signal is output from MSB synchronously with the rising edge of BCLK and SYNC.

Refer to Figure 2 on page 11.

PCMIN

Receive PCM data input.

This PCM input signal is shifted in on falling edge of BCLK and is input from MSB.

Refer to Figure 2 on page 11.

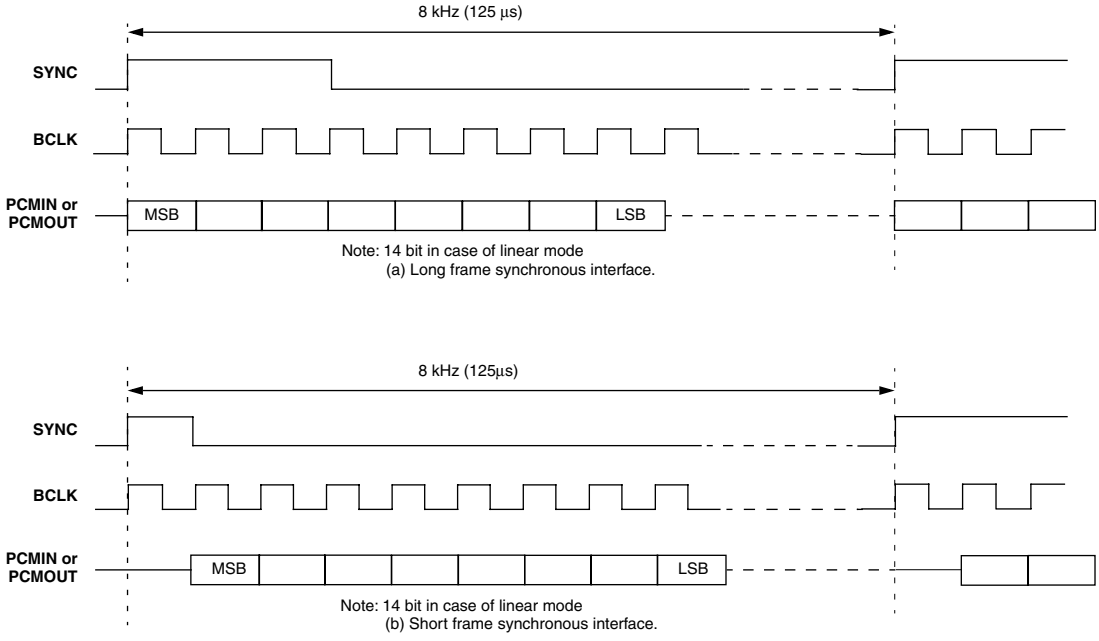


Figure 2. PCM Interface Basic Timing Diagram

SDA, SCL

SDA is the serial data input/output pin and SCL is the serial clock input pin. SDA requires pull-up resistor.

A master clock is necessary while read and writing of the data.

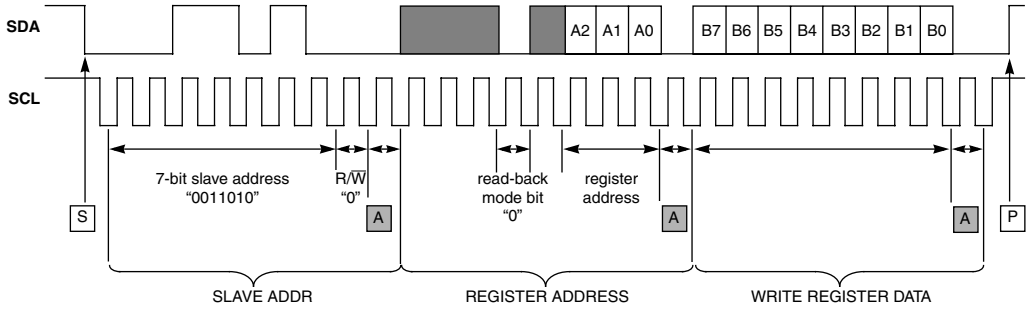
Transfer Format

The I^2C bus of the ML7041 operates the interface using the control register. Writes and reads to the control register are enabled to access with the following transfer format. See Figure 6 on page 27.

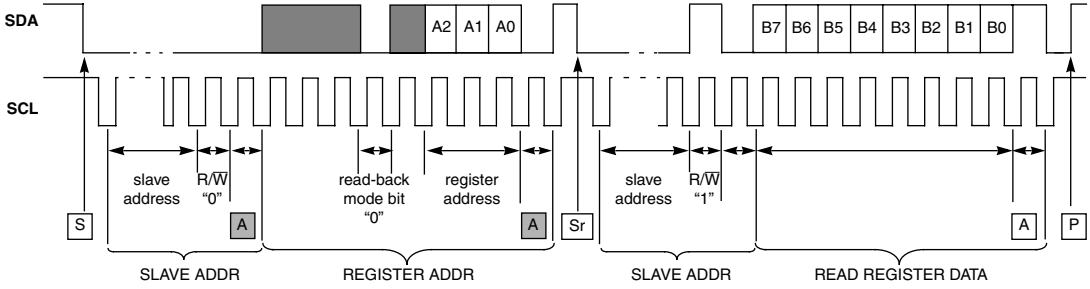
The register address is 3 bits and the register data is 8 bits.

Table , "Register Map," on page 13 shows the register map.

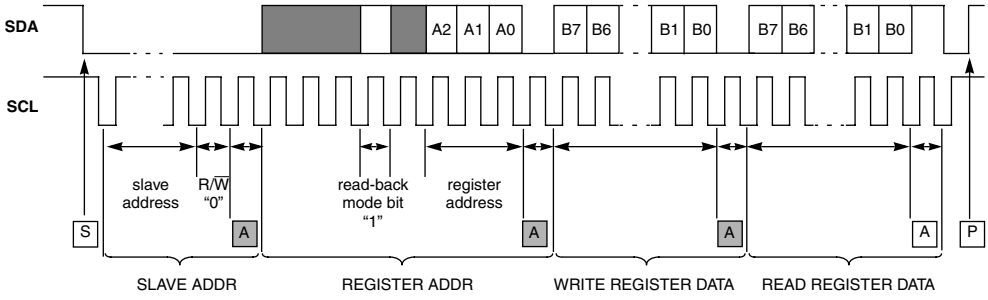
I²C Interface Write Timing



I²C Interface Read Timing : Normal Mode



I²C Interface Read Timing : Readback Mode



ML7041 Slave address "0011010"

S	START condition	A	Acknowledge (ML704 drive SDA to "0")
P	STOP condition	A	Not Acknowledge
Sr	Repeated START condition		Don't care ("0" or "1")

Figure 3. I²C Interface Timing

Register Map

Name	Address			Control and Detect Data								RW
	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	A/μ SEL	SPOUT PON	PDN ALL	PDN TX	PDN RX	SLP	SLP SEL	LNR	R/W
CR1	0	0	1	MIC SEL1	MIC SEL0	SP SEL1	SP SEL0	SHORT FRAME	—	SW C/A	RX PAD	R/W
CR2	0	1	0	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	1	1	Side Tone	Side Tone	Side Tone	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0	R/W
CR4	1	0	0	DTMF/ OTHERS SEL	TONE SEND	—	TONE4	TONE3	TONE 2	TONE1	TONE0	R/W
CR5	1	0	1	GP1 SEL CR/TONE	—	RG2PDN	RG1PDN	GP4C	GP3C	GP2C	GP1C	R/W
CR6	1	1	0	VOX ON/OFF	ON LVL1	—	—	—	—	—	—	R/W
CR7	1	1	1	VOX OUT	TX NOISE1	TX NOISE0	—	—	—	—	—	R

R/W : Read/Write enable R : Read-only register

FUNCTIONAL DESCRIPTION

Control Registers

CR0 (Basic operating mode 1)

Note: Initial Value: Reset state by /PDN

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	A/μ SEL	SPOUT PON	PDN ALL	PDN TX	PDN RX	SLP	SLP SEL	LNR
Initial value	0	0	0	0	0	0	0	0

B7 PCM Companding law select
0 = μ-law, 1 = A-law

B6 Power on control for output amps (SPOUT+, SPOUT-)
0 = Power down
1 = Power on

B5 Power down (entire system)
0 = Power on
1 = Power down
When using this data for power down control, set $\overline{\text{PDN}}$ pin to “1” level.
The control registers are not reset by this signal.

B4 Power down (Transmit only)
0 = Power on
1 = Power down

B3 Power down (Receive only)
0 = Power on
1 = Power down

B2 Slope Filter enable
0 = Slope Filter disable
1 = Slope Filter enable

B1 The type of Slope Filter select (refer to Figure “Frequency Response of Slope Filter” on page 15)
0 = CASE1
1 = CASE2

B0 PCM interface linear code select
0 = Companding law selected by CR0-B7
1 = 14-bit Linear code (2’s complement) regardless of setting of CR0-B7

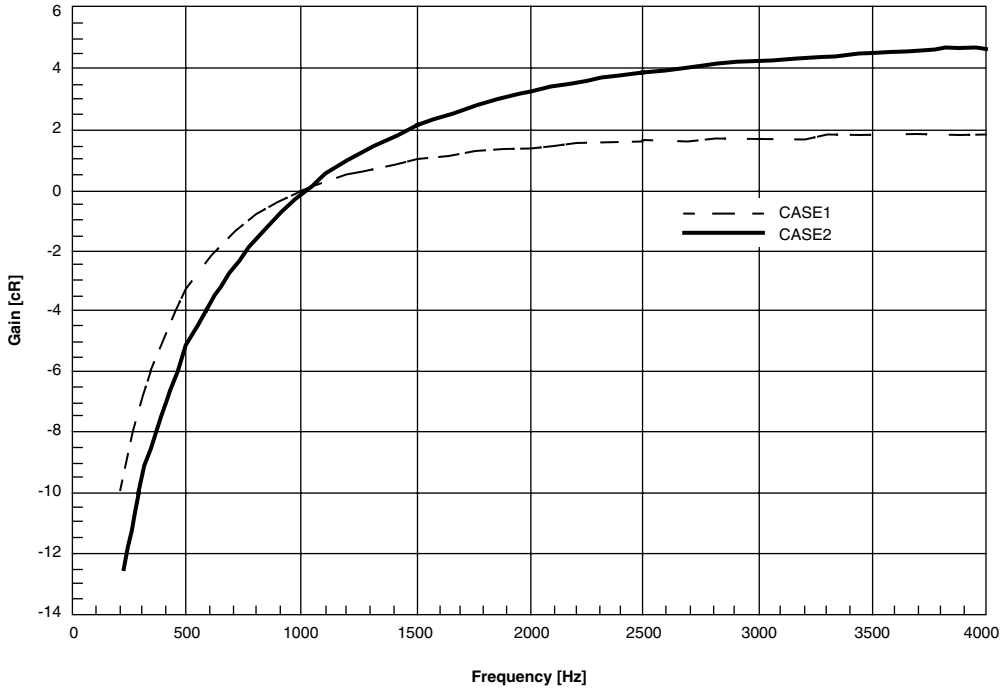


Figure 4. Frequency Response of Slope Filter

CR1 (Basic operating mode 2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	MIC SEL1	MICSEL0	SPSEL1	SPSEL0	SHORT FRAME	—	SW C/A	RX PAD
Initial Value	0	0	0	0	0	0	0	0

B7, B6 Selection of input amplifier to encoder.

B7	B6	
0	0	MIC1
0	1	MIC2
1	0	MIC3
1	1	no input

B5, B4 Selection of output amplifier

B5	B4	
0	0	EXTO
0	1	EAR1O
1	0	EAR2O
1	1	no-output

B3 Short Frame Synchronous interface select
0 = Long Frame Synchronous interface
1 = Short Frame Synchronous interface

B2 Not used

B1 Analog switch control
0 = SWB to SWA Closed: the SWC pin is high impedance
1 = SWB to SWC Closed: the SWA pin is high impedance.

B0 Receive side PAD
0 = no PAD
1 = inserted, 12 dB loss

CR2 (PCM CODEC operating mode setting and transmit/receive gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0
Initial Value	0	0	1	1	0	0	1	1

B7 PCM Coder disable
0 = Enable
1 = Disable (transmit PCM idle pattern)

B6, B5, B4 Transmit gain adjustment, refer to table below.

B3 PCM Decoder disable
0 = Enable
1 = Disable (receive PCM idle pattern)

B2, B1, B0 Receive gain adjustment, refer to table below.

B6	B5	B4	Transmit Gain	B2	B1	B0	Receive Gain
0	0	0	-6 dB	0	0	0	-12 dB
0	0	1	-4 dB	0	0	1	-9 dB
0	1	0	-2 dB	0	1	0	-6 dB
0	1	1	0 dB	0	1	1	-3 dB
1	0	0	+2 dB	1	0	0	0 dB
1	0	1	+4 dB	1	0	1	+3 dB
1	1	0	+6 dB	1	1	0	+6 dB
1	1	1	+8 dB	1	1	1	+9 dB

This programmable gain table is not only for transmit/receive voice signal and the transmitted DTMF and other tones. The transmission of these tone signals is enabled by the CR4-B6 data described later. The original (reference) signal amplitude of these tones is analogically defined as follows.

DTMF low-group-tones	-16 dBm0
DTMF high-group-tones and others	-14 dBm0

For example, when selecting +8 dB (B6, B5, B4) = (1, 1, 1) as a transmit gain, each tone signal amplitude with an analogical expression on the pin PCMOUT becomes as follows:

DTMF low-group tones	- 8 dBm0
DTMF high-group tones and other tones	- 6 dBm0

Gain setting for the side tone (path to receive side from transmit side) and the receive side tone is performed by register CR3.

CR3 (Side tone and other tone generator gain setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Side, tone GAIN2	Side, tone GAIN1	Side, tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5 Side tone path gain setting, refer to table below.

B7	B6	B5	Side Tone Path Gain
0	0	0	OFF
0	0	1	-15 dB
0	1	0	-13 dB
0	1	1	-11 dB
1	0	0	-9 dB
1	0	1	-7 dB
1	1	0	-5 dB
1	1	1	-3 dB

B4 Tone generator enable
0 = Disable
1 = Enable

B3, B2, B1, B0 Tone generator gain adjustment for receive side, refer to table below:

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0	0	0	0	OFF	1	0	0	0	-20 dB
0	0	0	1	-34 dB	1	0	0	1	-18 dB
0	0	1	0	-32 dB	1	0	1	0	-16 dB
0	0	1	1	-30 dB	1	0	1	1	-14 dB
0	1	0	0	-28 dB	1	1	0	0	-12 dB
0	1	0	1	-26 dB	1	1	0	1	-10 dB
0	1	1	0	-24 dB	1	1	1	0	-8 dB
0	1	1	1	-22 dB	1	1	1	1	-6 dB

The tone generator gain setting table for the receive side, as shown in the table above, depends upon the following reference level.

DTMF low-group tones	+4 dBm0
DTMF high-group tones and others	+6 dBm0

For example, when selecting - 6 dB (B3, B2, B1, B0) = (1, 1, 1, 1) as a tone generator gain, each DTMF tone signal amplitude on EXTO or EAR1O or EAR2O is as follows.

DTMF low-group tone	- 2 dBm0
DTMF high-group tone or other tones	0 dBm0

CR4 (Tone generator operating mode and frequency select)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	DTMF/ Others SEL	TONE SEND	—	TONE4	TONE3	TONE2	TONE1	TONE0
Initial Value	0	0	0	0	0	0	0	0

B7 DTMF or other tones select
0 = Others
1 = DTMF

B6 Tone transmit enable (Transmit side)
0 = Voice signal (transmit)
1 = Tone transmit

B5 Not used

B4, B3, B2, B1, B0 ... Tone frequency setting, refer to tables below.

Tone Frequency Setting for B7 = 1 (DTMF tone)

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
*	0	0	0	0	697 Hz + 1209 Hz	*	1	0	0	0	852 Hz + 1209 Hz
*	0	0	0	1	697 Hz + 1336 Hz	*	1	0	0	1	852 Hz + 1336 Hz
*	0	0	1	0	697 Hz + 1477 Hz	*	1	0	1	0	852 Hz + 1477 Hz
*	0	0	1	1	697 Hz + 1633 Hz	*	1	0	1	1	852 Hz + 1633 Hz
*	0	1	0	0	770 Hz + 1209 Hz	*	1	0	0	0	941 Hz + 1209 Hz
*	0	1	0	1	770 Hz + 1336 Hz	*	1	1	0	1	941 Hz + 1336 Hz
*	0	1	1	0	770 Hz + 1477 Hz	*	1	1	1	0	941 Hz + 1477 Hz
*	0	1	1	1	770 Hz + 1633 Hz	*	1	1	1	1	941 Hz + 1633 Hz

*Unrelated

Tone Frequency Setting for B7 = 0 (Other tones)

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	0	0	0	2730 Hz / 2500 Hz 8 Hz wamb.	1	0	0	0	0	1200 Hz
0	0	0	0	1	2000 Hz / 2667 Hz 8 Hz wamb.	1	0	0	0	1	1300 Hz
0	0	0	1	0	1000 Hz /1 333 Hz 8 Hz wamb.	1	0	0	1	0	
0	0	0	1	1		1	0	0	1	1	1477 Hz
0	0	1	0	0		1	0	1	0	0	1633 Hz
0	0	1	0	1		1	0	1	0	1	2000 Hz

Tone Frequency Setting for B7 = 0 (Other tones) (Continued)

B4	B3	B2	B1	B0	Frequency	B4	B3	B2	B1	B0	Frequency
0	0	1	1	0		1	0	1	1	0	2100 Hz
0	0	1	1	1		1	0	1	1	1	
0	1	0	0	0		1	1	0	0	0	2400 Hz
0	1	0	0	1	400 Hz	1	1	0	0	1	
0	1	0	1	0	440 Hz	1	1	0	1	0	2500 Hz
0	1	0	1	1	480 Hz	1	1	0	1	1	
0	1	1	0	0		1	1	1	0	0	
0	1	1	0	1	667 Hz	1	1	1	0	1	2700 Hz
0	1	1	1	0	800 Hz	1	1	1	1	0	
0	1	1	1	1	1000 Hz	1	1	1	1	1	3000 Hz

CR5 (Regulator control, General purpose driver control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	GP1 SEL CR/TONE	–	RG2PDN	RG1PDN	GP4C	GP3C	GP2C	GP1C
Initial Value	0	0	0	0	0	0	0	0

B7 Selection of how to control General purpose driver 1
0 = Control register CR5-B0
1 = A sign bit of the receiver

B6 Not used

B5, B4 Power down control for Regulator 2 or Regulator 1
0 = Power down
1 = Power on
When using this data, set pin RG2PDN or RG1PDN at “0” level.

B3, B2, B1, B0 General purpose driver control
0 = off (High impedance)
1 = on (Low output)

CR6 (VOX function control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	VOX ON/OFF	ON LVL1	—	—	—	—	—	—
Initial Value	0	0	*	0	0	0	0	0

B7 VOX function enable
0 = Disable
1 = Enable

B6 Voice detector level setting
0 = -26 dBmO
1 = -38 dBmO

B5 Reserved

B4, B3, B2, B1, B0 Not used

CR7 (Detect register, read only)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	VOX OUT	TX Noise Level1	TX Noise Level0	—	—	—	—	—
Initial Value	0	0	0	*	*	*	*	*

*For IC test

B7 Voice detection
0 = Silence
1 = Voice detect

B6, B5 Voice detect level (indicator)

B6	B5	
0	0	Below -50 dBmO
0	1	-40 to -50 dBmO
1	0	-30 to -40 dBmO
1	1	Above -30 dBmO

Note: These outputs are enabled when the VOX function is turned ON by CR6-B7.

B4, B3, B2, B1, B0 Not used

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating			Unit
Power Supply Voltage	V_{DD}	—	-0.3	to	+4.6	V
Analog Input Voltage	V_{AIN}	—	-0.3	to	V_{DD}+0.3	V
Digital Input Voltage	V_{DIN}	—	-0.3	to	V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	-55	to	+150	˚C
Operating Junction Temperature (Peak) [1]	Tjmax	—	-40	to	+150	˚C
Operating Junction Temperature (Average) [1]	Tjmaxa	—	-40	to	+105	˚C

1. Tjmax = $P \times \theta ja + Ta$

   P : Power (W)

   θja : the junction to ambient thermal resistance

   Ta : the ambient temperature

   48 pin TQFP θja = 195˚C (no-mount, no-flow)

   θja = 156˚C (typical PCB mounting, no-flow)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	—	+2.4	—	+3.3	V
Operating Temperature	Ta	—	-40	+25	+85	˚C
Input High Voltage	VIH	To all digital input pins	0.7 x V_{DD}	—	V_{DD}	V
Input Low Voltage	VIL	To all digital input pins	0	—	0.20 x V_{DD}	V
Digital Input Rise Time	t_{ir}	To all digital input pins	—	—	50	ns
Digital Input Fall Time	t_{if}	To all digital input pins	—	—	50	ns
Digital Output Load	CDL	To all digital output pins	—	—	100	pF
Bypass Capacitor for SG	CSG	Between SG and AG	0.1	—	—	µF
Master Clock Frequency	FMCK	MCK	0.01%	2.048	0.01%	MHz
Bit Clock Frequency	FBCK1	BCLK (A/µ-law)	64	—	2048	kHz
	FBCK2	BCLK (Linear)	128	—	2048	kHz
Synchronous Signal Frequency	FSYNC	SYNC	—	8.0	—	kHz
Clock Duty Ratio	DCLK	MCK, BCLK, EXCK	40	50	60	%
Sync Pulse Setting Time	tXR	BCLK <=> SYNC	100	—	—	ns
Synchronous Signal Width	tWS	SYNC	1 BCLK	—	100	µs

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD} = 2.4 V to 3.3 V, Ta = -40˚C to +85˚C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Current	I_{DD1}	Operation Mode No Signal (V_{DD}=3.0 V)	0	5.0	11.0	mA
	I_{DD2}	Operation Mode No Signal (V_{DD}=3.0 V) SPO+, SPO- or EAR1, 2 is active	0	12.0	25.0	mA
	I_{DD3}	Power Down Mode (V_{DD}=3.0 V, Ta=25˚C)	0	1.0	10	µA
Input Leakage Voltage	I_{IH}	V_I=V_{DD}	—	—	2.0	µA
	I_{IL}	V_I=0 V	—	—	1.5	µA
Output High Voltage	V_{OH}	I_{OH}=0.4 mA	0.5x V_{DD}	—	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL}=-1.2 mA	0	0.2	0.4	V
Input Capacitance	C_{IN}	—	—	5	—	pF

Analog Interface Characteristics (V_{DD} = 2.4 V to 3.3 V, Ta = -40˚C to +85˚C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Resistance Load	R_{INX}	MIC1O, MIC2O, MIC3O, EXTO	10	—	—	MΩ
Output Load Resistance	R_{LGX1}	MIC1O, MIC2O, MIC3O, EXTO	20	—	—	KΩ
	R_{LGX2}	EAR1O, EAR2O	32	—	—	W
	R_{LGX3}	SPO+, SPO- Differential	8	—	—	W
Output Load Capacitance	C_{LGX}	Analog output pins	—	—	100	pF
Output Amplitude	V_{O1}	MIC1O, MIC2O, MIC3O, EXTO RL=20 kΩ EAR1O, EAR2O RL= 32 Ω Note [1]	—	—	±1.3	VPP
	V_{O2}	SPO+, SPO- Differential Output V_{DD}=3.0 V RL= 8 Ω	—	—	2.6	VPP
Total Harmonic Distortion	THD	EAR1O, EAR2O, SPO+, SPO-V_{DD}=3.0 V	—	—	5.0	%
Input Offset Voltage	V_{OFGX1}	MIC1O, MIC2O, MIC3O, EXTO	-20	—	20	mV
	V_{OFGX2}	EAR1O, EAR2O, SPO+, SPO-	-100	—	100	mV
SG Output Voltage	VSG	SG	—	1.4	—	V
SG Output Impedance	RSG	SG	—	40	80	KΩ
Internal switch ON Impedance	Rsw	All Internal switches (DC bias 1.4 V)	—	—	300	W

1. -7.7 dBm (600 Ω) = 0 dBm0, + 3.17 dBm0 = 1.3 VPP

AC Characteristics (V_{DD} = 2.4 V to 3.3 V, Ta = -40˚+85˚C)

Parameter	Symbol	Condition			Min	Typ	Max	Unit
		Frequency (Hz)	Level (dBmO)	Others				
Tx Freq Response	L_{OSS} T1	0 to 60	0	-	25	—	—	dB
	L_{OSS} T2	300 to 3000			-0.15	—	0.20	dB
	L_{OSS} T3	1020			Reference			dB
	L_{OSS} T4	3300			-0.15	—	0.80	dB
	L_{OSS} T5	3400			0	—	0.80	dB
	L_{OSS} R6	3968.75			13	—	—	dB
Rx Freq Response	L_{OSS} R1	0 to 3000	0	—	-0.15	—	0.80	dB
	L_{OSS} R2	1020			Reference			dB
	L_{OSS} R3	3300			-0.15	—	0.80	dB
	L_{OSS} R4	3400			0	—	0.80	dB
	L_{OSS} R5	3968.75			13	—	—	dB
Tx Signal to Distortion Ratio	SD T1	1020	3	Note [1]	35	—	—	dB
	SD T2		0		35	—	—	dB
	SD T3		-30		35	—	—	dB
	SD T4		-40		28	—	—	dB
	SD T5		-45		23	—	—	dB
Tx Signal to Distortion Ratio	SD T1	1020	3	Note [1]	35	—	—	dB
	SD T2		0		35	—	—	dB
	SD T3		-30		35	—	—	dB
	SD T4		-40		28	—	—	dB
	SD T5		-45		23	—	—	dB
Rx Signal to Distortion Ratio	SD R1	1020	3	Note [1]	35	—	—	dB
	SD R2		0		35	—	—	dB
	SD R3		-30		35	—	—	dB
	SD R4		-40		28	—	—	dB
	SD R5		-45		23	—	—	dB
Tx Gain Tracking	GT T1	1020	3	—	-0.2	—	0.2	dB
	GT T2		-10		Reference			dB
	GT T3		-40		-0.2	—	0.2	dB
	GT T4		-50		-0.6	—	0.6	dB
	GT T5		-55		-1.2	—	1.2	dB
Rx Gain Tracking	GT R1	1020	3	—	-0.2	—	0.2	dB
	GT R2		-10		Reference			dB
	GT R3		-40		-0.2	—	0.2	dB
	GT R4		-50		-0.6	—	0.6	dB
	GT R5		-55		-1.2	—	1.2	dB

1. Use the P-message weighted filter.

AC Characteristics (Continued)

Parameter	Symbol	Condition			Min	Typ	Max	Unit
		Freq. (Hz)	Level (dBmO)	Others				
I^2C Interface timing	f_{SCL}	—	CL = 50 pF	See Figure 6 on page 27	0	—	100	kHz
	t_{BUF}				4.7	—	—	µs
	t_{HDSTA}				4.0	—	—	µs
	t_{LOW}				4.7	—	—	µs
	t_{HIGH}				4.0	—	—	µs
	t_{SUSTA}				4.7	—	—	µs
	t_{HDDAT}				0	—	—	µs
	t_{SUDAT}				250	—	—	ns
Idle Channel Noise	N_{IDLT}	—	MIC1I, MIC2I, MIC3I = SG	Note [1]	—	—	-68	dBmOp
	N_{IDLR}	—	—	Notes [1] and [2]	—	—	-72	
Absolute Signal Amplitude	A_{VT}	1020	0	MIC1O, MIC2O, MIC3O	0.285	0.320 Note [3]	0.359	Vrms
	A_{VR}			EXTO	0.285	0.320 Note [3]	0.359	Vrms
Power Supply Noise Rejection Ratio	P_{SRRT}	Noise Freq:	Noise Level:	—	30	—	—	dB
	P_{SRRR}	0 to 50 kHz	50 mVpp		30	—	—	dB
Digital Input/Output Timing PCM Interface	t_{SDX} t_{SDR}	—	1 LSTTL + 100 pF	See Figure 5 on page 26	0	—	200	ns
	t_{XD1} t_{RD1}				0	—	200	ns
	t_{XD2} t_{RD2}				0	—	200	ns
	t_{XD3} t_{RD3}				0	—	200	ns

1. Use the P-message weighted filter
2. PCMIN input code
   "11010101"(A-law)
   "11111111"(u-law)
3. 0.320 Vrms = 0 dBmO = -7.7 dBm

AC Characteristics (DTMF and Other Tones) (V_{DD} = 2.4 V to 3.3 V, Ta = -40˚C to +85˚C)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Frequency Difference	D_{FT}	DTMF Tones, Other Tones		-1.5	—	+1.5	%
Original (reference) Tones Signal Level [1]	V_{TL}	Transmit Tones (Gain setting 0 dB)	DTMF (Low) and Other Tones	-18	-16	-14	dBmO
	V_{TH}		DTMF (High)	-16	-14	-12	dBmO
	V_{RL}	Receive Tones (Gain setting -6 dB)	DTMF (Low)	-4	-2	0	dBmO
	V_{RH}		DTMF (High) and Other Tones	-2	0	+2	dBmO
Relative Level of DTMF Tones	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		+1	+2	+3	dB

1. Does not contain the setting value set for the programmable gain.

AC Characteristics (Programmable Gain Stages) (V_{DD} = 2.4 V to 3.3 V, Ta = -40˚C to +85˚C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Gain Accuracy	D_G	All gain stages, to programmed value	-1	0	+1	dB

AC Characteristics (Voice Detect Function) (V_{DD} = 2.4 V to 3.3 V, Ta = -40˚C to +85˚C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voice Detection Time	TVON	Silence>Voice	—	5	—	ms
	TVOF	(Voice/Silence differential:10 dB)	140	160	180	ms
Voice Detection Accuracy	DVX	For detection level set values by CR6-B6, B5	-2.5	0	2.5	dB

AC Characteristics (General Purpose Drivers) (V_{DD} = 2.4 V to 3.3 V, Ta = -40˚C to +85˚C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage	V_O	I_{OUT}=150 mA, GP1 - GP4	—	—	0.7	V
Output Load Resistance	R_O		20	—	—	Ω

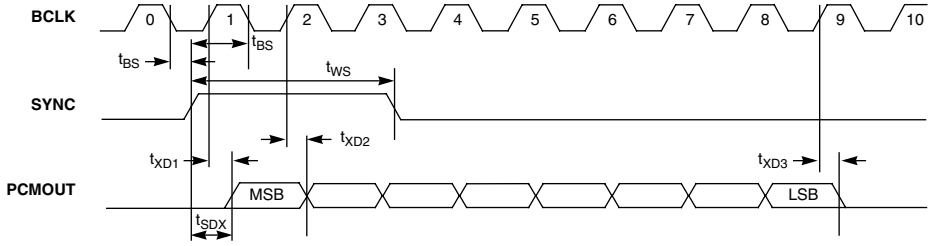
AC Characteristics (Regulator1, 2) (V_{DD} = 2.4 V to 3.3 V, Ta = -40˚C to +85˚C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage	Vi1	I_{OUT}=70 mA	3.1	3.6	4.1	V
	Vi2	I_{OUT}=150 mA	3.4	3.6	4.1	V
Output Voltage	V_O	RGIN=3.6 V	2.94	3.00	3.06	V
Load Current	Io	3.4 V<RGIN<4.1 V	—	—	150	mA
Dropout Voltage	V_{DROP}	I_{OUT}=150 mA, RGIN=3.6 V	—	—	200	mV
Output Voltage Line Regulation	dV_O/dV_I	I_{OUT}=70 mA 3.1 V < RGIN < 4.1 V	—	0.01	0.05	%/V
Standby Current	$I_{standby}$	RGPDN=0		0.1	10	µA

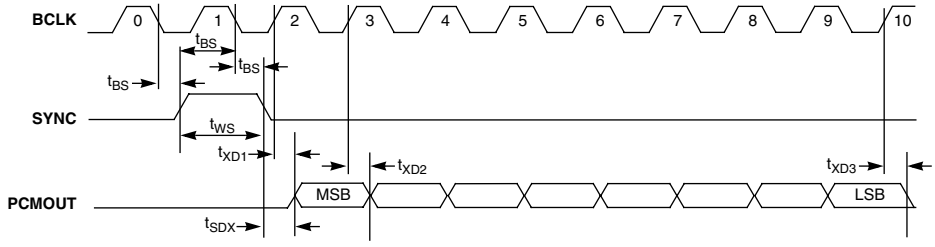
PCM INTERFACE TIMING DIAGRAMS

See also Figure 2 on page 11.

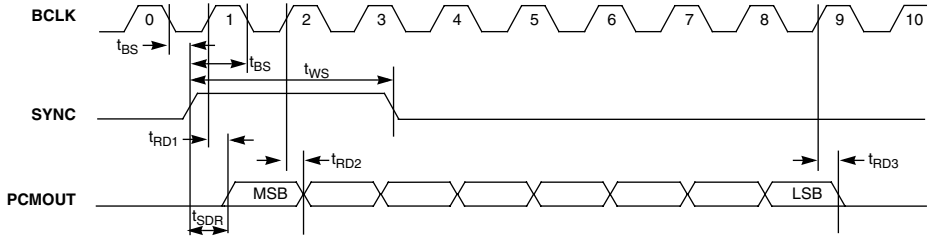
Transmit Side PCM Timing (Normal Synchronous Interface)



Transmit Side PCM Timing (Short Frame Synchronous Interface)



Receive Side PCM Timing (Normal Synchronous Interface)



Receive Side PCM Timing (Short Frame Synchronous Interface)

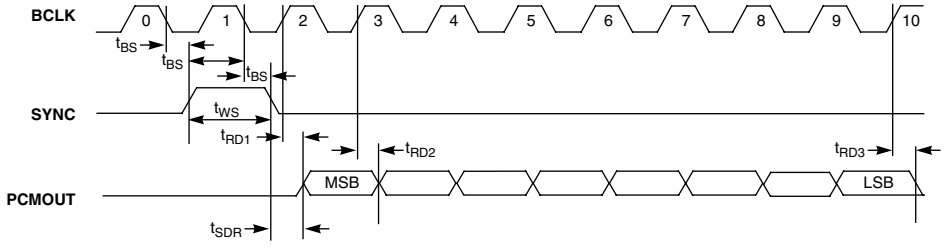


Figure 5. PCM Interface Timing

I²C INTERFACE TIMING DIAGRAM

See also Figure 3 on page 12.

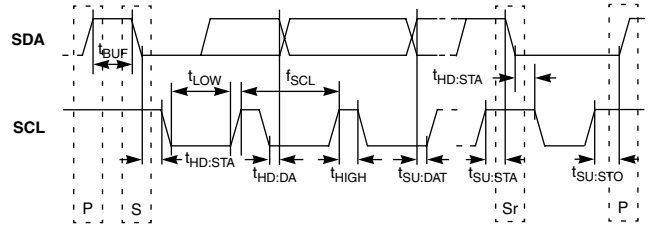
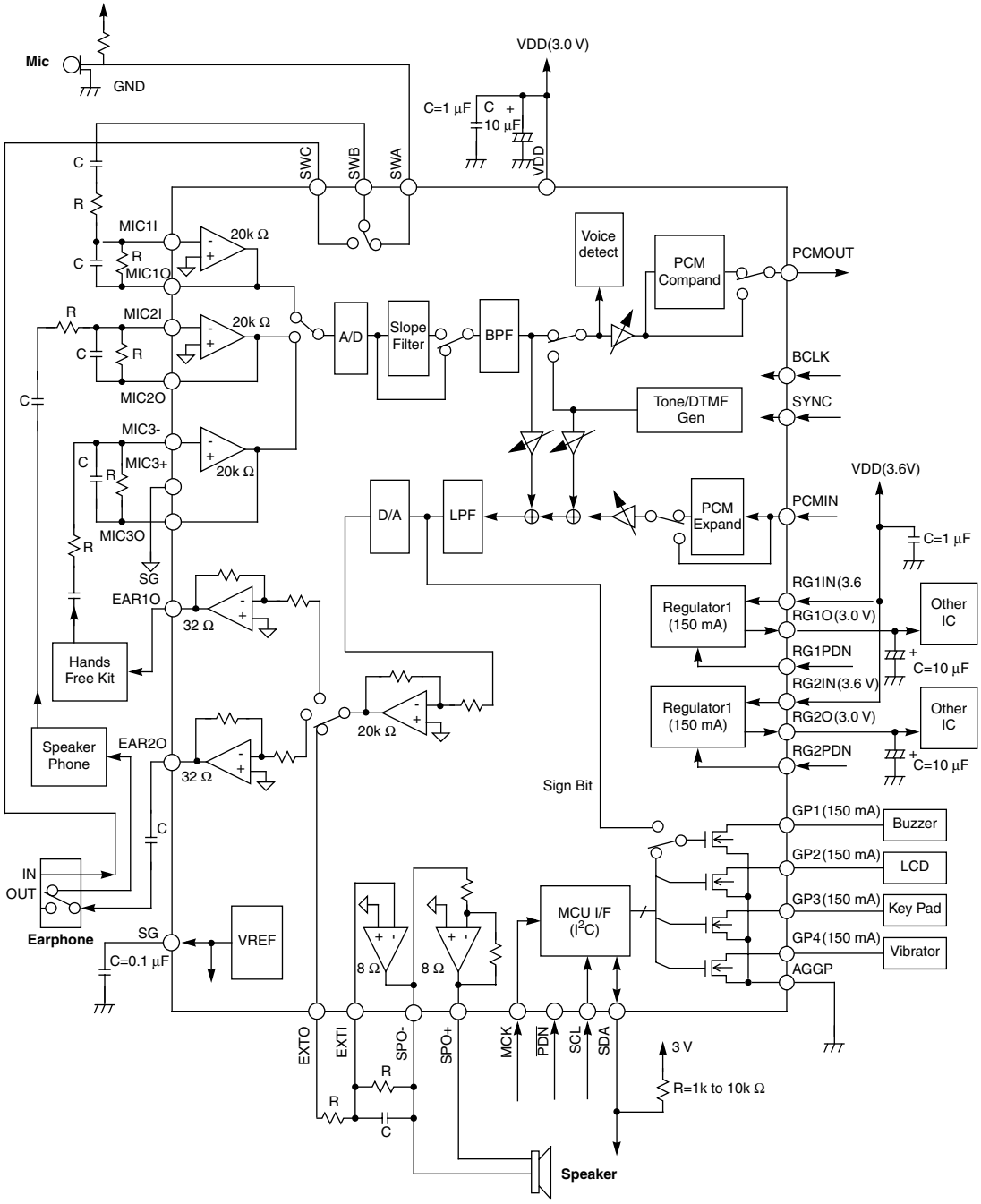


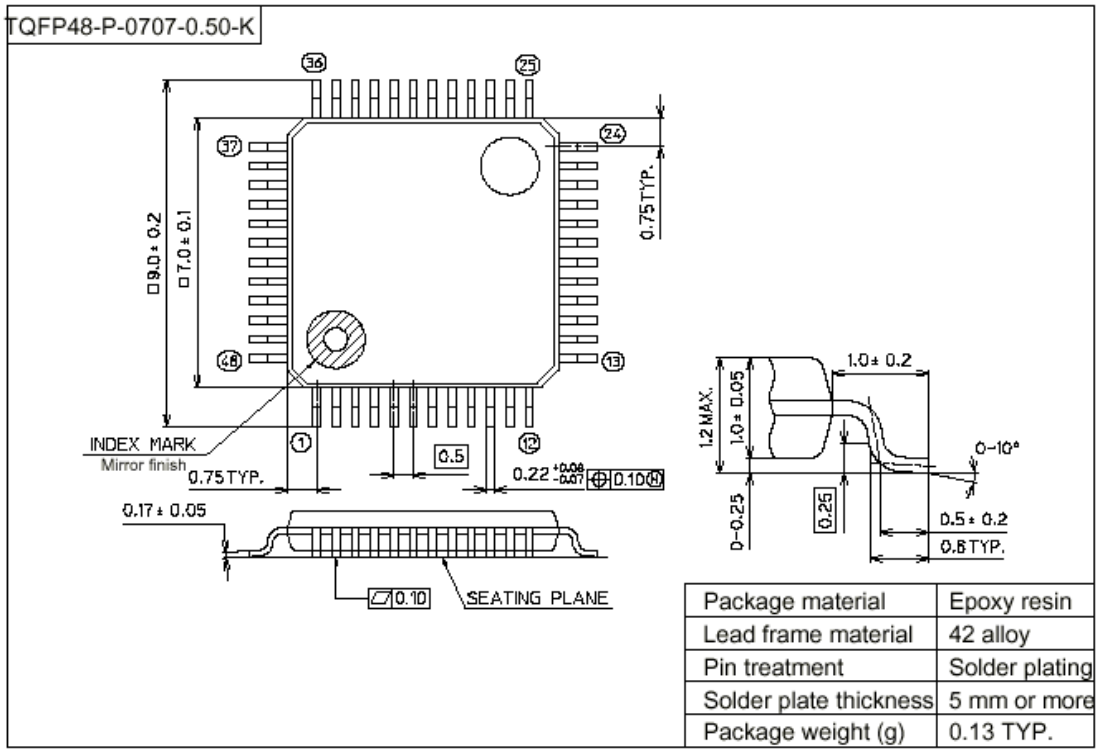
Figure 6. I²C Interface Timing

APPLICATION CIRCUITS



PACKAGE DIMENSIONS

(Units: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 mm or more
Package weight (g)	0.13 TYP.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

NOTES:

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Please make sure before using the product that the information you are referring to is up-to-date.

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