

DESCRIPTION

The 8262 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the 8262. (A logic HIGH on the INHIBIT input forces both outputs to a logic LOW).

When used as a Parity Generator, the 8262 supplies a parity bit which is transmitted together with the data word.

At the receiving end, the 8262 acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

PIN CONFIGURATION

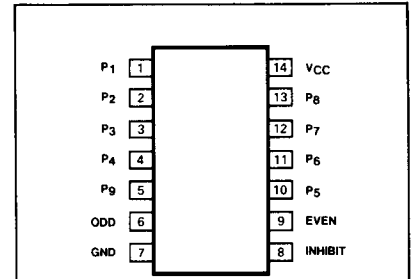


Figure A

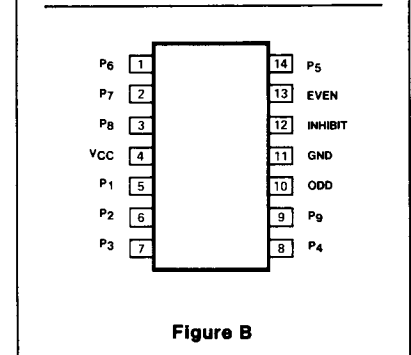
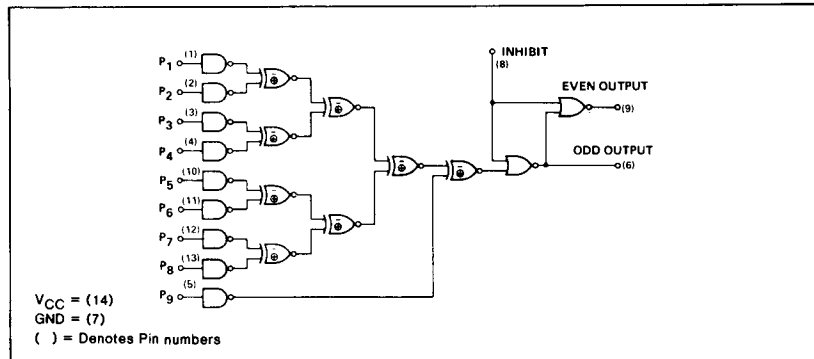


Figure B

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N8262N	• N82S62N	
Ceramic DIP	Fig. A	N8262F	• N82S62F	S8262F
Flatpak	Fig. B			S8262W

LOGIC DIAGRAM



LOGIC EQUATIONS

$$\text{Odd} = P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$$

$$\text{Even} = P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	8262		UNIT
		Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = Max, I _{OH} = -800μA	2.6		V
V _{OL} Output LOW voltage	V _{CC} = 4.75, I _{OL} = 16mA		0.40	V
I _{IH} Input HIGH current Data inputs Inhibit inputs	V _{CC} = Max, V _{IN} = 4.5V		80 160	μA μA
I _{IL} Input LOW current Data inputs Inhibit inputs	V _{CC} = Max, V _{IN} = 0.4V		-1.6 -3.2	mA mA
V _{BD} Voltage breakdown	V _{CC} = Max, I _{IN} = 10mA	5.5		V
I _{OS} Output short circuit-current	V _{CC} = Max, V _{OUT} = 0V	-20	-70	mA
I _{CC} Supply current	V _{CC} = Max		70	mA

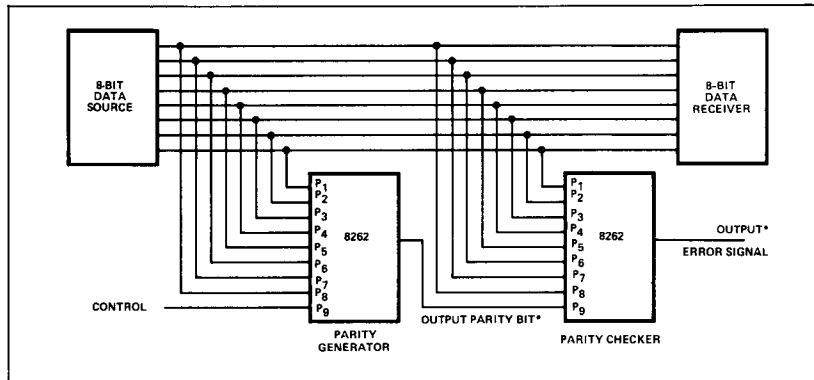
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	82S62		UNIT
		Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = - / mA	2.7		V
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 20mA		0.5	V
I _{IH} Input HIGH current	V _{CC} = Max, V _{IN} = 4.5V		10	μA
I _{IL} Input LOW current Data inputs P ₁ -P ₈ Data input P ₉ & Inhibit input	V _{CC} = Max, V _{IN} = 0.5V		-800 -1.2	μA mA
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-30	-100	mA

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8262		82S62		UNIT
		$C_L = 30\text{pF}$ $R_L = 84.5\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay P ₁ - P ₈ to even		50 55		23 23	ns ns
t _{PLH} t _{PHL}	Propagation delay P ₁ - P ₈ to odd		45 45		34 34	ns ns
t _{PLH} t _{PHL}	Propagation delay P ₉ to even		35 40		12 12	ns ns
t _{PLH} t _{PHL}	Propagation delay P ₉ to odd		30 35		18 18	ns ns
t _{PLH} t _{PHL}	Propagation delay inhibit to even		15 18		9 9	ns ns
t _{PLH} t _{PHL}	Propagation delay inhibit to odd		15 18		9 9	ns ns

TYPICAL APPLICATION



*Output can be conditioned for odd or even parity.
 An "even parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an even number.
 An "odd parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an odd number.

AC WAVEFORMS

