18-bit Data Bus Dynamic RAM Card

Connector Type

Two-piece 60-pin

MF11M1-978APXX
MF12M1-977BPXX
MF14M1-977BPXX
MF14M1-978APXX

DESCRIPTION

Mitsubishi's Dynamic RAM cards are based on the JEDEC standard for a 60pin DRAM card. (JC-42. 5-90-93. Item #273)
The DRAM cards provide large memory capacities on a device approximately the size of a credit card (54mm×85.6mm×3.4mm).
The cards use an 18-bit data bus. Available 1 MB, 2 MB, 4 MB capacities.

- Standard card size : 54mm (W) ×85.6mm (L) ×3.4mm (T)
- 60pin 2 piece connector type.
- $\overline{RAS}$ only refresh mode, $\overline{CAS}$ before $\overline{RAS}$ refresh mode and Page mode functions are available.

FEATURES

- Data bus width : 18bit (with parity)
- All inputs except $\overline{RAS}$ inputs are buffered.

APPLICATIONS

Main/expansion memory unit for Personal Computer. Laser-Printer, FAX.

PRODUCT LIST

PRODUCT No.	Item / Type Name	Memory Capacity	Data Bus Width (bits)	Access Time (t_{RAC})	Connector Type	Number of Pins	Outline Drawing
No. 1	MF11M1-978APXX	1 MB	18	80ns	Two-piece	60	60P-002
No. 2	MF12M1-977BPXX	2 MB		70ns			
No. 3	MF14M1-977BPXX	4 MB		70ns			
No. 4	MF14M1-978APXX	4 MB		80ns			

PIN ASSIGNMENT

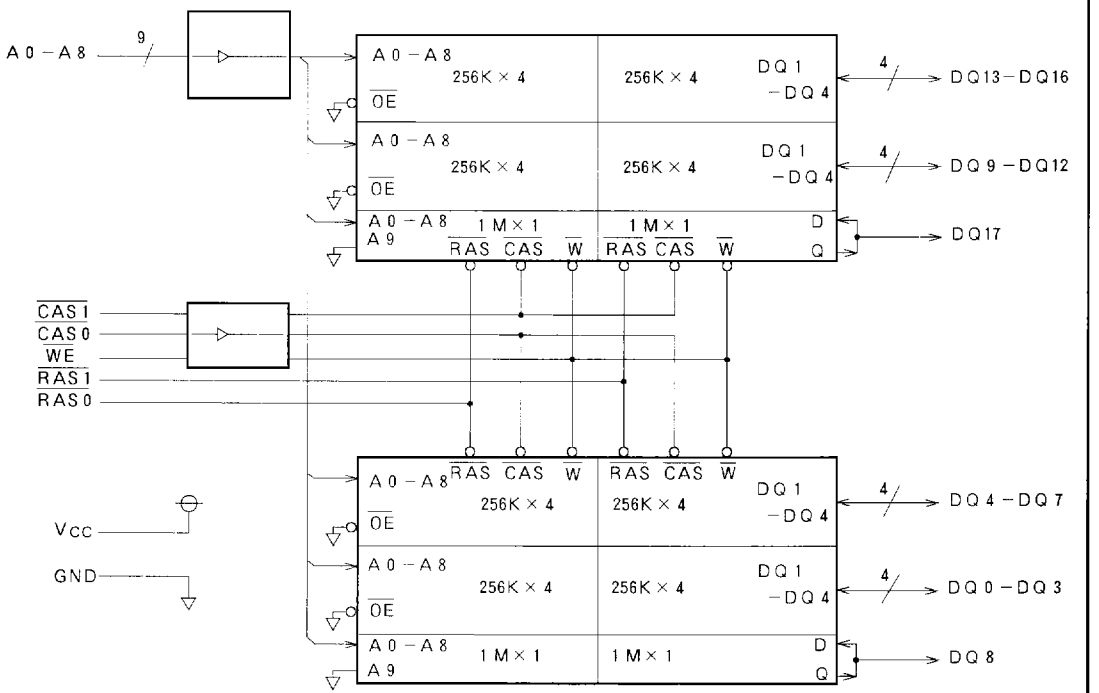
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	PD 6	Presence detect 6	2	PD 3	Presence detect 3
3	PD 1	Presence detect 1	4	PD 2	Presence detect 2
5	$\overline{WE}$	Write enable	6	Vcc	Power supply
7	NC	No connection	8	NC	No connection
9	GND	Ground	10	A 0	Address input
11	NC	No connection	12	NC	No connection
13	A 1	Address input	14	Vcc	Power supply
15	A 2		16	A 3	Address input
17	GND	Ground	18	A 4	
19	DQ 8	Data I/O	20	DQ17	Data I/O
21	DQ 0		22	Vcc	Power supply
23	DQ 1		24	DQ 9	Data I/O
25	GND	Ground	26	DQ10	
27	DQ 2	Data I/O	28	DQ11	
29	DQ 3		30	Vcc	Power supply
31	DQ 4		32	DQ12	Data I/O
33	GND	Ground	34	DQ13	
35	DQ 5	Data I/O	36	DQ14	
37	DQ 6		38	Vcc	Power supply
39	DQ 7		40	DQ15	Data I/O
41	GND	Ground	42	DQ16	
43	$\overline{CAS0}$	Column address strobe 0	44	A 5	Address input
45	A 6	Address input	46	Vcc	Power supply
47	A 7		48	A 8	Address input
49	GND	Ground	50	NC/A9	No connection/address input
51	$\overline{RAS0}$	Row address strobe 0	52	$\overline{RAS1}$/NC	Row address strobe 1/No connection
53	NC	No connection	54	NC	No connection
55	$\overline{CAS1}$	Columm address strobe 1	56	Vcc	Power supply
57	PD 5	Presence detect 5	58	PD 4	Presence detect 4
59	GND	Ground	60	NC	No connection

PinNo. / PRODUCT No.	50	52
No. 1	NC	$\overline{RAS1}$
No. 2	A 9	NC
No. 3, 4	A 9	$\overline{RAS1}$

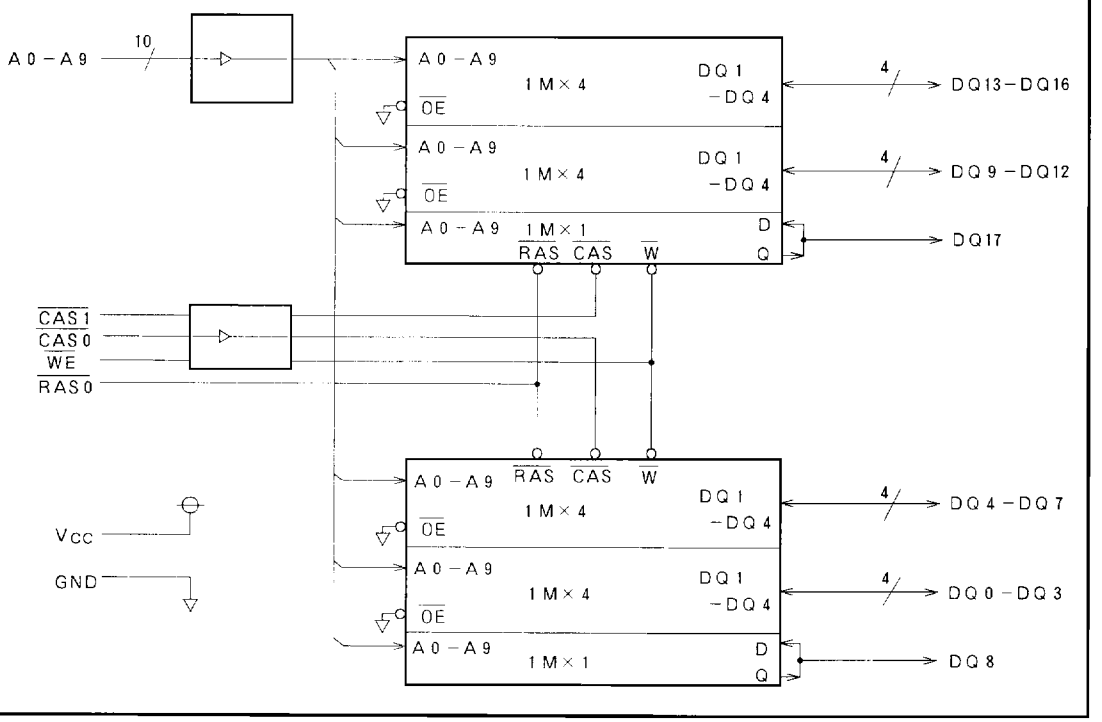
PD Pin Table

PRODUCT No.	PD 1	PD 2	PD 3	PD 4	PD 5	PD 6
No. 1	GND	NC	GND	GND	GND	GND
No. 2	GND	GND	GND	GND	NC	NC
No. 3	NC	GND	GND	GND	NC	NC
No. 4	NC	GND	GND	GND	GND	GND

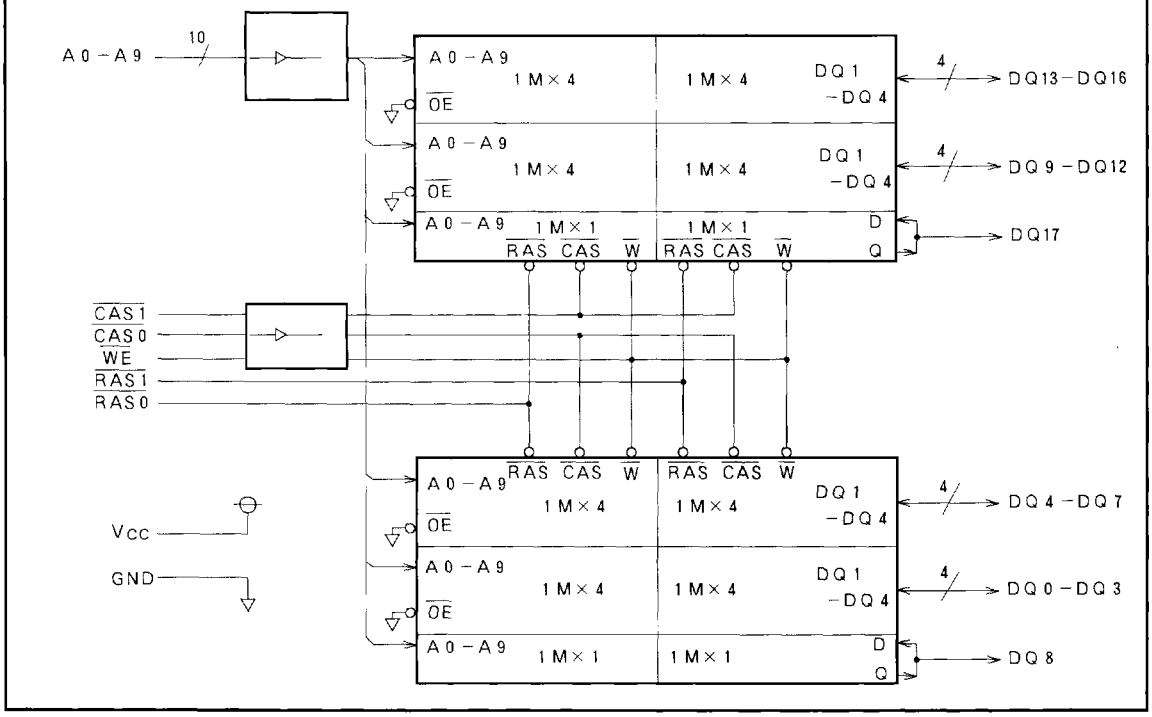
BLOCK DIAGRAM (No. 1)



BLOCK DIAGRAM (No. 2)



BLOCK DIAGRAM (No. 3, 4)



FUNCTION TABLE

Operation	input					input/output		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	input	output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Page mode indentical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note 1 : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open
Do not make more than one $\overline{RAS}$ signal active at the same time.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings		Unit
V_{CC}	Supply voltage	With respect to GND	−0.5 ~ 6		V
V_I	Input voltage		−0.5 ~ V_{CC} + 0.5		V
V_O	Output voltage		−0.5 ~ V_{CC} + 0.5		V
I_O	Output current		50		mA
P_d	Power dissipation	T_a = 25°C	No 1, 4	No 2, 3	W
			12	7.2	
T_{opr}	Operating temperature		0 ~ 50		°C
T_{stg}	Storage temperature		−40 ~ 80		°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 50℃, unless otherwise noted) : (Note 2)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
GND	Supply voltage	0	0	0	V
V_{IL}	Low input voltage	0		0.8	V
V_{IH}	High input voltage	0.7×V_{CC}		V_{CC}	V

Note 2 : With respect to GND

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 50℃, V_{CC} = 5 V ± 5 %, GND = 0 V) : (Note 3)

Symbol	Parameter	Test condition		Limits						Unit
				Min.		Typ	Max.			
				No.1, 3, 4	No. 2		No. 1	No. 2	No. 3	No. 4	
V_{OH}	High output voltage	I_{oh} = − 5 mA		2.4			V_{CC}				V
V_{OL}	Low output voltage	I_{ol} = 4.2mA		0			0.4				V
I_{OZ}	Off-stage output current	0 V ≦ V_{OUT} ≦ V_{CC}		−20	−10		20	10	20	20	μA
I_I	Input current	0 V ≦ V_{IN} ≦ V_{CC} Other input pins = 0 V	$\overline{RAS}$ inputs	−60			60				μA
			Other inputs	− 1			1				
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 4, 5)	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min, output open					432	600	692	572	mA
$I_{CC5(AV)}$	Supply current from Vcc, standby	$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.2V, other input pins ≧ V_{CC} − 0.2V or ≦ 0.2V, output open					13	3	5	13	mA
$I_{CC3(AV)}$	Average supply current from Vcc, refreshing (Note 4)	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min, output open					840	600	1240	1120	mA
$I_{CC4(AV)}$	Avetage supply current from Vcc, Page-Mode (Note 4, 5)	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{RC} = min, output open					372	540	632	1000	mA
$I_{CC6(AV)}$	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 4)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min, output open					840	600	1240	1120	mA

Note 3 : Current flowing into a CARD is positive, out is negative.

4 : $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Specified values are obtained at the fastest cycle rate.

5 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the outputs open.

SWITCHING CHARACTERISTICS (T_a = 0 ~ 50℃, V_{CC} = 5 V ± 5 %, GND = 0 V) : (Note 6)

Symbol	Parameter	Limits				Unit
		No. 1, No. 4		No. 2, No. 3		
		Min.	Max.	Min.	Max.	
t_{CAC}	Access time from $\overline{CAS}$ (Note 7, 8)		27		25	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 7, 9)		80		70	ns
t_{CAA}	Column Address access time (Note 7, 10)		47		42	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge		52		47	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note 11)	0	27	0	25	ns

Note 6 : An initial pause of 500 μsec is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 2 TTL loads and 100pF.

8 : Assume that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

9 : Assume that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$.

10 : Assume that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11 : $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($|I_{out}| \leqq 20\,\mu A$ (No. 2, $10\,\mu A$)) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (T_a = 0 ~ 50℃, V_{CC} = 5 V ± 5 %, GND = 0 V) : (Note 12, 13)

Symbol	Parameter	Limits					Unit
		No. 1, No. 4			No. 2, No. 3		
		Min.	Max.		Min.	Max.	
			No. 1	No. 4			
t_{REF}	Refresh cycle time		8	16		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	70			40		ns
t_{RCD}	Delay time. $\overline{RAS}$ low to $\overline{CAS}$ low (Note 14)	25	53		20	45	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low (Note 15)	17			17		ns
t_{CPN}	$\overline{CAS}$ high pulse width (Note 16)	10			10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note 17)	20	33		15	28	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	7			7		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note 18)	2	15		2	12	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	15			10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low or $\overline{WE}$ low	18			15		ns
t_T	Transition time (Note 19)	3	50		3	50	ns

Note 12 : The timing requirements are assumed t_T = 5 ns.

13 : $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14 : $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA}.

15 : t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.

16 : t_{CPN} is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)}$ except for tcp of page mode cycle.

17 : $t_{RAD(max)}$ is specified as reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is assumed by t_{CAA} for read cycle.

18 : $t_{ASC(max)}$ is specified as a reference point only of address access time.

19 : t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		No. 1, No. 4		No. 2, No. 3		
		Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	160		120		ns
t_{RAS}	$\overline{RAS}$ low pulse width	80	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	27	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	80		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	27		25		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	2		2		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	2		2		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	5		5		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	20		20		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	47		42		ns

Write Cycle (Early Write)

Symbol	Parameter	Limits				Unit
		No. 1, No. 4		No. 2, No. 3		
		Min.	Max.	Min.	Max.	
t_{WC}	Write cycle time	160		120		ns
t_{RAS}	$\overline{RAS}$ low pulse width	80	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	27	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	80		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	27		25		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	2		2		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	18		15		ns
t_{DS}	Data setup time	2		2		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	22		22		ns

Page Mode Cycle (Read, Early Write)

Symbol	Parameter	Limits						Unit
		No. 1		No. 4		No. 2, No. 3		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PC}	Read, Write cycle time	57		57		52		ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 20)	10	20	10	20	10	17	ns
t_{RAS}	$\overline{RAS}$ low pulse width	135	50000	135	100000	115	100000	ns

Note 20 : $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leqq t_{CP}$ access time is assumed by t_{CAC}.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 21)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	17		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	30		ns
t_{RPC}	$\overline{RAS}$ precharge $\overline{CAS}$ hold time	20		ns

Note 21 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

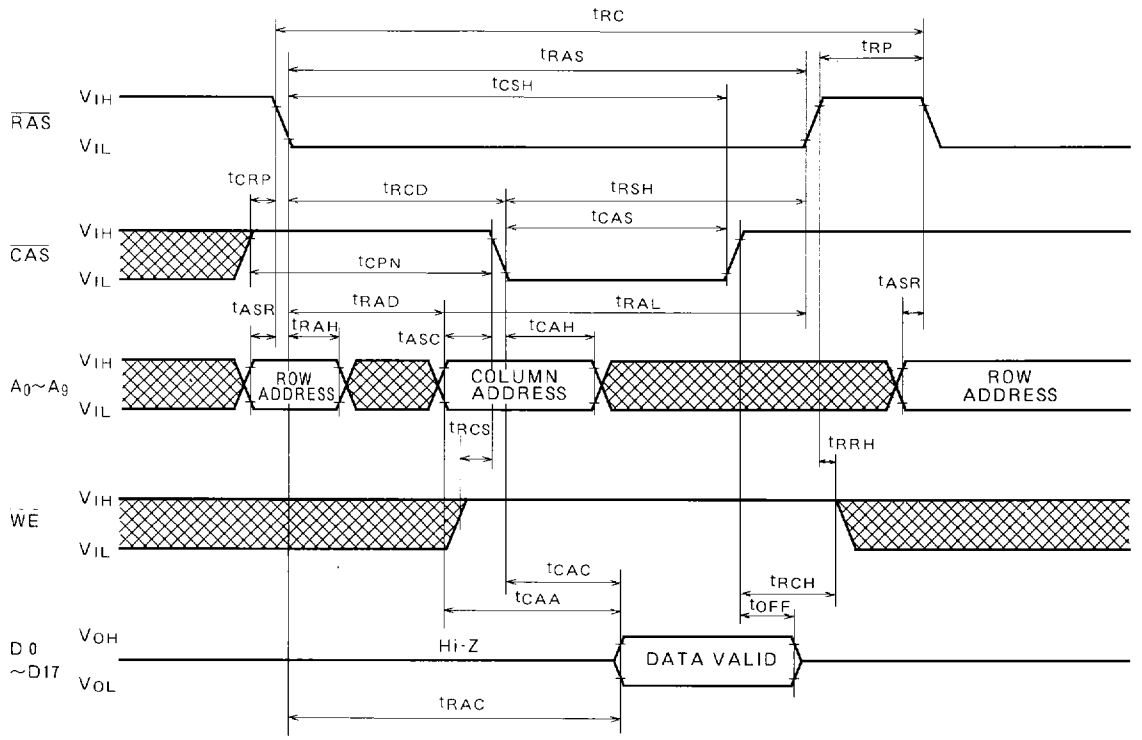
CAPACITANCE

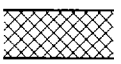
Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
C_I	Input capacitance	V_I = GND, V_i = 25mVrms, f = 1 MHz, T_a = 25°C	$\overline{RAS}$		60		pF
			Other inputs		20		
C_O	Output capacitance	V_O = GND, V_o = 25mVrms, f = 1 MHz, T_a = 25°C	DQ0-DQ17		45		pF

Note 22 : These items are not 100% tested.

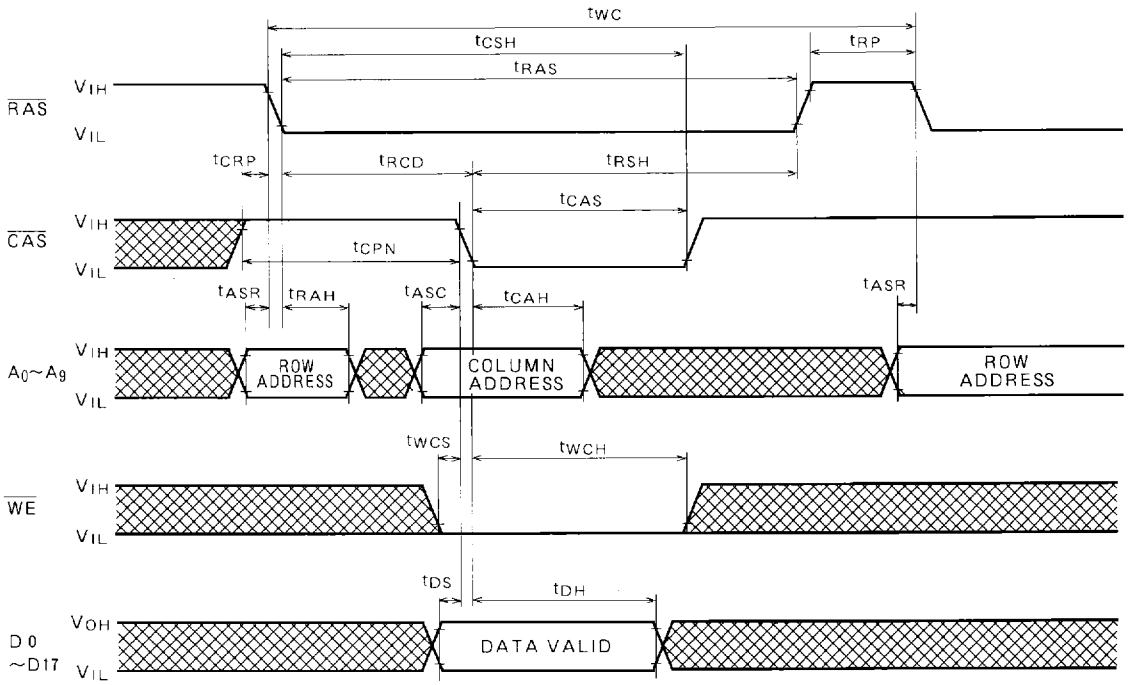
TIMING DIAGRAMS (Note 23)

Read Cycle

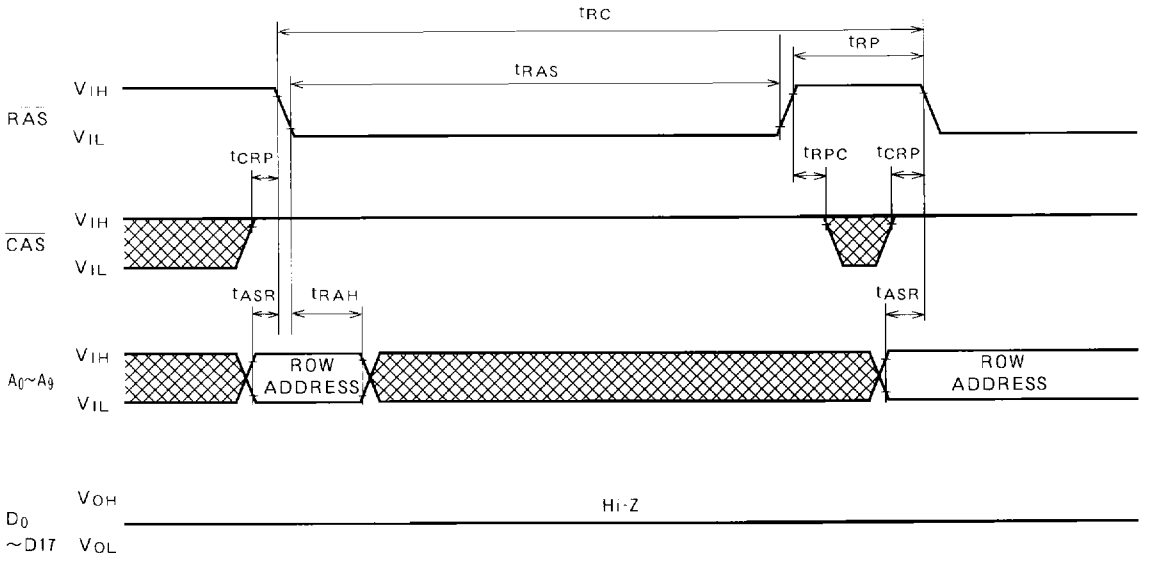


Note 23 :  Indicates the don't care input.

Early Write Cycle

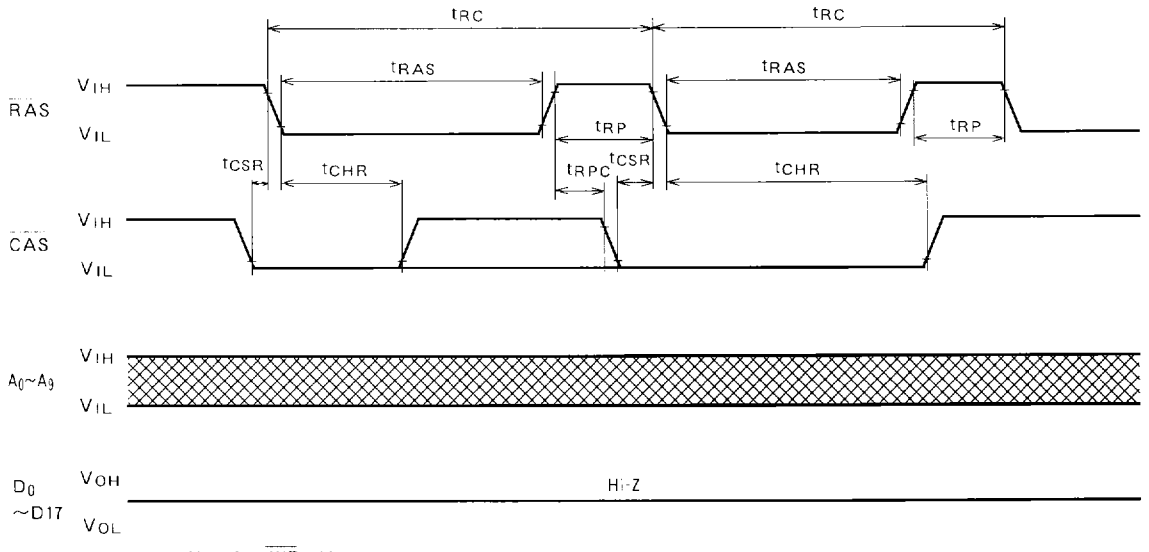


$\overline{RAS}$ only Refresh Cycle (Note 24)



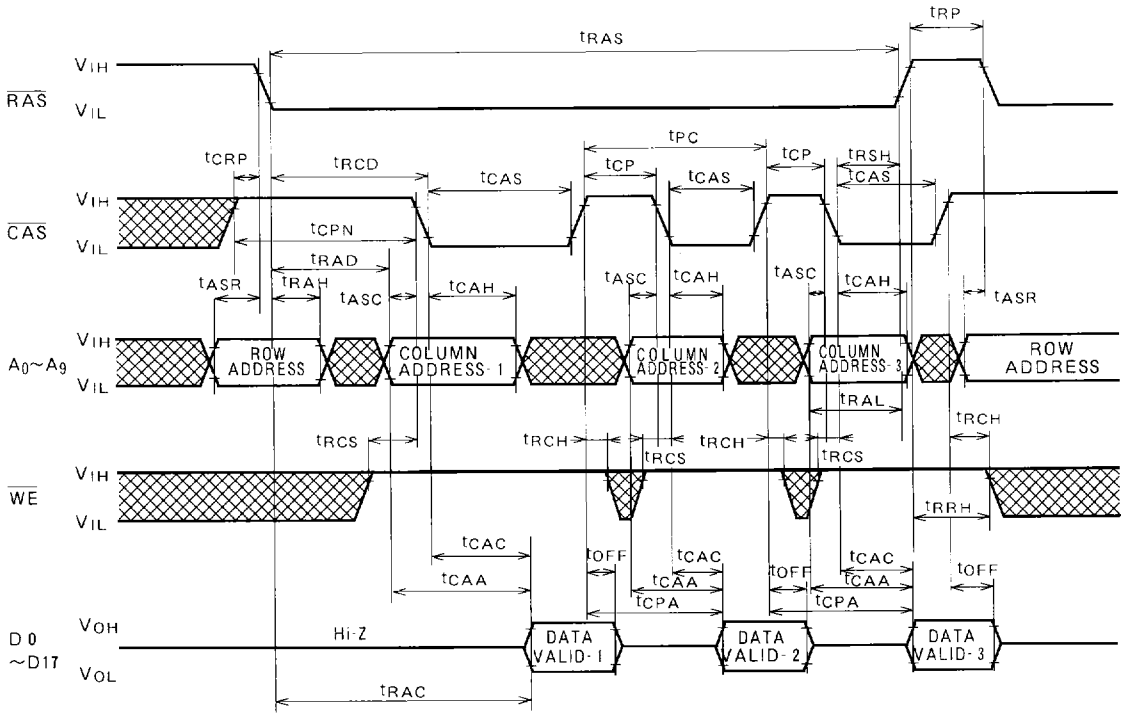
Note 24 : $\overline{WE}$ = don' t care.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 25)



Note 25 : $\overline{WE} = V_{IH}$

Page-Mode Read Cycle



Page-Mode Early Write Cycle