μA1391•μA1394

TV HORIZONTAL PROCESSOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA1391 is an integrated circuit which performs the low level horizontal processing functions in a television receiver. It includes a phase detector, an oscillator and a predriver. The μA1394 is electrically similar to the μA1391, except that it accepts a negative flyback input.

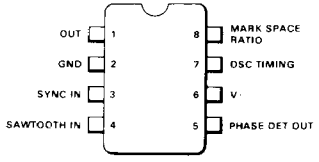
The device is constructed on a single silicon chip using the Fairchild Planar* epitaxial process.

- **INTERNAL SHUNT REGULATOR**
- **PRESET HOLD CONTROL CAPABILITY**
- **±300 Hz TYPICAL PULL-IN**
- **LINEAR BALANCED PHASE DETECTOR**
- **VARIABLE OUTPUT DUTY CYCLE FOR DRIVING A TUBE OR TRANSISTOR OUTPUT STAGE**
- **LOW THERMAL FREQUENCY DRIFT**
- **SMALL STATIC PHASE ERROR**
- **ADJUSTABLE DC LOOP GAIN**

ABSOLUTE MAXIMUM RATINGS: T_A = 25°C unless otherwise noted.

Supply Current	40 mA
Output Voltage	40 V
Output Current	30 mA
Sync Input Voltage (Pin 3)	5.0 V_{p-p}
Flyback Input Voltage (Pin 4)	5.0 V_{p-p}
Power Dissipation (Package Limitation)	
Plastic Package	625 mW
Derate above T_A = 25°C	5.0 mW/°C
Operating Temperature Range (Ambient)	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

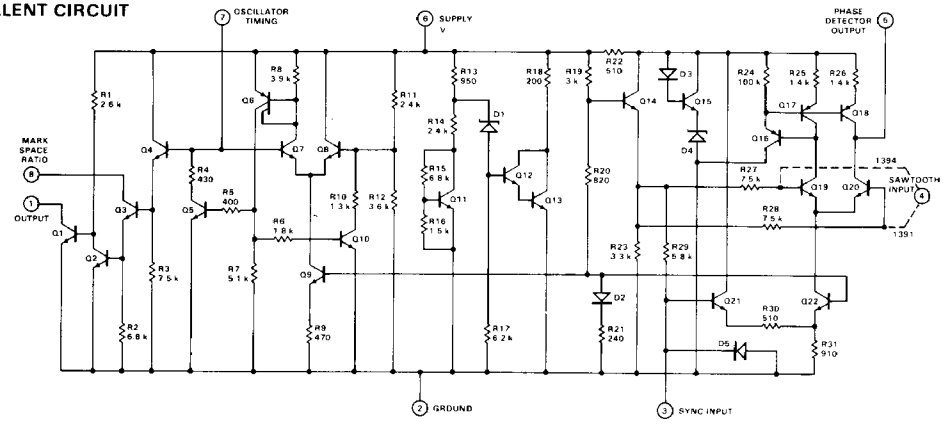
CONNECTION DIAGRAM
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T
PACKAGE CODE T



ORDER INFORMATION

TYPE	PART NO.
μA1391	μA1391TC
μA1394	μA1394TC

EQUIVALENT CIRCUIT



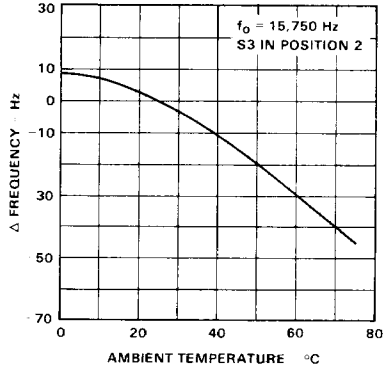
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: T_A = 25°C, unless otherwise noted (See Test Circuit, all switches in Position 1)

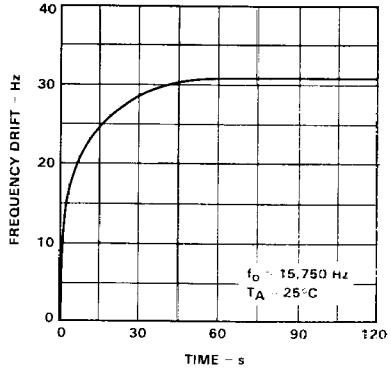
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Regulated Voltage (Pin 6)		8.0	8.6	9.0	V
Supply Current (Pin 6)			20		mA
Collector-Emitter Saturation Voltage (Output Transistor Q1 in Equivalent Circuit)	I_C = 20 mA, Pin 1		0.15	0.25	V
Voltage (Pin 4)			2.0		V
Oscillator Pull-in Range Adjust R_H in Figure 2			±300		Hz
Oscillator Hold-in Range Adjust R_H in Figure 2			±900		μs
Static Phase Error	Δf = 300 Hz		0.5		μs
Free-running Frequency Supply Dependance (S1 in Position 2)			±3.0		Hz/V
Phase Detector Leakage (Pin 5) (All switches in Position 2)				+1.0	μA
Sync Input Voltage (Pin 3)		2.0		5.0	V_{p-p}
Sawtooth Input Voltage (Pin 4)		1.0		3.0	V_{p-p}

TYPICAL ELECTRICAL CHARACTERISTICS

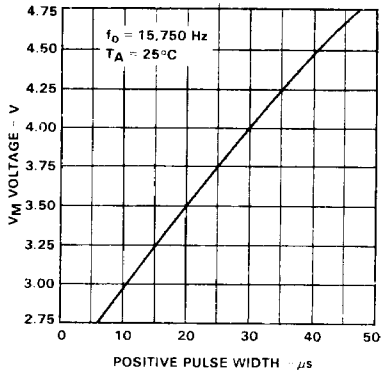
FREQUENCY AS A FUNCTION OF AMBIENT TEMPERATURE

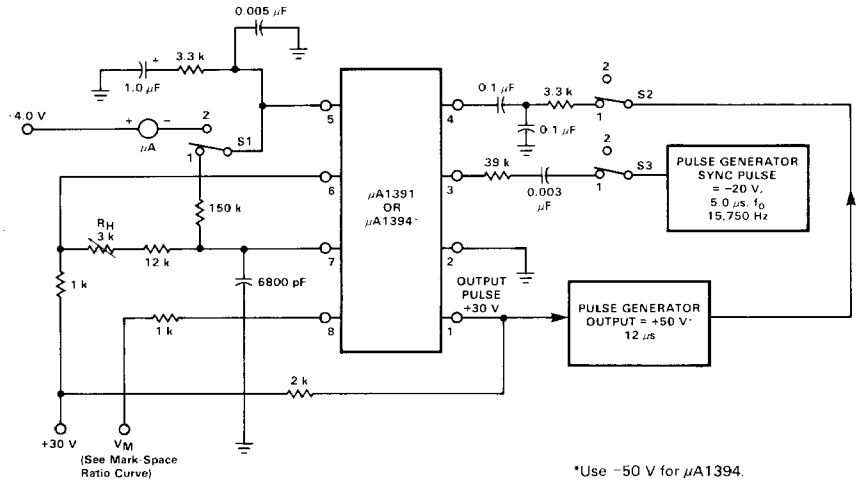


FREQUENCY DRIFT AS A FUNCTION OF WARM-UP TIME



MARK SPACE RATIO





TEST CIRCUIT

μA1391/μA1394 APPLICATIONS INFORMATION

The μA1391 and μA1394 integrated circuits are identical except for the polarity of the sawtooth input signal accepted at Pin 4. The μA1391 requires a positive ramp sawtooth signal during the horizontal retrace period; the μA1394 requires a negative ramp.

The following discussion makes no distinction between the μA1391 and the μA1394. Reference should be made to the "Typical Application Circuit."

This circuit contains a temperature-compensated shunt regulator which operates over a wide current range to accommodate normal fluctuations from an unregulated power supply. A minimum current of 18 mA into Pin 6 is recommended for good regulation. Allowing for 2 mA of shunt current external to the device, a minimum of 20 mA should be supplied through dropping resistors R_A and R_B:

$$R_A + R_B = \frac{\text{Unregulated Supply (Min)} - 9.0\ \text{V}}{20\ \text{mA}}$$

Resistors R_A and R_B may be combined and capacitor C_A eliminated when operating from a supply having less than 3% ripple.

The duty cycle of the output is controlled by the voltage (V_M) applied to Pin 8. The OFF time (output HIGH) is variable from 6 μs to 48 μs by changing V_M from 2.75 V to 4.75 V. (See Mark-Space Ratio Typical Performance Curve.) The source impedance to Pin 8 (parallel resistance of R_D and R_E) should be 1 kΩ for stable operation.

The oscillator free-running fequency is primarily determined by the RC network connected to Pin 7 and is given by the approximate expression:

$$f_o \simeq \frac{1}{0.6\ R_C\ C_B}$$

The desired free-running oscillator fequency is 15,734 Hz in conventional receivers or 31,468 Hz for systems which derive vertical sync by counting down from twice horizontal frequency. Either frequency may be obtained by a wide combination of values for R_C and C_B.

Oscillator sensitivity, however, is a direct function of R_C which therefore provides an independent means for adjusting the dc loop gain and thus the static phase accuracy. The expression for dc loop gain is

$$f_c = \mu\beta$$

where f_c is loop gain with units of Hz/radian, μ is phase detector sensitivity which, for the μA1391/94, has units of A/radian and β is oscillator sensitivity with units, correspondingly, of Hz/A.

The phase detector sensitivity of the μA1391/94 is:

$$\mu = \frac{I_{5(\text{positive})} - I_{5(\text{negative})}}{6.28\ \text{radians}}$$

Typically, $I_{5(\text{positive})} - I_{5(\text{negative})} = 0.5$ mA,

$$\therefore\ \mu_{\text{typical}} = 0.16\ \text{mA/radian}$$

Neglecting the effects of R_Y and R_4, oscillator sensitivity of the device is given by:

$$\beta = \frac{f_o R_C}{0.6\ V_6}$$

Typically, $V_6 = 8.5$ V and $f_o = 15{,}734$ Hz,

$$\beta_{\text{typical}} = R_C \times 3.1\ \text{Hz/mA}$$

Combining the above expressions for μ and β:

$$f_{c\ \text{typical}} = 0.5\ R_C\ \text{Hz/radian}$$

where R_C is in ohms.

The static phase error is inversely proportional to dc loop gain and is given by:

$$\theta = \frac{\Delta f}{f_c} \text{ radians}$$

where θ is static phase error in radians and Δf is oscillator tuning error in Hz.

For convenience, static phase error may also be expressed in μs. At f_o = 15,734 Hz:

$$t_s = 10.1 \frac{\Delta f}{f_c} \ \mu s$$

Static phase error, for a given oscillator tuning error, can therefore be chosen by the selection of R_C. Static phase error should only be made small enough to ensure clean burst gating (about ±0.5 μs for color receivers), since unnecessarily high dc loop gain would have the undesirable effect of making the loop overly sensitive to thermal noise induced horizontal jitter.

Static phasing can be adjusted by adding a small resistor in a series or a large resistor in parallel with the flyback pulse integrating capacitor.

The design of the dynamic characteristics of the loop is less straightforward and involves certain compromises. A loop filter designed for high immunity to impulse noise disturbances will tend to have a response which is too slow for tracking phase changes caused by airplane flutter. Pull-in time and pull-in range will also be adversely affected. A fast responding loop, however, may suffer from excessive ringing following an impulse noise disturbance.

The dynamic characteristics of the loop can be directly affected by the selection of values for R_X, R_Y and C_C once R_C is selected for satisfactory static phase error performance. The values of R_X, R_Y and C_C shown in the Typical Application Circuit represent a reasonable compromise although factors ranging from horizontal APC interaction with the AGC system to designer preferences could modify these values. It should be noted that an increase in the value of R_Y will reduce the hold-in range.

The following simplified equations may be found helpful for optimizing the loop characteristics:

$$f_{\eta\eta} \text{ (noise bandwidth)} = \frac{1 + X^2 \omega_c}{4 \times 1}$$

$$\omega_\eta \text{ (natural undamped loop resonant feequency)} = \frac{\omega_c}{(1 + X)\, T}$$

and

$$K \text{ (Damping coefficient)} = \frac{X^2 T \omega_c}{4}$$

where

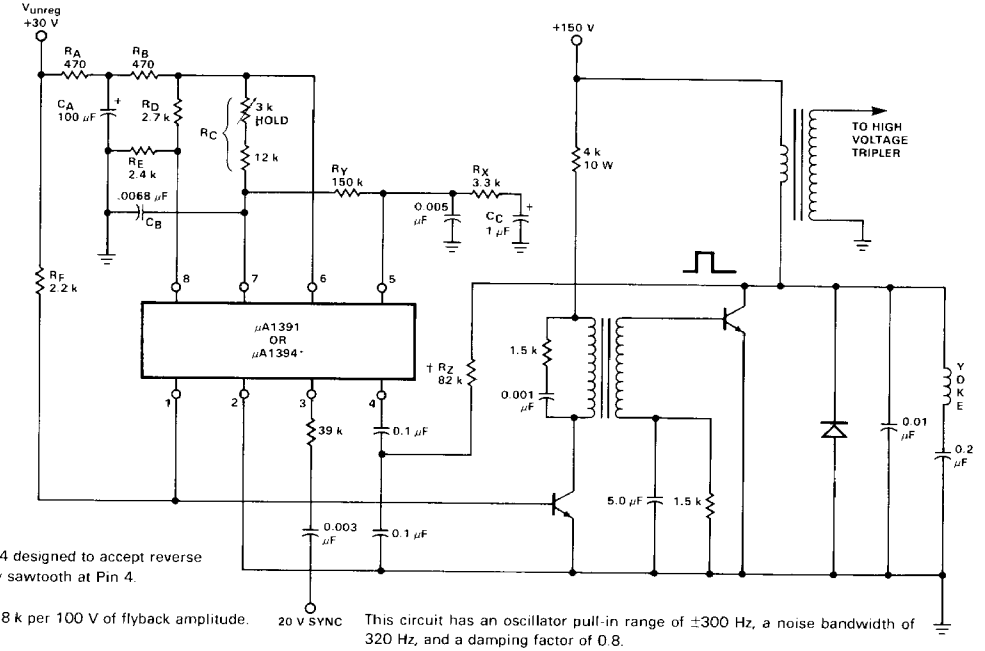
$$X = \frac{R_Y}{R_X}$$

$$\omega_c = 2 \pi f_c,$$

and

$$T = R_Y C_C$$

Although the μA1391/94 operates at a relatively low frequency, care should nevertheless be exercised in the layout of associated components to prevent ringing and undesired coupling of signals.



*μA1394 designed to accept reverse polarity sawtooth at Pin 4.

†R_Z = 6.8 k per 100 V of flyback amplitude.

This circuit has an oscillator pull-in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

Fig. 1 TYPICAL APPLICATION CIRCUIT