

## 8-Bit Serial Shift Registers

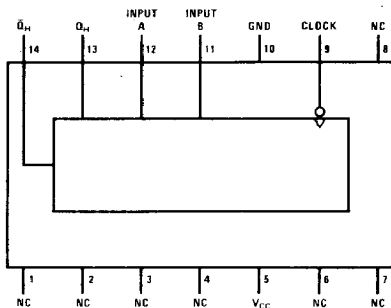
### General Description

These serial-in, serial-out 8-bit shift registers are composed of eight **RS** master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift-register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

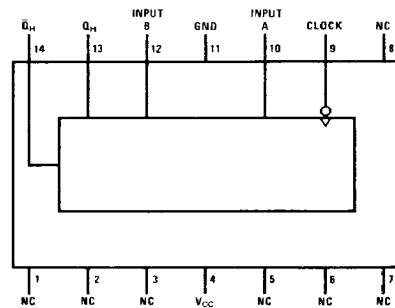
### Features

TYPE	TYPICAL CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
91A	22 MHz	175 mW
L91	8 MHz	17.5 mW

### Connection Diagrams



5491A/7491A(J), (N);  
54L91/74L91(J), (N)



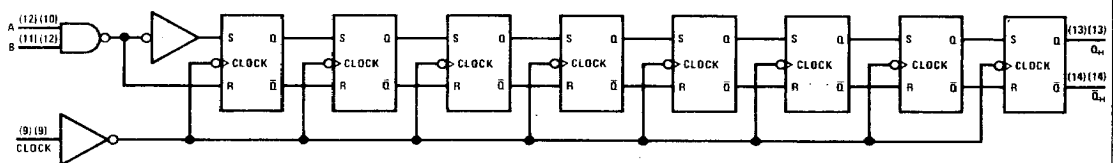
5491A/7491A(W);  
54L91/74L91(W)

### Truth Table

INPUTS		OUTPUTS	
A	B	Q <sub>n</sub>	Q <sub>n+8</sub>
H	H	H	L
L	X	L	H
X	L	L	H

H = High, L = Low,  
X = Don't Care  
t<sub>n</sub> = Reference bit time, clock low,  
t<sub>n+8</sub> = Bit time after 8  
low-to-high  
clock transitions.

### Logic Diagram



**Electrical Characteristics** over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	DM54/74			DM54L/74L			UNITS
			91A			L91			
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
$V_{IH}$	High Level Input Voltage		2			2		V	
$V_{IL}$	Low Level Input Voltage				0.8		0.7	V	
$I_{OH}$	High Level Output Current				-800		-200	$\mu$ A	
$V_{OH}$	High Level Output Voltage	$V_{CC} = \text{Min}, V_{IH} = 2V$ $V_{IL} = \text{Max}, I_{OH} = \text{Max}$	2.4	3.5		2.4	2.8	V	
$I_{OL}$	Low Level Output Current		DM54		16		2	mA	
			DM74		16		3.6		
$V_{OL}$	Low Level Output Voltage	$V_{CC} = \text{Min}, V_{IH} = 2V$ $V_{IL} = \text{Max}, I_{OL} = \text{Max}$	DM54	0.22	0.4		0.15	0.3	V
			DM74	0.22	0.4		0.2	0.4	
$I_I$	Input Current at Maximum Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5V$			1		0.1	mA	
$I_{IH}$	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4V$			40		10	$\mu$ A	
$I_{IL}$	Low Level Input Current	$V_{CC} = \text{Max}$						mA	
									$V_I = 0.3V$
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}(2)$	DM54	-20	-57	-3	-8	-15	mA
			DM74	-18	-57	-3	-8	-15	
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}(3)$	DM54		35	50		3.5	6.6
			DM74		35	58		3.5	6.6

**Notes**

- (1) All typical values are at  $V_{CC} = 5V, T_A = 25^\circ C$ .
- (2) Not more than one output should be shorted at a time.
- (3)  $I_{CC}$  is measured after the eighth clock pulse with the output open and A and B inputs grounded.

**Switching Characteristics**  $V_{CC} = 5V, T_A = 25^\circ C$ 

PARAMETER		CONDITIONS	DM54/74			CONDITIONS	DM54L/74L			UNITS	
			91A				L91				
			MIN	TYP	MAX		MIN	TYP	MAX		
$f_{max}$	Maximum Clock Frequency	$C_L = 15 \text{ pF}$ $R_L = 400\Omega$	10	22		$C_L = 50 \text{ pF}$ $R_L = 4 \text{ k}\Omega$	4	8		MHz	
$t_{PLH}$	Propagation Delay Time, Low-to-High Level Output			18	40			40	80		ns
$t_{PHL}$	Propagation Delay Time, High-to-Low Level Output			27	40			65	130		ns
$t_{W(CLOCK)}$	Width of Clock Input Pulse		25				120			ns	
$t_{SETUP}$	Setup Time		25				120			ns	
$t_{HOLD}$	Hold Time		0				0			ns	