Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

11.0 D.C. SPECIFICATIONS

11.1 Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Supply Voltage	−0.5V to +8.0V
Voltage on Any Input	GND −2V to 6.5V
Voltage on Any Output	GND −0.5V to V_{CC} +0.5V
Power Dissipation	1W

11.2 D.C. Characteristics T_A = 0°C to 70°C, V_{SS} = AV_{SS} = 0V

64 PIN D.C. CHARACTERISTICS

Symbol	Parameter	V_{CC} = +5V ±10%(7)			V_{CC} = 3.3V ± 0.3V		
		Min(V)	Max(V)	Test Conditions	Min(V)	Max(V)	Test Conditions
V_{ILC}	Input Low Voltage, X1	−0.5	0.8		−0.3	0.8	
V_{IHC}	Input High Voltage, X1	3.9	V_{CC} + 0.5		2.4	V_{CC} + 0.3	
V_{IL}	Input Low Voltage (all pins except X1)	−0.5	0.8		−0.3	0.8	
V_{IH}	Input High Voltage (all pins except X1)	2.0	V_{CC} + 0.5		2.0	V_{CC} + 0.3	
V_{OL}(8)	System Interface		0.45	I_{OL} = 12 mA		0.45	I_{OL} = 6 mA
	FDD Interface outputs		0.45	I_{OL} = 24 mA		0.45	I_{OL} = 12 mA
	Status Outputs (Note 6)		0.45	I_{OL} = 4 mA		0.45	I_{OL} = 4 mA
V_{OH}	All outputs	3.0		I_{OH} = −4.0 mA	2.4		I_{OH} = −2.0 mA
	All outputs	V_{CC} − 0.4		I_{OH} = −100 µA	V_{CC} − 0.2		I_{OH} = −100 µA

64 PIN D.C. CHARACTERISTICS (I_{CC})

Symbol	Parameter	V_{CC} = +5V ±10%(7)			V_{CC} = 3.3V ± 0.3V		
		Typ	Max(A)	Test Conditions	Typ	Max(A)	Test Conditions
I_{CC1}	1 Mbps Data Rate V_{IL} = V_{SS}, V_{IH} = V_{CC}	15.4 mA	25 mA	(Notes 1, 2, 5)	8.4 mA	16 mA	(Notes 1, 2)
I_{CC2}	1 Mbps Data Rate V_{IL} = 0.45V, V_{IH} = 2.4V	20.8 mA	30 mA	(Notes 1, 2, 5)	8.6 mA	16 mA	(Notes 1, 2)
I_{CC3}	500 Kbps Data Rate V_{IL} = V_{SS}, V_{IH} = V_{CC}	11.8 mA	20 mA	(Notes 1, 2)	6.2 mA	14 mA	(Notes 1, 2)
I_{CC4}	500 Kbps Data Rate V_{IL} = 0.45V, V_{IH} = 2.4V	17.6 mA	25 mA	(Notes 1, 2)	6.2 mA	14 mA	(Notes 1, 2)
I_{CCSB}	I_{CC} in Powerdown	0 µA	60 µA	(Notes 3, 4)	0 µA	60 µA	(Notes 3, 4)

64 PIN D.C. CHARACTERISTICS (I_{CC}) (Continued)

Symbol	Parameter	V_{CC} = +5V ±10%(7)			V_{CC} = 3.3V ± 0.3V		
		Typ	Max(A)	Test Conditions	Typ	Max(A)	Test Conditions
I_{IL}	Input Load Current (all input pins)		10 μA −10 μA	$V_{IN} = V_{CC}$ $V_{IN} = 0V$		10 μA −10 μA	$V_{IN} = V_{CC}$ $V_{IN} = 0V$
I_{OFL}	Data Bus Output Float Leakage		±10 μA	$0.45 < V_{OUT} < V_{CC}$		±10 μA ±10 μA	$0.45 < V_{OUT} < V_{CC}$

NOTES:
1. Only the data bus inputs may float.
2. Tested while reading a sync field of "00". Outputs not connected to D.C. loads.
3. $V_{IL} = V_{SS}$, $V_{IH} = V_{CC}$; Outputs not connected to D.C. loads.
4. Typical value with the oscillator off.
5. I_{CC} for 2 Mbps Data Rate: Max 40 mA (TTL), 35 mA (CMOS) at 5.5V, typical 29.2 mA (TTL) and 24.4 (CMOS).
6. Status outputs are PD, IDLE, and RDGATE.
7. V_{CC} and V_{CCF} for the 82078-1 is +5V ±5%.
8. V_{OL} change effective for both 44-pin and 64-pin package offerings.

2

64 PIN MIXED MODE D.C. CHARACTERISTICS

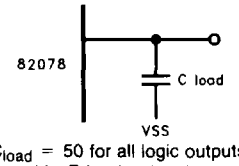
Symbol	Parameter	V_{CC} = 3.3V ±0.3V, V_{CCF} = +5V ±10%(7)		
		Min(V)	Max(V)	Test Conditions
V_{ILC}	Input Low Voltage, X1	−0.3	0.8	
V_{IHC}	Input High Voltage, X1	2.4	V_{CC} + 0.3	
V_{IL}	Input Low Voltage (system pins except X1) (floppy drive interface pins)	−0.3 −0.5	0.8 0.8	
V_{IH}	Input High Voltage (system interface pins except X1) (floppy drive interface pins)	2.0 2.0	V_{CC} + 0.3 V_{CC} + 0.5	
V_{OL}	System Interface		0.4	I_{OL} = 6 mA
	FDD Interface outputs		0.4	I_{OL} = 24 mA
	Status Pins: IDLE, PD, RDGATE		0.4	I_{OL} = 4 mA
V_{OH}	All system outputs	2.4		I_{OH} = −2.0 mA
	All FDD interface outputs	3.0		I_{OH} = −4.0 mA
	All system outputs	V_{CC} − 0.2		I_{OH} = −100 μA
	All FDD interface outputs	V_{CC} − 0.4		I_{OH} = −100 μA

CAPACITANCE

C_{IN}	Input Capacitance	10	pF	F = 1 MHz, T_A = 25°C
C_{IN1}	Clock Input Capacitance	20	pF	Sampled, not 100% Tested
$C_{I/O}$	Input/Output Capacitance	20	pF	

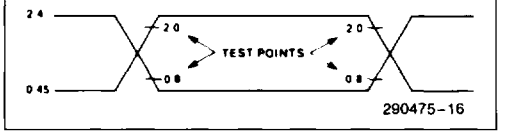
NOTE:
All pins except pins under test are tied to AC ground.

LOAD CIRCUIT

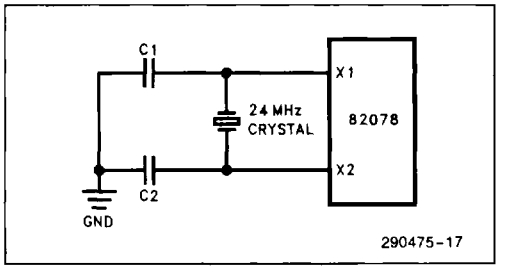


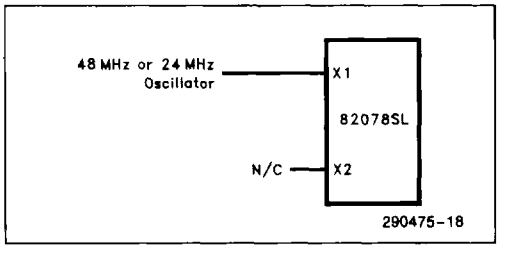
C_{load} = 50 for all logic outputs, 100 pF for the data bus.

A.C. TESTING INPUT, OUTPUT WAVEFORM



11.3 Oscillator





The 24 MHz clock can be supplied either by a crystal or a MOS level square wave. All internal timings are referenced to this clock or a scaled count which is data rate dependent.

The crystal oscillator must be allowed to run for 10 ms after V_{CC} has reached 4.5V or exiting the POWERDOWN mode to guarantee that it is stable.

Frequency:	24 MHz ±0.1%
Mode:	Parallel Resonant
	Fundamental Mode
Series Resistance:	Less than 40Ω
Shunt Capacitance:	Less than 5 pF