SP9550

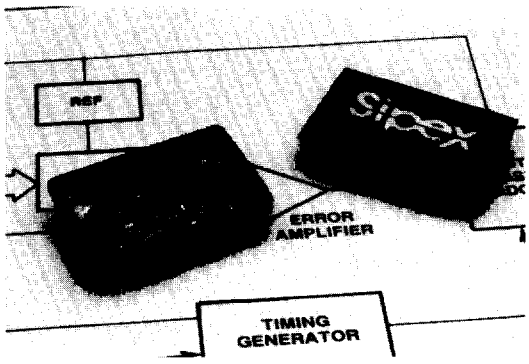
5 MHz, MULTIPASS™ 12-BIT A/D CONVERTER

DESCRIPTION

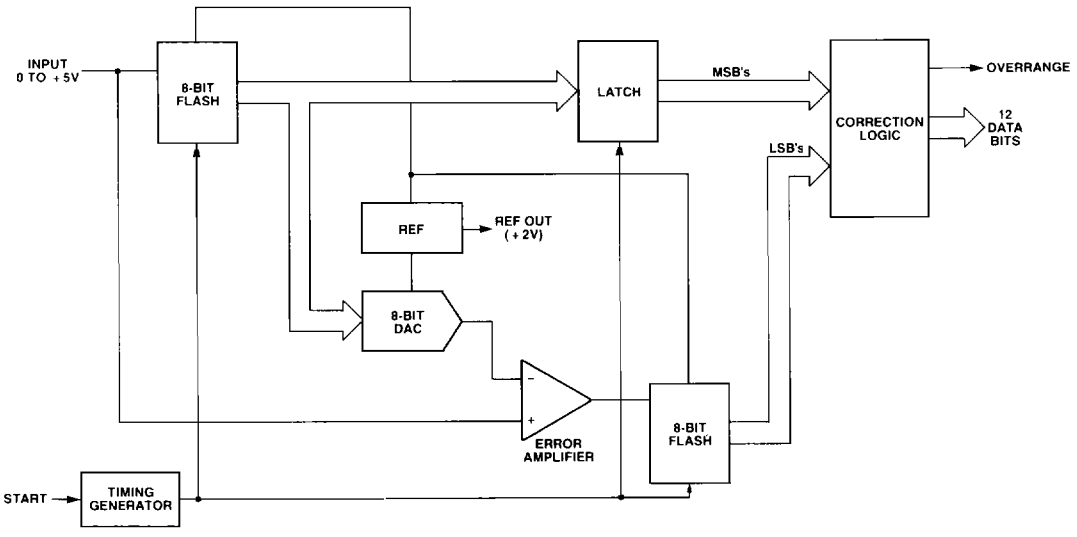
The SP9550 is a 12-bit, 200 nanosecond, analog-to-digital converter employing the SIPEX state-of-the-art Multipass™ subranging Flash technology. The subranging Multipass process is optimized for high accuracy operation by using two 8-bit Flashes in a feed-forward error correction scheme to yield a final resolution of 12 bits while consuming less than 2.5 watts.

The SP9550 can be used in either a single or continuous mode. In the single mode, a START command initiates the conversion on its rising edge and completes the conversion on its falling edge. Total conversion can be completed in less than 200 nanoseconds. By repeating the START command every 200 nanoseconds, the SP9588 will operate in a continuous mode at a maximum of 5 MHz.

The SP9550 input range, 0 to +5V, has been optimized for high accuracy applications such as radar, sonar and video digitization, and high speed data acquisition systems. The SP9550 is ideal in all applications that require 12-bit performance at relatively high speed with moderately low power consumption.



FUNCTIONAL DIAGRAM



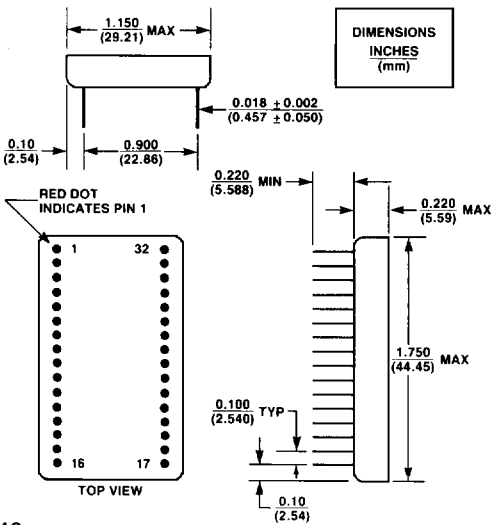
9

SPECIFICATIONS

(Typical @25°C and nominal supply voltages unless otherwise specified.)

MODEL	SP 9550
RESOLUTION	12-Bits
ANALOG INPUTS	
Input Voltage Range	0 to +5V
Input Impedance	1kΩ
DIGITAL INPUTS	
Logic Levels: Logic "1"	2.4V min
Logic "0"	0.4V max
Logic Loading	1 TTL Load
ACCURACY	
Integral Linearity	
@25°C	±½ LSB
0°C to +70°C	±1 LSB
Differential Linearity	
@25°C	±½ LSB
0°C to +70°C	±1 LSB
No Missing Codes	Guaranteed
Offset Error	0.2% of FSR typ, 0.5% max
Gain Error	0.2% of FSR typ, 0.5% max
DYNAMIC PERFORMANCE	
Conversion Time	200nsec
STABILITY	
Integral Linearity Tempco	10 ppm/°C
Differential Linearity Tempco	2 ppm/°C
Unipolar Offset Error Drift	5 ppm/°C
Gain Error Drift	40 ppm/°C
DIGITAL OUTPUTS	
Output Coding (Straight Binary)	See Table
Output Drive Capability	4 TTL Loads
REFERENCE	
Voltage	+2.0V nom
External Current	5mA
POWER SUPPLY REQUIREMENTS	
Current @nominal Voltage	
+15V (±10%)	15mA
−15V (±10%)	15mA
+5V Digital (±10%)	225mA
+5V Analog (±1%)	125mA
−5V (±1%)	75mA
Dissipation	2.4W typ, 2.7W max
PACKAGE	
Triple DIP — Metal	32-Pin

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	START (CLOCK)	32	NC
2	NC*	31	+5V DIGITAL
3	NC*	30	DIGITAL GND
4	BIT 12 (LSB)	29	+5V ANALOG
5	BIT 11	28	−5V
6	BIT 10	27	ANALOG GND
7	BIT 9	26	ANALOG GND
8	BIT 8	25	−15V
9	BIT 7	24	+15V
10	BIT 6	23	REF OUT
11	BIT 5	22	TEST POINT
12	BIT 4	21	NC
13	BIT 3	20	TEST POINT
14	BIT 2	19	NC
15	BIT 1 (MSB)	18	TRIM
16	OVERRANGE	17	ANALOG INPUT

*Internally connected to ground

THEORY OF OPERATION

INTERFACE INFORMATION

The SP 9550 is designed primarily for high speed applications that require a conversion time as low as 200 nanoseconds (185ns min). Of course, the SP 9550 will operate at slower conversion times with no degradation. The rate of conversion is set by the START signal that is applied to it. The rising edge of the START signal initiates the conversion process and the falling edge of the START signal completes the process.

The input stage has been designed for fast settling so as to function in a data acquisition environment with S/H amplifiers and multiplexers. As such, the input signal should be driven by a low impedance source sufficient to drive the 1K ohm input impedance at 12-bit accuracy. Most S/H amplifiers and fast operational amplifiers are adequate...but some thought must be given to their selection.

CONVERSION PROCESS

As shown in the block diagram, the input analog signal is directed to the input of the first 8-BIT FLASH ADC. The FLASH converter also receives a reference voltage (REF) of 2.0 volts. The input signal is compared to this reference in the conversion process by the FLASH converter and the resulting digital 8-bit word, which represents the most significant bits (MSB), is internally latched for further processing by both the 8-bit DAC and the CORRECTION LOGIC.

The above sequence is refered to as the "first pass" or "input" conversion. The resulting 8-bit word is sent to an 8-bit DAC which is trimmed to better than 12-bit accuracy. The DAC output is then directly subtracted from the input signal to determine the "error" or "second pass" input signal to be converted by the Flash.

The "second pass" occurs when the ERROR AMPLIFIER output is directed to the input of the second FLASH converter. The result of this conversion process is a digital word which represents the least significant bits (LSB). This digital output is now ready for further processing by the CORRECTION LOGIC.

INPUT VOLTAGE	BINARY BITS OR	1	2	3	4	5	6	7	8	9	10	11	12	HEX CODE
0.00000		0	0	0	0	0	0	0	0	0	0	0	0	0 0 0 0
0.00122		0	0	0	0	0	0	0	0	0	0	0	1	0 0 0 1
2.49878		0	1	1	1	1	1	1	1	1	1	1	1	0 7 F F
2.50000		1	0	0	0	0	0	0	0	0	0	0	0	0 8 0 0
2.50122		1	0	0	0	0	0	0	0	0	0	0	1	0 8 0 1
4.99878		1	1	1	1	1	1	1	1	1	1	1	1	0 F F F
5.00000	1	0	0	0	0	0	0	0	0	0	0	0	0	1 0 0 0
5.00122	1	0	0	0	0	0	0	0	0	0	0	0	1	1 0 0 1
5.29175	1	0	0	0	0	1	1	1	0	1	1	1	1	1 0 E F
5.83%	Overrange													

SP 9550 Coding Table @5 Volt Full Scale

The CORRECTION LOGIC accepts the 8 MSB's and the 8 LSB's and combines them by an improved, unique algorithm using digital addition. The result is a 12-bit digital word which accurately represents the analog input. The CORRECTION LOGIC also provides an overrange (O.R.) bit to indicate that the input has exceeded full scale. The output coding is straight binary. Refer to Coding Table.

The entire conversion process is controlled by the TIMING GENERATOR which only requires a START signal as previously described. The falling edge of the START signal indicates that the digital data is ready.

SINGLE CONVERSION MODE

The single conversion mode is shown on the TIMING GENERATOR timing diagram. The timing sequence shown reflects the nominal minimum conversion time required.

Referring to the timing diagram, the process is as follows:

1. The rising edge of the START signal causes the first FLASH to perform a conversion to determine the MSB's. Old data from the previous conversion remains intact.
2. The falling edge of the START signal causes the second FLASH to perform a conversion to determine the LSB's. New data will be valid 50 nanoseconds later.

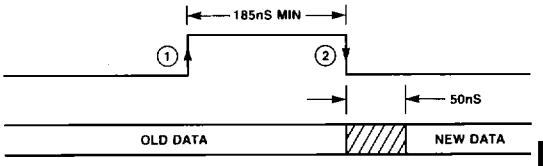
CONTINUOUS CONVERSION MODE

The SP 9550 will be in the continuous conversion mode as long as the START signal is repeated. This mode is used to follow high speed input signals and is capable of a 5 MHz converting rate. However, an external S/H amplifier is required...the time necessary for the S/H amplifier to acquire and settle must be taken into consideration.

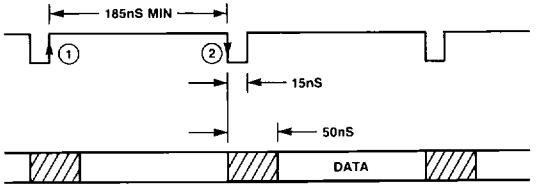
Referring to the timing diagram, the process is as follows:

1. The rising edge of the START signal causes the first FLASH to perform a conversion to determine the MSB's. Old data from the previous conversion reamins intact.
2. The falling edge of the START signal causes the second FLASH to perform a conversion to determine the LSB's. New data will be valid 50 nanoseconds later.

The process is repeated continuously as shown in the timing diagram. When operating at the maximum rate of 5 MHz, the START signal should be high for only 185 nanoseconds and low for 15 nanoseconds. When using an external S/H amplifier, the START signal should be high for the full 200 nanoseconds and low for the time required for the S/H amplfier to acquire and settle. The resulting conversion rate will be proportional to the total time required for both the S/H amplifier and the SP 9550.



SINGLE CONVERSION



5 MHZ CONVERSION

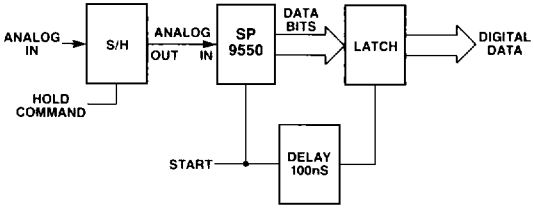
SP 9550 Timing Diagram

TYPICAL APPLICATIONS

The application block diagram illustrates a typical system using the SP 9550 with an external S/H amplifier and an external latch for the data bits. Since the data is valid 50 nanoseconds after the falling edge of the START signal, the START signal needs to be de-

layed by more than 50 nanoseconds if it is to be used as the strobe for the latch.

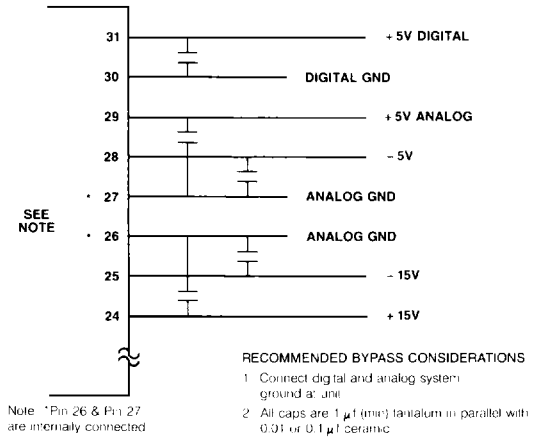
The SP 9550 can be used directly without a S/H amplifier to take a quick snapshot of a slow moving input signal. The maximum input frequency that can be followed without a S/H amplifier is approximately 20 kHz which allows for the conversion of audio band signals.



Typical Application: SP 9550 With External S/H Amplifier & External Latch

POWER SUPPLY CONNECTIONS

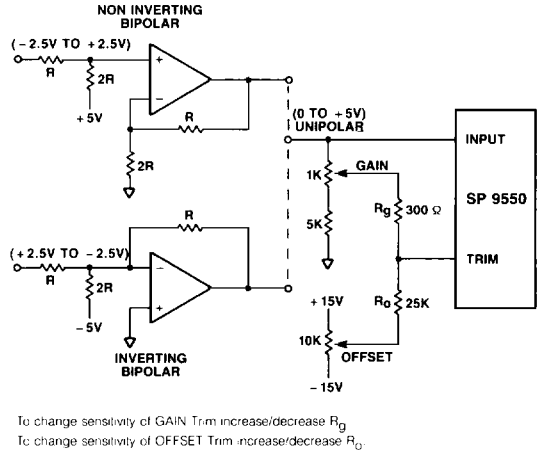
As shown in the Power Supply Connection diagram, 5 pairs of capacitors are recommended for bypassing the power supplies at the SP 9550. Also note that it is recommended to externally connect the analog and digital grounds at the SP 9550. Also, the analog and digital + 5V supplies should be separate for optimum performance.



SP 9550 Power Supply Connections

TRIM ADJUSTMENTS

The SP 9550 can be externally trimmed for gain and offset as shown in the block diagram. To change the sensitivity of the gain trim, increase or decrease the value of R_g (300 ohm). To change the sensitivity of the offset trim, increase or decrease the value of R_o (25k ohm). The interaction of the gain and offset trim is minimal; some readjustment may have to be made if one or the other trim is extreme.



To change sensitivity of GAIN Trim increase/decrease R_g
To change sensitivity of OFFSET Trim increase/decrease R_o

SP 9550 Fine Trim Adjustments

BIPOLAR OPERATION

Since the SP 9550 is a unipolar A/D converter, bipolar operation can only be obtained by level shifting the input signal. The FINE TRIM block diagram illustrates this process for either inverting or non-inverting operation using a suitable Operational Amplifier. The value of R should be carefully selected for speed and accuracy. The GAIN and OFFSET adjustments can be used to trim the final input range as previously described.

SUMMARY

The SP 9550 has been designed to simplify high speed conversion and operate at reasonable power levels. The subranging technique and correction logic have been optimized to provide the accuracy. With this in mind, the SP 9550 is a realistic solution to most high speed data conversion problems.

ORDERING INFORMATION

MODEL	OPERATING TEMPERATURE RANGE	SCREENING
SP 9550C	0 to +70°C	—
SP 9550B	−55°C to +125°C	MIL-STD-883C