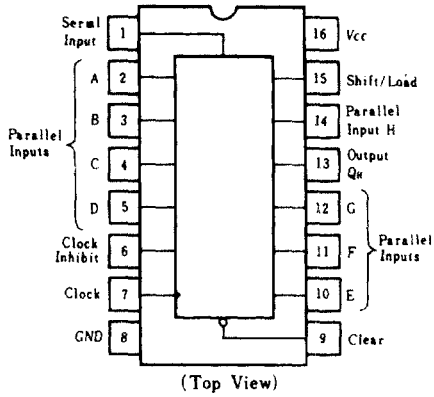
HD74HC166 ● Parallel-load 8-bit Shift Register

This device is an 8-bit shift register with an output from the last stage. Data may be loaded into the register either in parallel or in serial form. When the Shift/Load input is low, the data is loaded asynchronously in parallel. When the Shift/Load input is high, the data is loaded serially on the rising edge of either clock inhibit or Clock. Clear is asynchronous and active-low.

The 2-input NOR clock may be used either by combining two independent clock sources or by designating one of the clock inputs to act as a clock inhibit.

■ PIN ARRANGEMENT

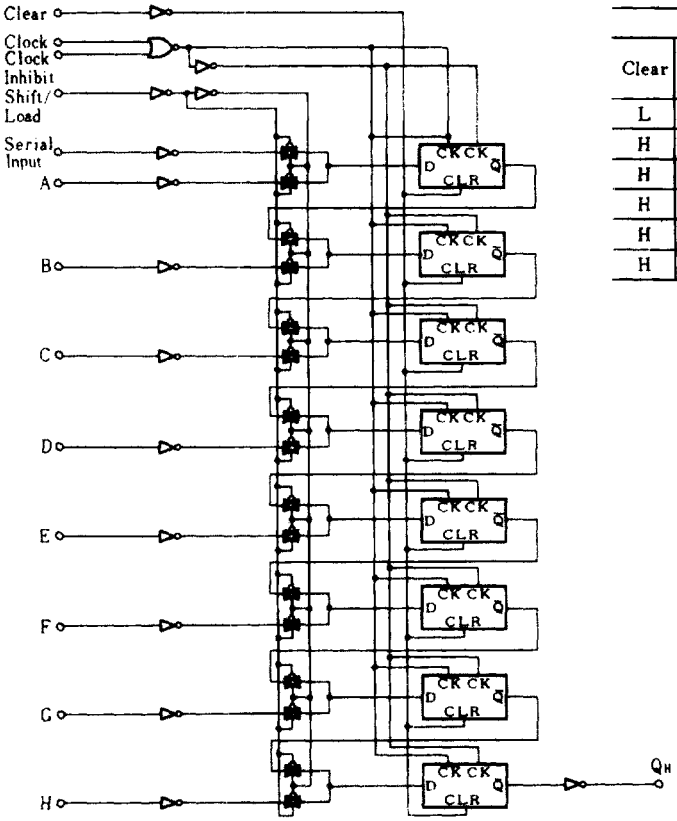


(Top View)

■ FEATURES

- High Speed Operation: t_{pd} (Clock to Q_H)=14ns typ. (C_L=50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: Vcc=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: Icc (static)=4μA max. (Ta=25°C)

■ LOGIC DIAGRAM



■ FUNCTION TABLE

Inputs						Internal Outputs		Output
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A···H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a···h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		$Ta=25°C$ min	$Ta=25°C$ typ	$Ta=25°C$ max	$Ta=-40\sim+85°C$ min	$Ta=-40\sim+85°C$ max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	$V_{in}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		$I_{OH}=-4mA$	4.18	—	—	4.13	—	
		6.0		$I_{OH}=-5.2mA$	5.68	—	—	5.63	—	
	V_{OL}	2.0	$V_{in}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		$I_{OL}=4mA$	—	—	0.26	—	0.33	
		6.0		$I_{OL}=5.2mA$	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	$V_{in}=V_{CC}$ or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	$V_{in}=V_{CC}$ or GND, $I_{out}=0\mu A$		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS ($C_L=50pF$, Input $t_r=t_f=6ns$)

Item	Symbol	V_{CC}(V)	Test Conditions	$Ta=25°C$ min	$Ta=25°C$ typ	$Ta=25°C$ max	$Ta=-40\sim+85°C$ min	$Ta=-40\sim+85°C$ max	Unit
Maximum Clock Frequency	f_{max}	2.0		—	—	5	—	4	MHz
		4.5		—	—	25	—	20	
		6.0		—	—	29	—	24	
Propagation Delay Time	t_{PHL} t_{PLH}	2.0	Clock to Q_H	—	—	175	—	220	ns
		4.5		—	14	35	—	44	
		6.0		—	—	30	—	37	
	t_{PHL}	2.0	Clear to Q_H	—	—	150	—	190	ns
		4.5		—	12	30	—	38	
		6.0		—	—	26	—	33	
Setup Time	t_{su}	2.0	Shift/Load to Clock	150	—	—	190	—	ns
		4.5		30	2	—	38	—	
		6.0		26	—	—	33	—	
		2.0	Data to Clock	100	—	—	125	—	ns
		4.5		20	1	—	25	—	
		6.0		17	—	—	21	—	
Hold Time	t_h	2.0	Clock to Data	5	—	—	5	—	ns
		4.5		5	0	—	5	—	
		6.0		5	—	—	5	—	
Pulse Width	t_w	2.0	Clock, Clear	80	—	—	100	—	ns
		4.5		16	6	—	20	—	
		6.0		14	—	—	17	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	5	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF

■ TIMING DIAGRAM