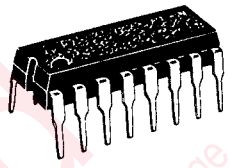
MN4027B/MN4027BS

Dual J-K Flip-Flop

■ Outline

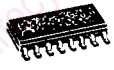
The MN4027B/S has two built-in circuits of J-K flip-flops in one chip. The respective flip-flop has independent J, K, set, clear, and clock outputs and complementary outputs (O, $\overline{O}$).
In the J-K mode, the clear input and the set input both become the "L" leve, and the output changes at the rise of the clock pulse according to the state of J and state of K.
This dual J-K flip-flop is equivalent to Motorola's MC14027B and RCA's CD4027B.

P-3



16-pin plastic DIL package

P-4



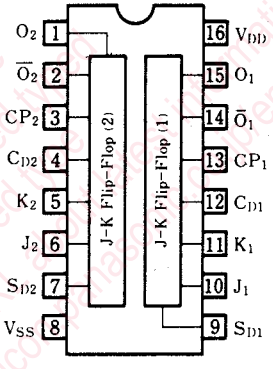
16-pin PANAFLAT package (SO-16D)

■ Truth Table

Input					Output	
S_D	C_D	CP	J	K	O_{n+1}	$\overline{O}_{n+1}$
L	L	↑	L	L	no change	
L	L	↑	H	L	H	L
L	L	↑	L	H	L	H
L	L	↑	H	H	$\overline{O}_n$	O_n
H	L	×	×	×	H	L
L	H	×	×	×	L	H
H	H	×	×	×	H	H
L	L	↓	×	×	no change	

Note) × : don't care

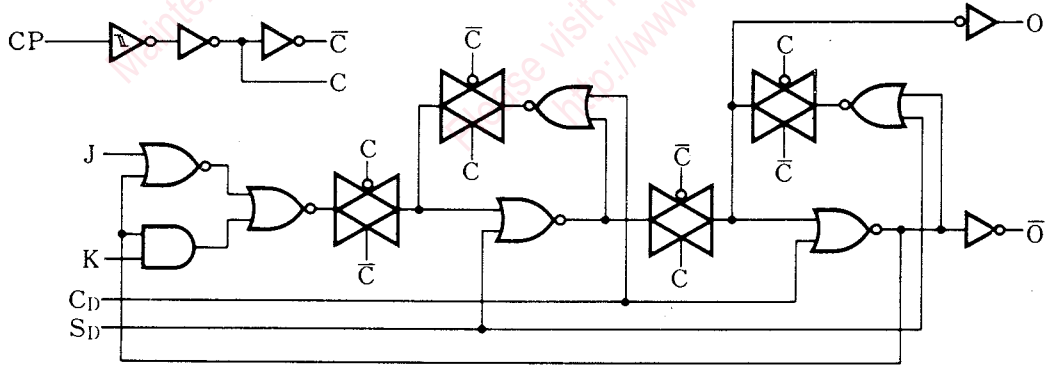
Pin Configuration



Pin description

J, K : Synchronous input
CP : Clock input (↑)
S_D : Asynchronous set input
C_D : Asynchronous clear input
O, $\overline{O}$: Output (complementary)

■ Logic Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Rating	Unit
Supply voltage		V_{DD}	−0.5～+18	V
Input voltage		V_I	−0.5～V_{DD}+0.5*	V
Output pin voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak input · output pin current		$\pm I_I$	max. 10	mA
Power dissipation (per package)	Ta=−40～+60°C	P_D	max. 400	mW
	Ta=+60～+80°C		Decrease to 200mW at the rate of 8mW/°C	
Power dissipation (per output pin)		P_D	max. 100	mW
Operating ambient temperature		T_{opr}	−40～+85	°C
Storage temperature		T_{stg}	−65～+150	°C

* V_{DD}+0.5V should be lower than 18V.

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Condition		Ta=−40°C min.	Ta=−40°C max.	Ta=25°C min.	Ta=25°C max.	Ta=85°C min.	Ta=85°C max.	Unit
Static supply current	5	I_{DD}	$V_I=V_{SS}$ or V_{DD}		—	4	—	4	—	30	μA
	10				—	8	—	8	—	60	
	15				—	16	—	16	—	120	
Output voltage low level	5	V_{OL}	$V_I=V_{SS}$ or V_{DD}, $\|I_O\|<1\mu A$		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output voltage high level	5	V_{OH}	$V_I=V_{SS}$ or V_{DD}, $\|I_O\|<1\mu A$		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input voltage low level	5	V_{IL}	$\|I_O\|<1\mu A$	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input voltage high level	5	V_{IH}	$\|I_O\|<1\mu A$	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output current low level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input leakage current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25°C, V_{SS}=0V, C_L=50pF)

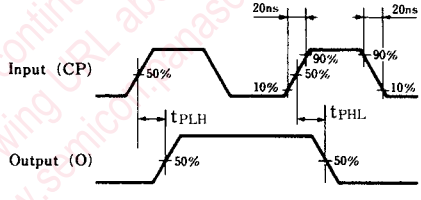
Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
Output rise time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output fall time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation time (CP→O, $\overline{O}$) (H→L)	5	t_{PLH}	—	115	345	ns
	10		—	50	150	
	15		—	35	105	
Propagation time (CP→O, $\overline{O}$) (L→H)	5	t_{PHL}	—	115	345	ns
	10		—	50	150	
	15		—	35	105	
Propagation time (S_D→O)	5	t_{PHL}	—	75	225	ns
	10		—	35	105	
	15		—	25	75	
Propagation time (C_D→O)	5	t_{PHL}	—	130	390	ns
	10		—	50	150	
	15		—	35	105	
Minimum set-up time (J, K→CP)	5	t_{su}	—	50	150	ns
	10		—	15	45	
	15		—	10	30	
Minimum clear pulse width Minimum pre-set pulse width	5	t_{WSDH} t_{WCDH}	—	40	120	ns
	10		—	20	60	
	15		—	15	45	
Maximum clock frequency	5	f_{max}	3	6	—	MHz
	10		7	15	—	
	15		11	22	—	
Input capacitance		C_I	—	—	7.5	pF

● Switching time measuring circuit

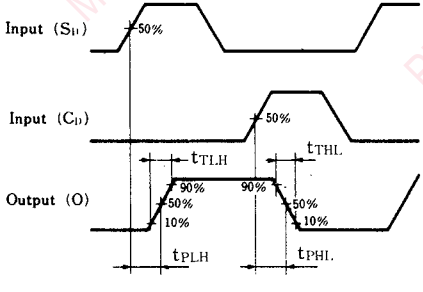
Test No.	J	K	C_D	S_D	CP
1	H	H	L	L	P.G. 1
2	H	H	P.G. 1	P.G. 2	H
3	P.G. 1	P.G. 1	L	L	P.G. 2

Note) P.G.=Pulse generator

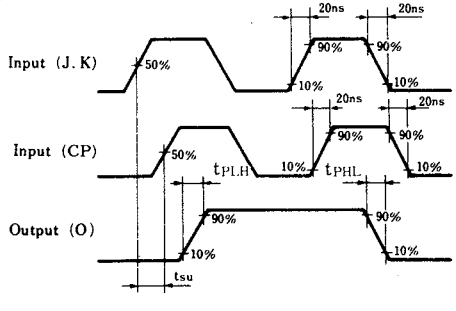
Test No.1 waveforms



Test No.2 waveforms



Test No.3 waveforms



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