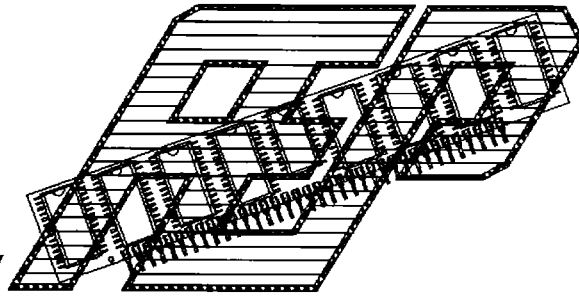


- >> 524,288 x 8 Organization
- >> Double sided to maximize bit density
- >> On board 1-of-16 Decoder
- >> Completely Static operation
- >> TTL compatible
- >> Low power, battery back-up operation capability
- >> Uses single +5V power supply
- >> Super Low Power version available



512 KILOBYTES STATIC RAM MODULE

DESCRIPTION:

The AEPSX512K8 is a high density 512 Kilo-word by 8 bit static random access memory module in a 36 pin single-inline-package format. Physically it consists of an FR4 PC material substrate mounted with sixteen 32K x 8 SOP (small outline package) ICs, the 1-of-16 decoder, four 0.1 microfarad decoupling capacitors, and 36 edge-clip I/O pins.

The module can use any of the 32K x 8 SRAMs made by any of a large number of manufacturers in both Mix-MOS and CMOS technologies. A wide range of access speeds are available. The decoder normally used is the 74HCT154. Other decoder choices available are the 74F154, the 74LS154, and the fully CMOS version 74HC154.

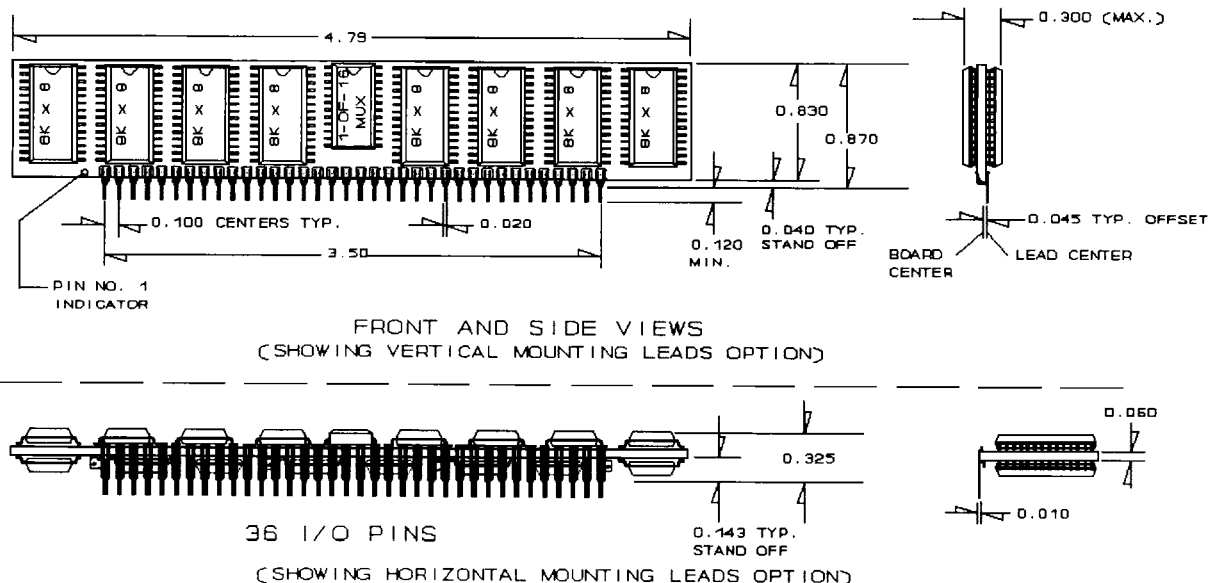
Performance specifications and electrical characteristics are determined by the IC devices used. A typical memory component on the module will draw 100uA (max.) in standby and 70mA (max.) during access (for standard low power devices, super low power use 2uA and 8mA typically).

Mechanical dimensions are 0.88 in. high by 4.79 in. long by 0.30 in. wide. The module is available with either vertical or 90 degree (horizontal) lead pins. The latter allows the module to be mounted on its side which gives a low 0.325 stand-off height. This module is also available in 128K x 8 SRAM organization.

SPECIFICATION DRAWING

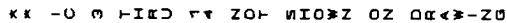
512K x 8 SRAM MODULE

DIMENSIONS IN INCHES, TOLERANCE: +/- 0.010 UNLESS SPECIFIED.



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FUNCTIONAL DIAGRAM



128K x 8 version notes:
pin 23 is a NO CONNECT.
pin 34 is a CHIP SELECT (active low).

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