Sub-1-GHz RF I/Q Front End for Software-Defined Radio and IEEE 802.15.4g

1 Device Overview

1.1 Features

- General
  - Supported Frequency Bands: 863 to 876 MHz and 902 to 930 MHz
  - Wide Supply Voltage Range: 2.3 to 3.6 V
  - Temperature Range: –40°C to +105°C
  - High-Performance Single-Chip Linear Quadrature RF Transceiver With a Digitized I/Q Interface to a DSP
  - Suitable for Systems Targeting Compliance With:
    - FCC 47 CFR Part 15
    - ARIB STD-T108
    - ETSI EN 300 220
    - ETSI EN 303 204
  - Low Current Consumption
    - RX: 32 mA
    - TX:
      - 48 mA @ +10 dBm
      - 42 mA @ +3 dBm
    - Power Down: <1 µA
    - Excellent Phase Noise
      - –101 dBc/Hz at 10-kHz Offset
      - –123 dBc/Hz at 1-MHz Offset
  - Low Cascaded Receiver Noise Figure: 7 dB
  - Industry-Leading RF Coexistence Properties
  - Blocking (3-dB Desensitization):
    - –33 dBm at 10-MHz Offset
    - –36 dBm at 2-MHz Offset
  - High-Performance Linear RF Front End
    - Tailored for All IEEE 802.15.4g PHY Options (MR-FSK, MR-OFDM, MR-O-QPSK [DSSS]) Using the Modulation Formats (G)FSK, O-QPSK, BPSK, QPSK, and 16-QAM
    - RF I/Q Up- and Down-Conversion With Digitized Baseband Input and Output Signals
    - Fully Integrated High-Performance Frequency Synthesizer and Quadrature LO Signal Generator
    - Programmable Output Power up to +13 dBm for Nonlinear Modulation Formats, Such as FSK and up to 3-dBm Average Power for 16-QAM OFDM With Very Fine Step Size
  - Receive Gain: 43 dB
  - TX Error Vector Magnitude (EVM): –29 dB
- Seamless Parallel Interface to DSP
- RoHS Compliant 7-mm × 7-mm RGZ-48 Package
- Optional Reference Clock Output to Facilitate Single Crystal Wireless System Designs

1.2 Applications

- High-Performance, Low-Power, Software-Defined Radio (SDR) Systems at 868-, 915-, and 920-MHz ISM Frequency Bands
- Wireless Smart Grid
- Automated Metering Infrastructure (AMI) and Automatic Meter Reading (AMR)
- Industrial Monitoring and Control
- Support for All IEEE 802.15.4g PHY Modes

1.3 Description

The CC1260 device contains a quadrature RF front end with a digitized baseband signal interface targeting software-defined radio systems. The combination of the CC1260 device and a DSP is tailored for high performance and flexible FSK, OFDM, and DSSS designs (including IEEE 802.15.4g MR-FSK, MR-OFDM, and MR-O-QPSK PHY options). The CC1260 device is designed for excellent performance at very low-power and low-voltage operation in cost-effective wireless systems. The device is mainly intended for the industrial, scientific, and medical (ISM) 863- to 876-MHz and 902- to 930-MHz frequency bands. A typical CC1260-based system design requires only a few external passive components, a DSP (for the digital modem), and a microcontroller (for system control and application). The main operating parameters of the CC1260 device can be controlled using an SPI interface.

Table 1-1. Device Information

PART NUMBER	PACKAGE	BODY SIZE
CC1260RGZR	RGZ (48)	7 mm × 7 mm
CC1260RGZT	RGZ (48)	7 mm × 7 mm

1.4 Functional Block Diagram

Figure 1-1 shows a functional block diagram of the CC1260 device. The CC1260 device can be used as an I/Q RF front end with a digitized interface to an external implementation of the modem functionality using, for example, a DSP. The receiver input can be matched in a differential or single-ended fashion to a 50-Ω impedance. The digital I/Q interface is tailored to fit seamlessly with TI DSP devices.

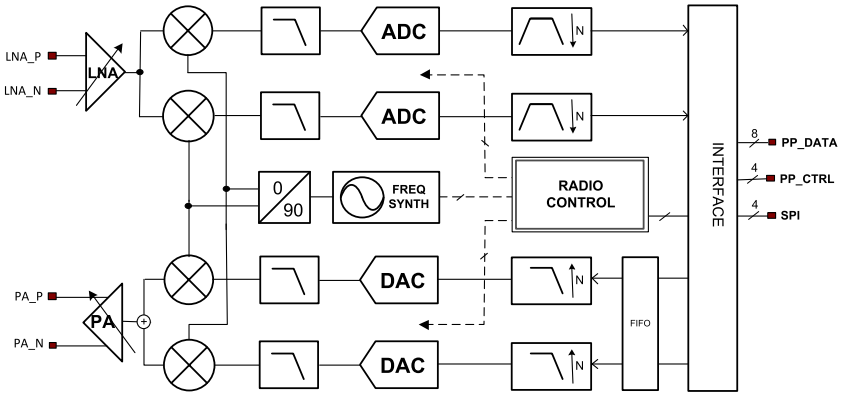


Figure 1-1. CC1260 Functional Block Diagram

Table of Contents

2 Revision History

Changes from Revision B (August 2014) to Revision C **Page**

- Added 863 to 876 MHz support 1
- Added 868-MHz frequency band to SDR systems 1
- Changed title of Section 4.3, *Recommended Operating Conditions* from *General Characteristics* 6
- Added Section 4.4, *Thermal Resistance Characteristics for RGZ Package* 6
- Added conditions to Section 4.6, *Current Consumption* 7
- Changed "The optional clock output is available in all modes except POWERDOWN and XOFF." to read "The optional clock output is always available unless the device is in POWERDOWN or XOFF mode." 20

3 Terminal Configuration and Functions

3.1 Pin Diagram

Figure 3-1 shows the pin designations for the CC1260 device.

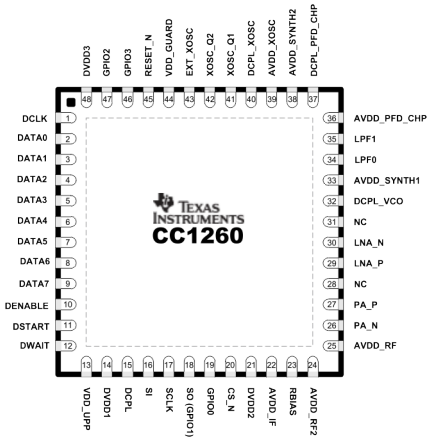


Figure 3-1. CC1260 48-Pin RGZ

3.2 Pin Attributes

Table 3-1 describes the CC1260 signals.

Table 3-1. Pin Attributes

PIN NUMBER	SIGNAL NAME	SIGNAL TYPE	DESCRIPTION
1	DCLK	Digital I/O	uPP interface clock
2	DATA0	Digital I/O	uPP interface data line
3	DATA1	Digital I/O	uPP interface data line
4	DATA2	Digital I/O	uPP interface data line
5	DATA3	Digital I/O	uPP interface data line
6	DATA4	Digital I/O	uPP interface data line
7	DATA5	Digital I/O	uPP interface data line
8	DATA6	Digital I/O	uPP interface data line
9	DATA7	Digital I/O	uPP interface data line
10	DENABLE	Digital I/O	uPP interface enable
11	DSTART	Digital I/O	uPP interface start
12	DWAIT	Digital output	uPP interface wait
13	VDD_UPP	Power	1.6- to 2.0-V VDD
14	DVDD1	Power	2.3- to 3.6-V VDD
15	DCPL	Power	Digital regulator output to external decoupling capacitor
16	SI	Digital input	Serial data in
17	SCLK	Digital input	Serial data clock
18	SO (GPIO1)	Digital I/O	Serial data out (General-purpose I/O)
19	GPIO0	Digital I/O	General-purpose I/O
20	CS_N	Digital input	Active-low chip select
21	DVDD2	Power	2.3- to 3.6-V VDD
22	AVDD_IF	Power	2.3- to 3.6-V VDD
23	RBIAS	Analog	External high-precision resistor
24	AVDD_RF2	Power	2.3- to 3.6-V VDD

Table 3-1. Pin Attributes (continued)

PIN NUMBER	SIGNAL NAME	SIGNAL TYPE	DESCRIPTION
25	AVDD_RF	Power	2.3- to 3.6-V VDD
26	PA_N	Analog	Differential TX output
27	PA_P	Analog	Differential TX output
28	NC		Not connected
29	LNA_P	Analog	Differential RX input
30	LNA_N	Analog	Differential RX input
31	NC		Not connected
32	DCPL_VCO	Power	Pin for external decoupling of VCO supply regulator
33	AVDD_SYNTH1	Power	2.3- to 3.6-V VDD
34	LPF0	Analog	External loop filter components
35	LPF1	Analog	External loop filter components
36	AVDD_PFD_CHP	Power	2.3- to 3.6-V VDD
37	DCPL_PFD_CHP	Power	Pin for external decoupling of PFD and CHP regulator
38	AVDD_SYNTH2	Power	2.3- to 3.6-V VDD
39	AVDD_XOSC	Power	2.3- to 3.6-V VDD
40	DCPL_XOSC	Power	Pin for external decoupling of XOSC supply regulator
41	XOSC_Q1	Analog	Crystal oscillator pin 1 (must be grounded if a TCXO or other external clock connected to EXT_XOSC is used)
42	XOSC_Q2	Analog	Crystal oscillator pin 2 (must be left floating if a TCXO or other external clock connected to EXT_XOSC is used)
43	EXT_XOSC	Digital input	Pin for external XOSC input (must be grounded if a regular XOSC connected to XOSC_Q1 and XOSC_Q2 is used)
44	VDD_GUARD	Power	2.3- to 3.6-V VDD
45	RESET_N	Digital input	Asynchronous, active-low digital reset
46	GPIO3	Digital I/O	General-purpose I/O (Default state: 20 MHz clock output)
47	GPIO2	Digital I/O	General-purpose I/O
48	DVDD3	Power	2.3- to 3.6-V VDD
–	GND	Ground pad	The ground pad must be connected to a solid ground plane.

4 Specifications

All measurements are performed on CC1260EM_FPGA R0.8 or on the production test platform. The test signal in TX (such as FSK and OFDM) is generated by an external FPGA.

4.1 Absolute Maximum Ratings

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage (VDD)		–0.3		3.9	V
Input RF level				+10	dBm
Voltage on digital pins (except uPP interface)		–0.3		VDD+0.3 max 3.9	V
Voltage on analog pins (including DCPL pins)		–0.3		2.0	V
Voltage on uPP interface (including VDD_UPP)		–0.3		2.0	V

4.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–40	+125	°C
V_{ESD}	Human body model (HBM) stress voltage, per ANSI/ESDA/JEDEC JS-01, all pins(1)	–2000	+2000	V
	Charged device model (CDM) ESD stress voltage, per JEDEC specification JESD22-C101, all pins(2)	–1000	+1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 2000 V may actually have higher performance.
(2) JEDEC document JEP155 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 1000 V may actually have higher performance.

4.3 Recommended Operating Conditions

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage supply range		2.3		3.6	V
uPP interface voltage		1.6		2.0	V
Temperature range		–40		105	°C

4.4 Thermal Resistance Characteristics for RGZ Package

NAME	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s)(3)
$R\theta_{JCT}$	Junction to case (top)	14.5	0.0
$R\theta_{JCB}$	Junction to case (bottom)	1.2	0.0
$R\theta_{JB}$	Junction to board	5.2	0.0
$R\theta_{JA}$	Junction to free air (high K)	28.3	0.0
Ψ_{JT}	Junction to package (top)	0.2	0.0
Ψ_{JB}	Junction to board	5.2	0.0

(1) °C/W = degrees Celsius per watt
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta-JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and changes based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Assumes power dissipation of 2 W and an ambient temperature of 70°C
(3) m/s = meters per second

4.5 RF Characteristics

T_A = 25°C, VDD = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz if nothing else stated

PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
Frequency bands			902		930	MHz
			863		876	MHz
Channel bandwidth	Minimum channel bandwidth is defined by DSP filtering and crystal tolerance. Bandwidths are scaled by the crystal frequency.	Receive			2	MHz
		Transmit			3	MHz

4.6 Current Consumption

T_A = 25°C, VDD = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz if nothing else stated

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Power down	Optional clock output not available		0.3	<1	µA
XOFF mode	Optional clock output not available		190		µA
IDLE mode			2.7		mA
RX current consumption	At 2 Msps sample rate		32		mA
TX current consumption:					mA
Transmitting FSK, +3 dBm			42		
Transmitting FSK, +10 dBm			48		
Transmitting FSK, max output power			57		

4.7 Receive Parameters

T_A = 25°C, VDD = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz if nothing else stated

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Noise figure: 1.6-MHz I/Q bandwidth (includes noise contribution from ADC)	RX calibration before entering RX required		6		dB
Noise figure: 2-MHz I/Q bandwidth (includes noise contribution from ADC)	RX calibration before entering RX required		7		dB
Noise figure: 200-kHz I/Q bandwidth centered around zero (includes noise contribution from ADC)	RX calibration before entering RX required		8		dB
	DC filter required		7		
Blocking/selectivity: Digital filter bandwidth of approximately 150 kHz with a Cascaded Integrator-Comb (CIC) filter decimation factor M = 64 and using minimum AAF bandwidth 3-dB signal-to-noise reduction	±400 kHz offset		–53		dBm
	±800 kHz offset		–44		
	±2 MHz offset		–36		
	±10 MHz offset		–33		
IIP2 (low-side/high-side)	At maximum gain		+33/+41		dBm
IIP3	At maximum gain		–16		dBm
	At minimum gain		+26		
1-dB compression point	Maximum gain		–30		dBm
	Minimum gain		+8		
ADC dynamic range	10-kHz bandwidth		90		dB
	1-MHz bandwidth		66		
	2-MHz bandwidth		60		
Cascaded receive gain	Maximum gain		43		dB
	Minimum gain		–43		
Cascaded gain accuracy			±1		dB
Cascaded receive gain step size			3		dB

Receive Parameters *(continued)*

T_A = 25°C, VDD = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz if nothing else stated

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
RX differential input impedance	At maximum gain		51 – j13		Ω
RX I/Q data sample rate: Maximum supported sample rate Minimum supported sample rate	The sample rate is configurable: $F_{SR} = \frac{F_{XTAL}}{M \times N}$ where M ϵ [4, 64] and N = 2 or 4, and are both integers		 5 0.16		MHz
Digital filter bandwidth	The digital filters are programmable (for more information, see Section 5.3, *Receiver*).	See Section 5.3, *Receiver*.			MHz
Anti-aliasing filter (AAF) –3-dB bandwidth (two-sided) Bandwidth setting 0b11 Bandwidth setting 0b10 Bandwidth setting 0b01 Bandwidth setting 0b00	The filters can be approximated as second-order Butterworth.		 3.4 1.5 1.0 0.6		MHz

4.8 Transmit Parameters

T_A = 25°C, VDD = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz if nothing else stated

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Maximum output power	TI recommends using the low-IF configuration if the CC1260 device outputs more than +3 dBm.		+13		dBm
Maximum (average) output power, OFDM	Assuming 10-dB peak-to-average ratio		+3		dBm
1-dB compression point	At maximum output power setting		+12		dBm
Minimum average output power	Assuming 10-dB peak-to-average ratio		–32		dBm
Output power step size	Using gain control only		3		dB
	Using both gain control and digital adjustment in TX digital-to-analog converters (DACs) to reduce output power		< 0.1		dB
Transmit EVM_{RMS}: Zero IF transmitter configuration, with calibration Zero IF transmitter configuration, without calibration	Measured using OFDM 802.15.4g option 3 MCS level 6, transmitted at +3 dBm		 –29 –25		dB

Transmit Parameters *(continued)*

T_A = 25°C, VDD = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz if nothing else stated

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
TX spurious emissions/channel leakage power (excluding harmonics):					dBc
Low IF transmitter configuration	Requires TX calibration				
> 1-MHz offset	Measured using OFDM 802.15.4g option 3 MCS level 6 transmitted at +3 dBm, sampled at 5 MHz over uPP interface		–29		
> 15-MHz offset			–71		
Zero IF transmitter configuration:					
0.4-MHz offset	Emissions are measured in 100-kHz bandwidth and presented in dBc relative to carrier power level.		–51		
0.5-MHz offset			–60		
0.8-MHz offset	TI recommends using the low-IF configuration if the CC1260 device outputs more than +3 dBm.		–64		
≧ 1.2-MHz offset			–66		
≧ 2-MHz offset			–68		
≧ 5.7-MHz offset, except spurs at ±40 MHz offset			–74		
			–71		
Harmonics:	Continuous wave transmitted at +3 dBm				dBm
Second harmonic			–28		
Third harmonic			–46		
Analog filter –3-dB bandwidth (two-sided):	The filters are programmable with a 4-bit range and can be approximated as 2nd order Butterworth.				MHz
Maximum programmable bandwidth			20		
Minimum programmable bandwidth			4.6		
Digital intermediate frequency (IF):	The analog filter bandwidth should be adjusted according to the IF.				MHz
Setting 0			0		
Setting 1			2.5		
Setting 2			5		
TX I/Q data sample rate:	The sample rate of the data sent to the CC1260 must be equal to: $F_{SR} = \frac{F_{XTAL}}{P}$ where $P \in [4, 128]$ and is an integer				MHz
Maximum supported sample rate			10		
Minimum supported sample rate			0.3		
TXDAC clock frequency	The CC1260 device performs first-order upsampling of the I/Q data to the DAC clock frequency.		40		MHz
TX optimum load impedance	The differential load impedance that the CC1260 device must see for best performance		140+j95		Ω
TX source impedance	The differential source impedance represented by the CC1260 device (at +10 dBm)		41-j291		Ω

4.9 Frequency Synthesizer

T_A = 25°C, VDD = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz if nothing else stated

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Frequency resolution			30		Hz
Phase noise	±10-kHz offset		–101		dBc/Hz
	±100-kHz offset		–102		dBc/Hz
	±1-MHz offset		–123		dBc/Hz

4.10 Wake-Up and Timing

T_A = 25°C, VDD = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz if nothing else stated

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Powerdown to IDLE	Depends on crystal		0.2		ms
IDLE to RX	Excluding calibration time		122		µs
IDLE to TX	Excluding calibration time		122		µs
RX/TX turnaround	Excluding calibration time		40		µs
PLL calibration			0.2		ms
RX AGC gain control settling time, at maximum bandwidth	Settling within 0.1% of final value, excluding propagation delay through digital RX filters.		2		µs
Propagation delay through RX digital filters. At maximum bandwidth (M = 4) and maximum FIR length.	Delay in seconds given by: $\text{Delay} = M \times \frac{\text{FIR\_LENGTH} + 12}{2 \times F_{XTAL}}$ where M ϵ [4, 64] and is identical to the RX sample rate M, and FIR_LENGTH is 29, 57, or 85		5		µs
SPI interface SCLK maximum read access frequency			10		MHz
SPI interface SCLK maximum write access frequency			10		MHz

4.11 Crystal Oscillator

T_A = 25°C, VDD = 3.3 V

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Crystal frequency	A significant increase in noise figure at multiples of the crystal frequency is expected.	38.4		40	MHz
Load capacitance (C_L)			10		pF
ESR	Simulated over operating conditions			60	Ω

4.12 Clock Output

T_A = 25°C, VDD = 3.3 V

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Clock output frequency	A significant increase in noise figure at multiples of the clock output frequency is expected.		XOSC/2		MHz
Output high voltage	Assuming a load capacitance of 15 pF or less	0.8 × Vdd			V
Output low voltage				0.2 × Vdd	V
Integrated jitter, from 1 kHz			1		ps

4.13 Clock Input (TCXO)

T_A = 25°C, VDD = 3.3 V if nothing else stated

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Clock frequency		38.4		40	MHz
Clock input amplitude (peak-to-peak)(1)	Must not exceed supply voltage. Signal must be AC-coupled. The recommended value is 18 pF.	0.8		VDD	V
Clock source phase noise: ± 10-kHz offset ± 100-kHz offset	Required to avoid degradation of CC1260 phase noise		 <–140 <–145		dBc/Hz
Input capacitance			1.5		pF

(1) Simulated over operating conditions

4.14 General I/O (GPIO, SPI, and RESET_N Pin)

T_A = 25°C, VDD = 3.3 V

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Logic input high voltage		0.8 × VDD			V
Logic input low voltage				0.2 × VDD	V
Logic output high voltage		0.8 × VDD			V
Logic output low voltage				0.2 × VDD	V

4.15 uPP Interface

T_A = 25°C, VDD = 3.3 V, VDD uPP interface = 1.8 V, assuming 5-pF load on pins when uPP interface outputs data

PARAMETER	CONDITION	MIN	u	Max	UNIT
uPP interface input high voltage			1.1		V
uPP interface input low voltage			0.7		V
uPP interface output high rise time	uPP interface uses slew-rate limited drivers to minimize disturbance in RX.(1)		11		ns
uPP interface output low fall time			11		ns
uPP interface output clock rate	Data sampled on both edges of clock			10	MHz
uPP interface input clock rate	Data sampled on both edges of clock			20	MHz

(1) The rise and fall time is specified from 0.3 to 1.5 V, assuming a 5-pF load and maximum configured I/O drive strength.

4.16 Temperature Sensor

VDD = 3.3 V

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Temperature sensor accuracy: Calibrated(1) Uncalibrated			 5 26		°C
Temperature sensor range		–40		105	°C
Output slope			103		ADC samples/°C

(1) Requires initial offset to be measured at room temperature and subtracted from measurements

4.17 Voltage Sensor

T_A = 25°C

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage sensor accuracy: Calibrated(1) Uncalibrated			 12 300		mV
Voltage sensor range		2.3		3.6	V
Output slope			15		ADC samples/mV

(1) Requires initial offset to be measured at 3.3 V and subtracted from measurements

4.18 Typical Characteristics

T_A = 25°C, V_{DD} = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz

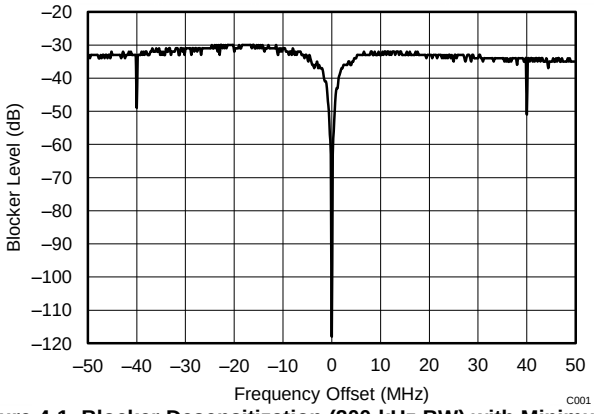


Figure 4-1. Blocker Desensitization (200-kHz BW) with Minimum AAF Bandwidth. Blocker Level at Which the Noise Figure Increases by 3 dB

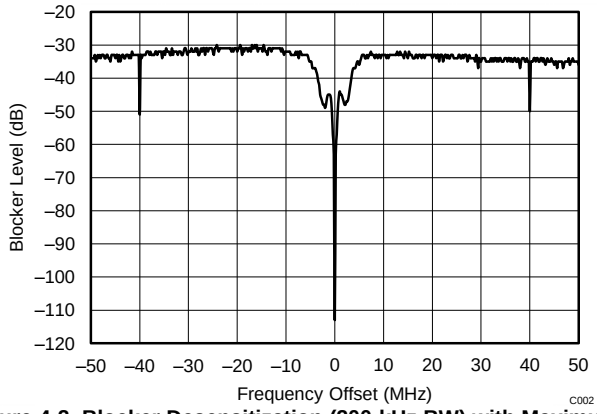


Figure 4-2. Blocker Desensitization (200-kHz BW) with Maximum AAF Bandwidth. Blocker Level at Which the Noise Figure Increases by 3 dB

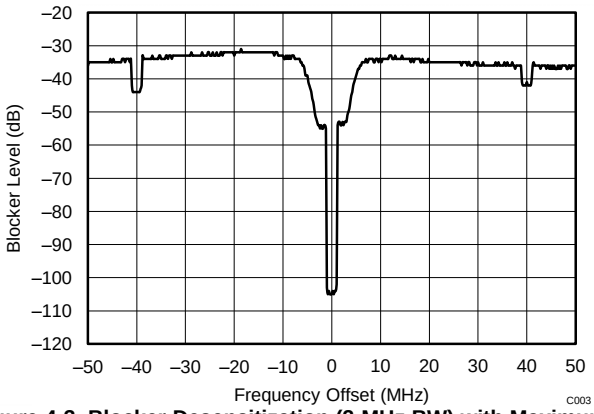
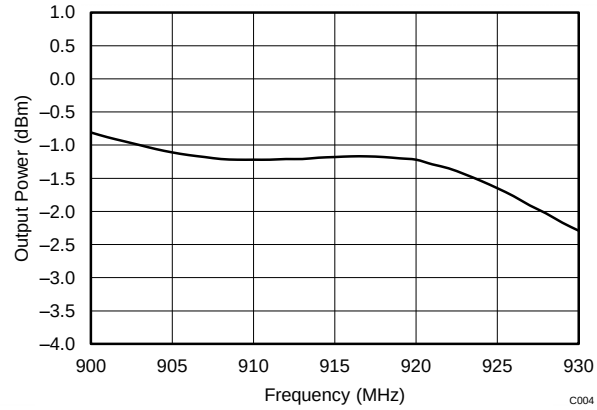
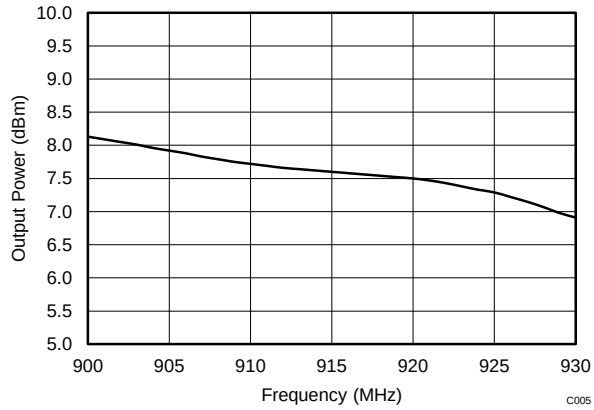


Figure 4-3. Blocker Desensitization (2-MHz BW) with Maximum AAF Bandwidth. Blocker Level at Which the Noise Figure Increases by 3 dB



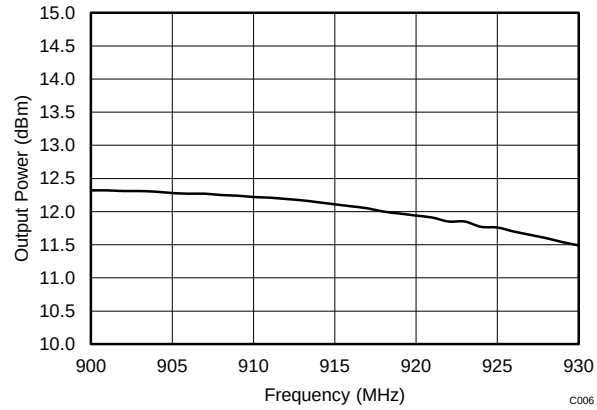
PA Setting = 0x36

Figure 4-4. TX Output Power vs Frequency



PA Setting = 0x76

Figure 4-5. TX Output Power vs Frequency

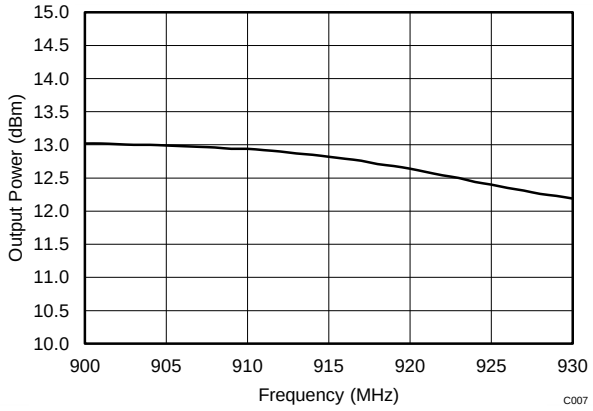


PA Setting = 0xB6

Figure 4-6. TX Output Power vs Frequency

Typical Characteristics *(continued)*

T_A = 25°C, V_{DD} = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz



PA Setting = 0xBF

Figure 4-7. TX Maximum Output Power vs Frequency

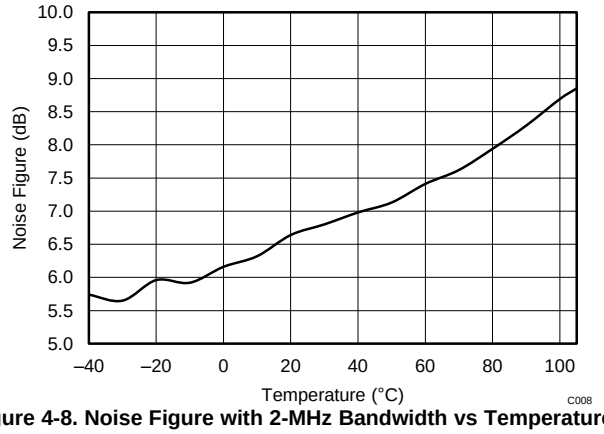


Figure 4-8. Noise Figure with 2-MHz Bandwidth vs Temperature

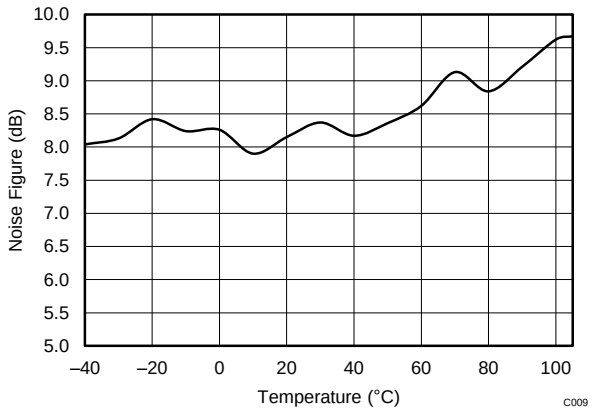
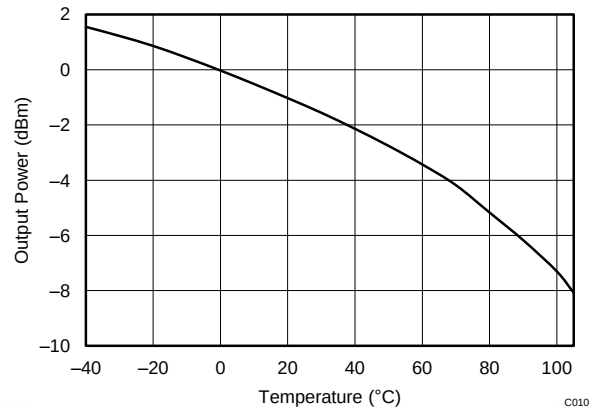
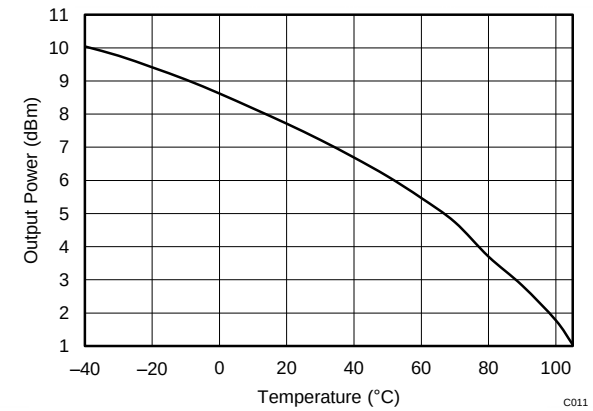


Figure 4-9. Noise Figure with 200-kHz Bandwidth vs Temperature



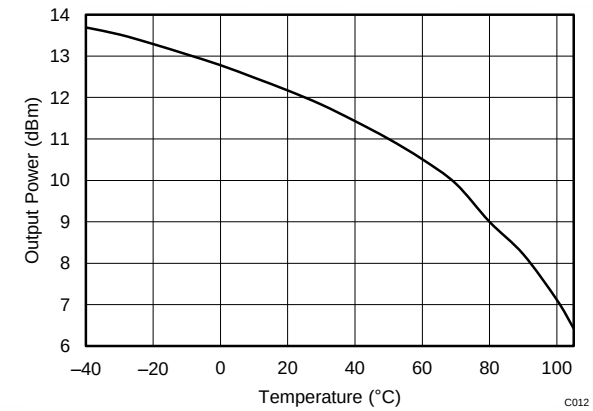
PA Setting = 0x36

Figure 4-10. TX Output Power vs Temperature



PA Setting = 0x76

Figure 4-11. TX Output Power vs Temperature



PA Setting = 0xB6

Figure 4-12. TX Output Power vs Temperature

Typical Characteristics *(continued)*

T_A = 25°C, V_{DD} = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz

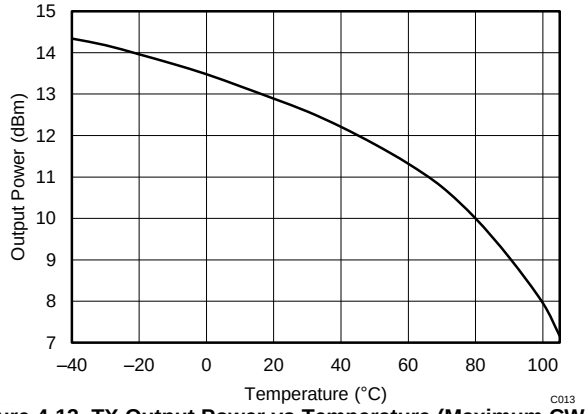


Figure 4-13. TX Output Power vs Temperature (Maximum CW Output Power)

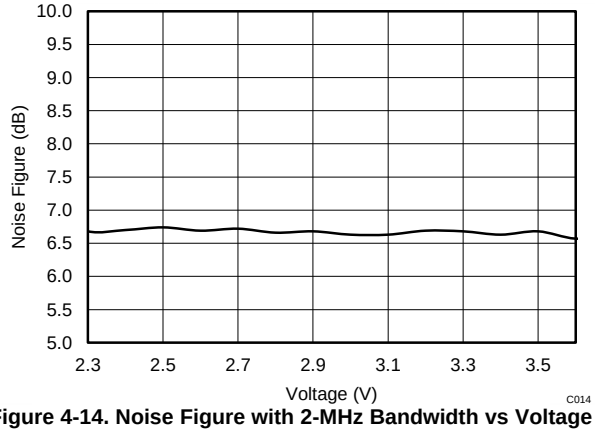


Figure 4-14. Noise Figure with 2-MHz Bandwidth vs Voltage

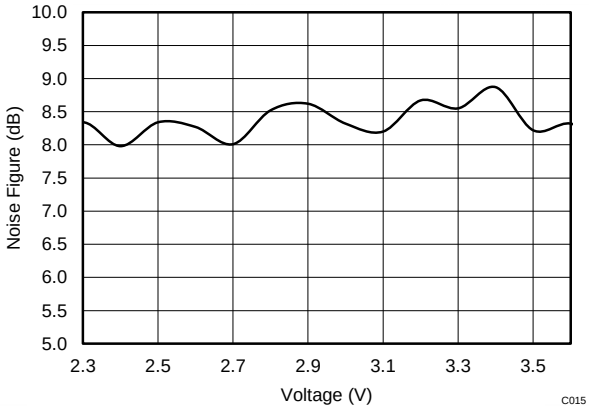
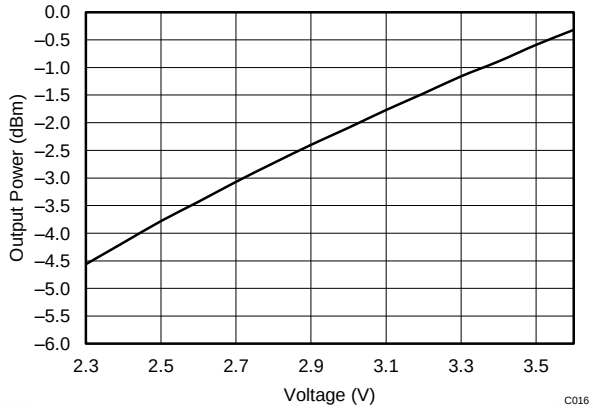
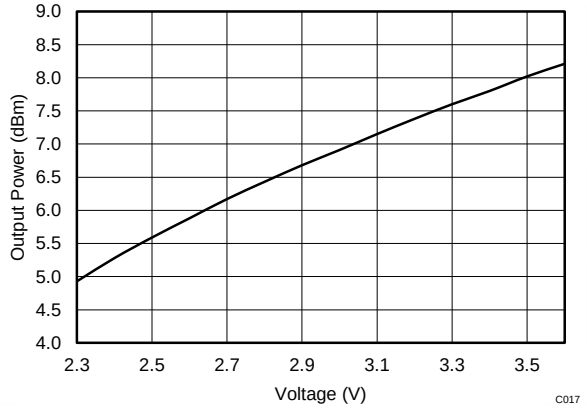


Figure 4-15. Noise Figure with 200-kHz Bandwidth vs Voltage



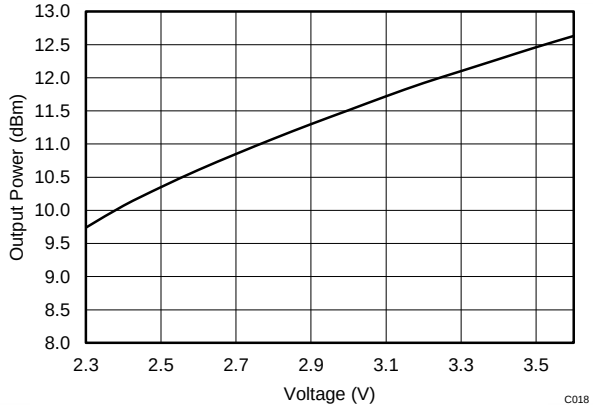
PA Setting = 0x36

Figure 4-16. TX Output Power vs Voltage



PA Setting = 0x76

Figure 4-17. TX Output Power vs Voltage

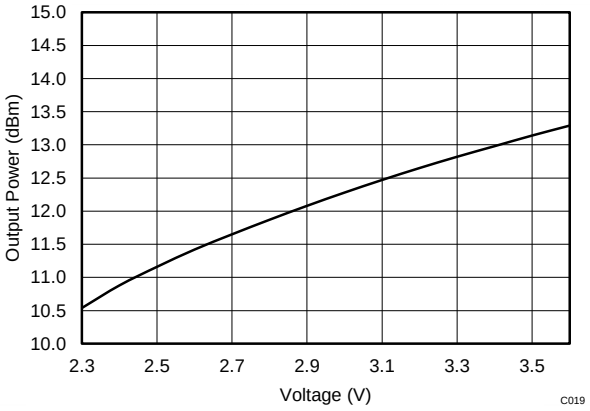


PA Setting = 0xB6

Figure 4-18. TX Output Power vs Voltage

Typical Characteristics *(continued)*

T_A = 25°C, V_{DD} = 3.3 V, f_c = 915 MHz, f_{xtal} = 40 MHz



PA Setting = 0xBF

Figure 4-19. TX Maximum Output Power vs Voltage

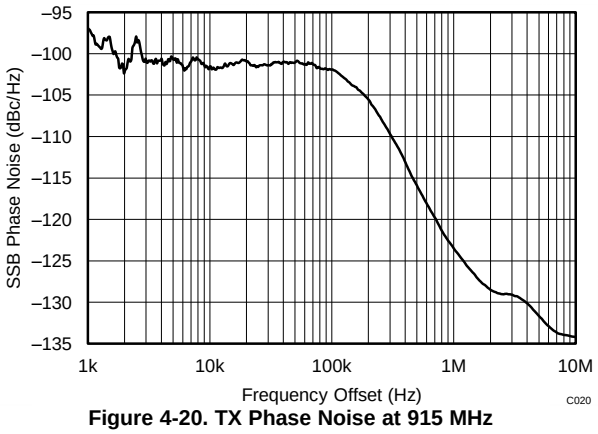


Figure 4-20. TX Phase Noise at 915 MHz

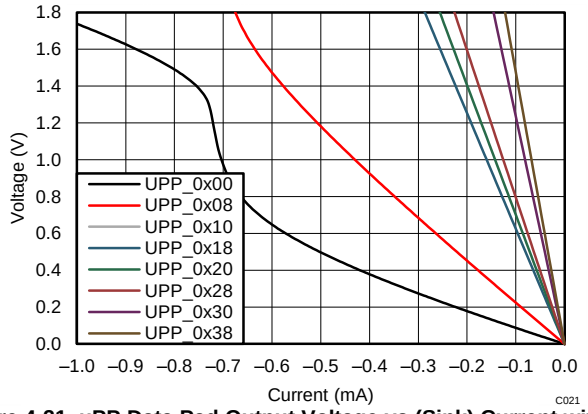


Figure 4-21. uPP Data Pad Output Voltage vs (Sink) Current with Pad Set Low (Values for Different uPP Register Setting

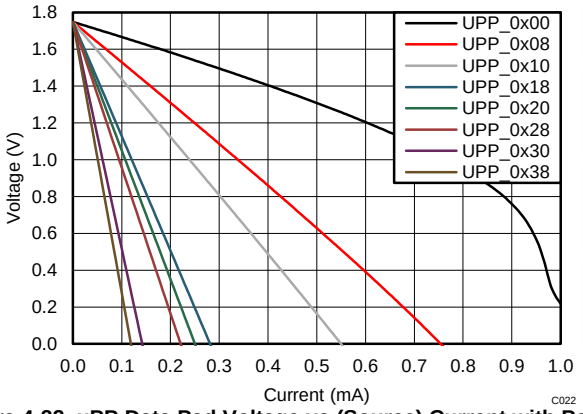


Figure 4-22. uPP Data Pad Voltage vs (Source) Current with Pad Set High (Values for Different uPP Register Settings)

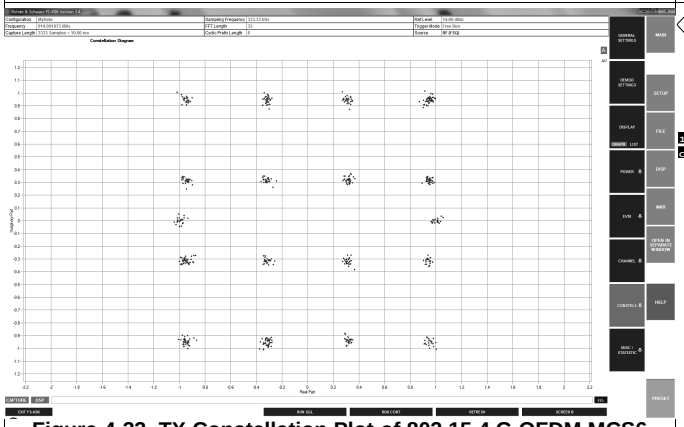


Figure 4-23. TX Constellation Plot of 802.15.4.G OFDM MCS6 Option 3, Generated by an External FPGA and Transmitted by the CC1260 at +3-dBm Average Output Level

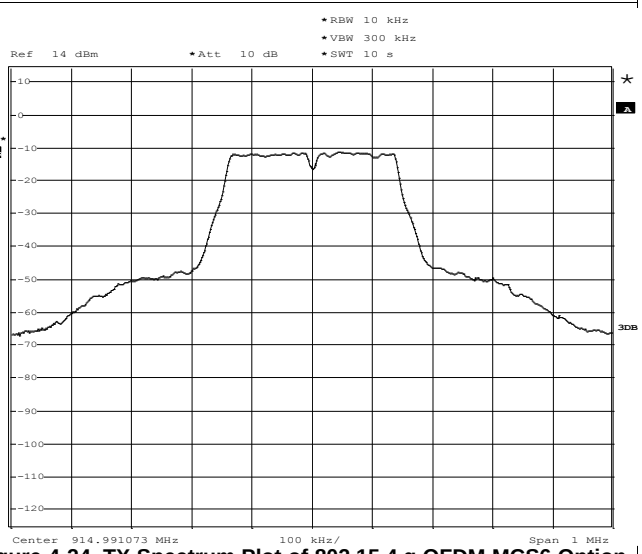


Figure 4-24. TX Spectrum Plot of 802.15.4.g OFDM MCS6 Option 3, Generated by an External FPGA and Transmitted by the CC1260 at +3-dBm Average Output Level

5 Detailed Description

5.1 Functional Block Diagram

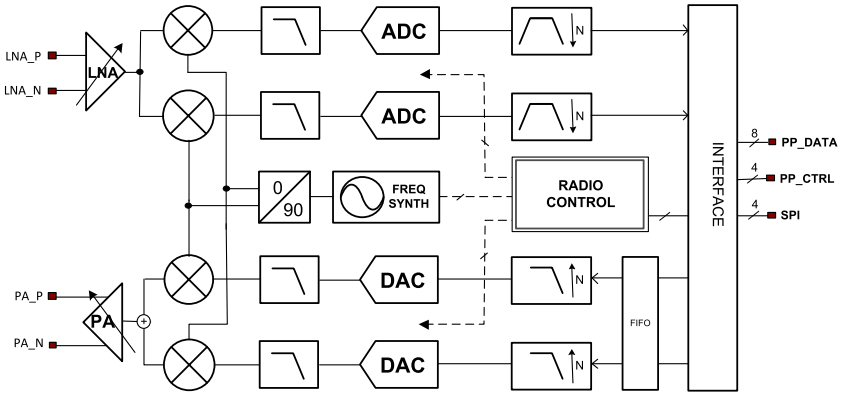


Figure 5-1. CC1260 Functional Block Diagram

5.2 Frequency Synthesizer

At the heart of CC1260 device is a fully integrated, fractional-N, ultra-high performance frequency synthesizer. The frequency synthesizer is designed for excellent phase noise performance, giving very high selectivity and blocking performance. The system is designed to comply with the most stringent regulatory spectral masks at maximum transmit power. A crystal can be connected to XOSC_Q1 and XOSC_Q2, or a TCXO can be connected to the external clock input. The oscillator generates the reference frequency for the synthesizer, as well as clocks for the analog-to-digital converters (ADCs) and the digital part. If a TCXO is used, the CC1260 device automatically turns the TCXO on and off when required to support low-power modes. The CC1260 device provides an optional clock output that can be used as the clock reference for the DSP. The optional clock signal is derived from the main reference clock on the CC1260 device.

5.3 Receiver

The CC1260 device features a high-performance direct-conversion receiver with programmable high-order digital filters. The received RF signal is amplified by the low-noise amplifier (LNA), down-converted in quadrature, filtered, and the I/Q signals are digitized by the high dynamic range ADCs. Automatic gain control (AGC) and RSSI functions are shared between the CC1260 device and the DSP.

5.3.1 Receiver Decimation and Filtering

To remove blockers and ADC quantization noise, the CC1260 device performs decimation and filtering of the received signal in two steps:

1. The signal passes through a programmable CIC decimation filter.
2. Additional filtering occurs in a programmable FIR filter (see Figure 5-2).

In the second step, the sample rate is decimated by a factor of 2 or 4. Section 4, *Specifications*, includes formulas for calculating the sample rate.

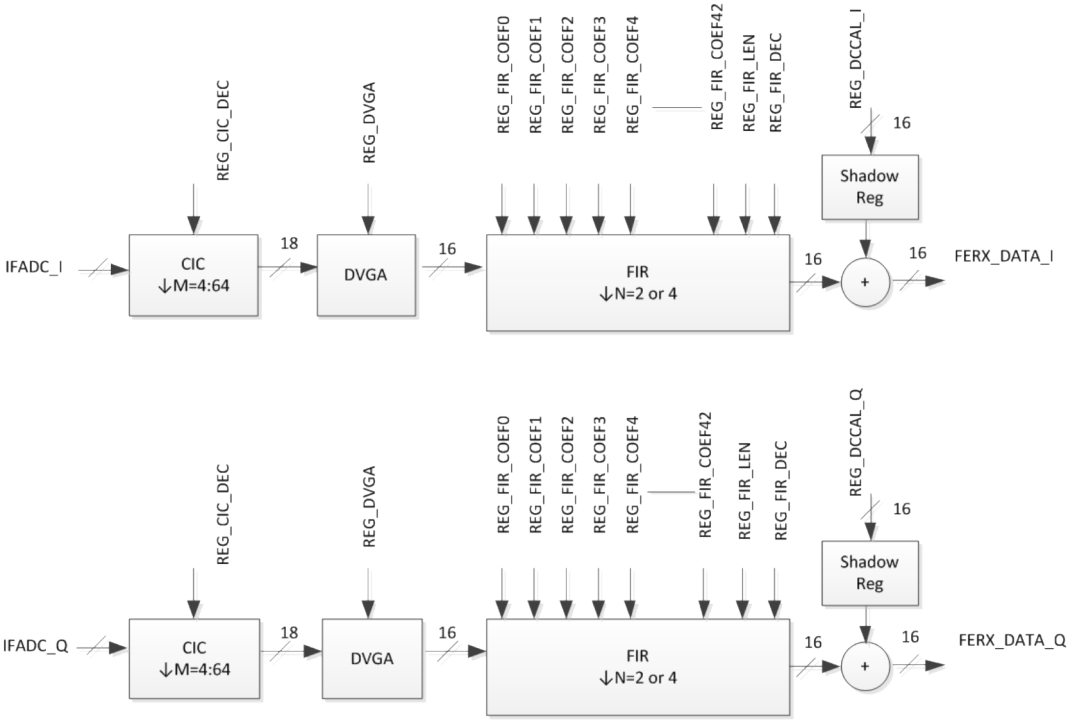


Figure 5-2. RX Digital Signal Processing

Figure 5-3 shows the CIC filter characteristics decimated by 5.

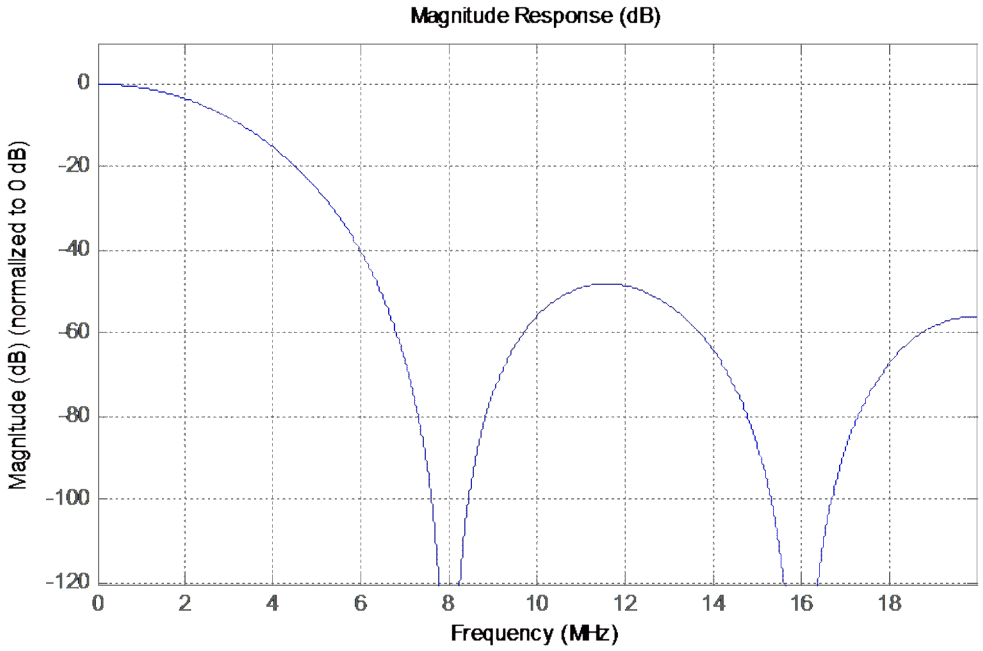


Figure 5-3. CIC Filter Characteristic Decimated by 5 (One-Sided)

5.3.2 Programmable FIR Filter

The FIR filters are programmable filters with odd length and even symmetry, and are implemented as polyphase filters with the option to decimate by either 2 or 4. The filter length is configurable as either 29, 57, or 85. The sum of the coefficients must be normalized, that is, the sum of the coefficients must be equal to 215 because the signal is represented as 16-bit signed.

5.3.3 DC Offset Correction

The CC1260 device includes hardware support for subtraction of DC error on I and Q. The subtraction value is stored in a shadow register, which allows byte-wise updating of DC calibration values and simultaneous enabling of all values using the SPI. The DC correction values are enabled when writing to the low byte of the DC calibration registers (for more information, see Section 6.2.4, *RX Calibration*).

5.4 Transmitter

The I/Q RF front end of the CC1260 device employs a linear quadrature up-conversion topology. The modulated I and Q data are passed from the DSP (or equivalent implementation) to the CC1260 device using a parallel interface tailored to fit seamlessly with TI DSPs, and then are upsampled to the system clock through first-order interpolation. The CC1260 transmitter, which comprises quadrature DACs, smoothing filters, an I/Q modulator, and a power amplifier (PA), converts the baseband data to the appropriate RF channel of operation. The output power is programmable with a fine step to enable accurate network power optimization.

Figure 5-4 shows a block diagram of the TX digital processing.

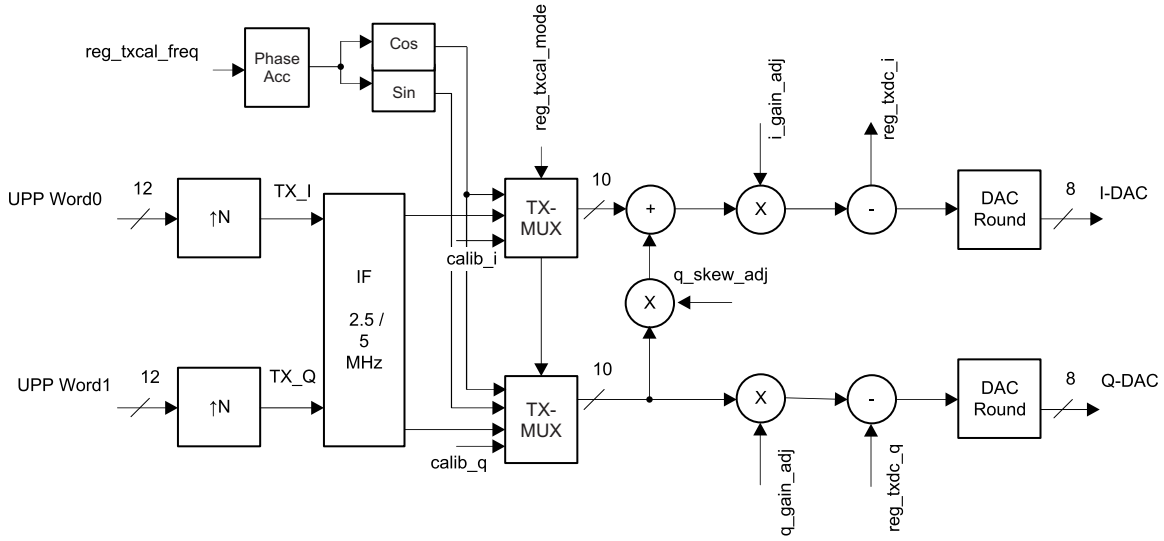


Figure 5-4. TX Digital Processing

5.4.1 Intermediate Frequency (Low IF, Zero IF)

The CC1260 device supports a transmitter intermediate frequency of 0, ±2.5, and ±5 MHz. Using an IF means that spurious emissions and noise due to transmitter non-idealities, such as I/Q mismatch, are pushed outside the signal bandwidth, resulting in improved EVM at the cost of increased power leak at the adjacent channel.

For the best EVM, using an IF (of either ±2.5 MHz or ±5 MHz) is recommended (and is referred to as *low IF*); applications that must meet strict spectral masks should use zero IF. The low-IF topology, which is less sensitive to injection pulling of the internal VCO by the PA, is recommended for systems targeting high-transmit output power from the CC1260 device.

5.4.2 Upsampling

Data sent to the CC1260 device through the uPP interface is upsampled from the uPP rate to the TX DAC clock frequency using a first-order Farrow interpolator (see Figure 5-5). Only integer upsampling rates are supported.

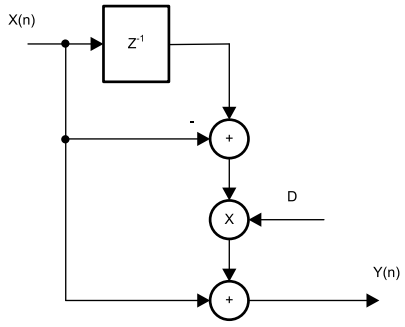


Figure 5-5. TX Upsampler

5.4.3 I/Q Correction

The CC1260 device includes hardware support for estimation and correction of the I/Q phase and gain mismatch and DC offset in the transmitter (for more information, see Section 6.2.2, *TX Calibration of I/Q Mismatch and DC Offset*).

5.5 Radio Control and User Interface

The CC1260 digital control system is built around the main radio control (MARC), which handles power modes and radio sequencing. A 4-wire protocol viewer serial interface is used for configuration.

5.5.1 Device States and Power Modes

The CC1260 device supports power modes in addition to the RX and TX modes:

- POWERDOWN: POWERDOWN has the lowest power consumption, longest start-up time, and no access to registers.
- XOFF: XOFF offers quicker start-up times but uses more current.
- IDLE: The radio is disabled. The clock is still running, registers can be accessed, strobe commands can be sent, and the external clock output is available. IDLE allows quick transition to RX or TX.
- TX_CAL: Allows access to dedicated system hardware which enables calibration of device imbalances and offsets

The optional clock output is always available unless the device is in POWERDOWN or XOFF mode. SPI commands provide transition between the different device states.

Figure 5-6 shows a simplified state diagram.

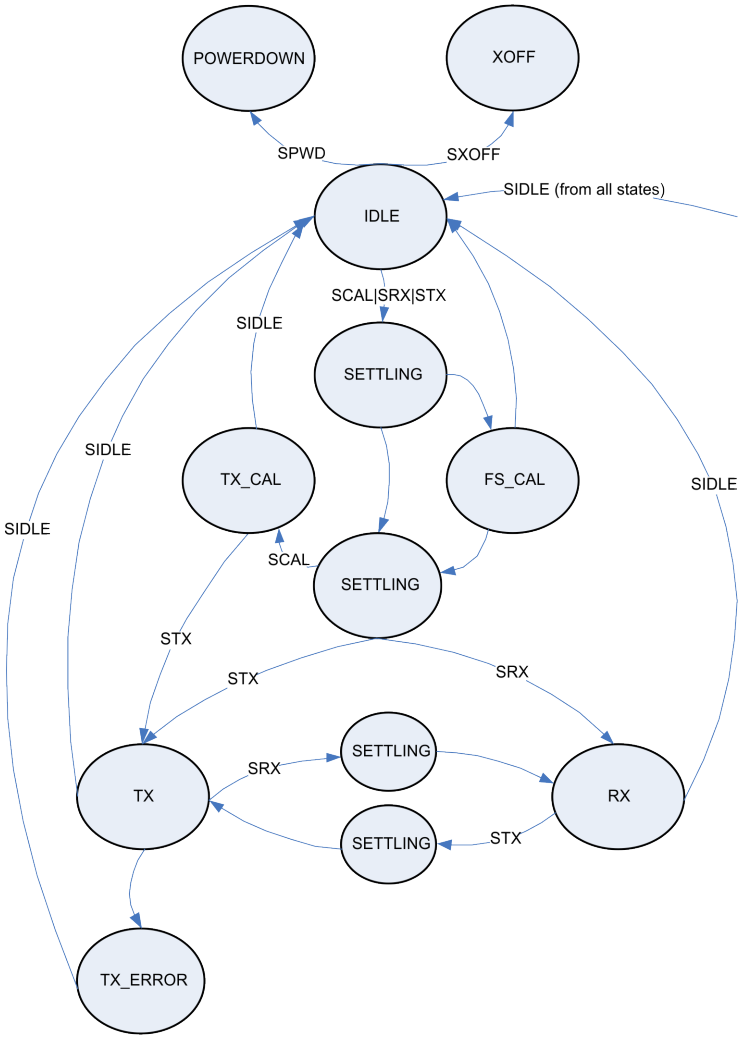


Figure 5-6. Simplified State Diagram

5.5.2 uPP Interface

The uPP interface is a source-synchronous parallel interface that transmits or receives (when the CC1260 device is in RX or TX, respectively) a continuous stream of words using both edges of the clock (DCLK). The 8-bit words are formatted into 4-word frames that encapsulate one complex 16-bit sample. DSTART indicates the start of each frame.

To minimize switching noise, all output lines (including the clock line) are slew-rate limited when the CC1260 device is in RX.

To avoid overflows when the CC1260 device is in TX, a 32-byte TX data FIFO is implemented and the DWAIT flow control signal indicates to the baseband processor that no data will be accepted in the following clock cycle. DWAIT is ignored when the CC1260 device is in RX.

The device enters the TX_ERROR state if the uPP interface is not handled correctly during TX.

Figure 5-7 and Figure 5-8 show the RX and TX data parallel interface waveforms, respectively.

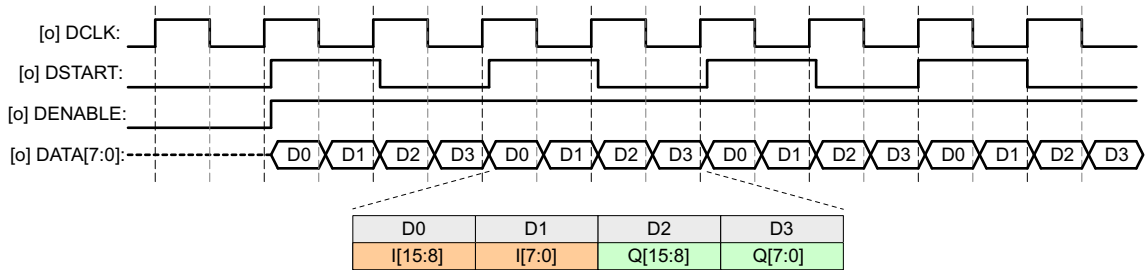


Figure 5-7. RX Data Parallel Interface Waveform

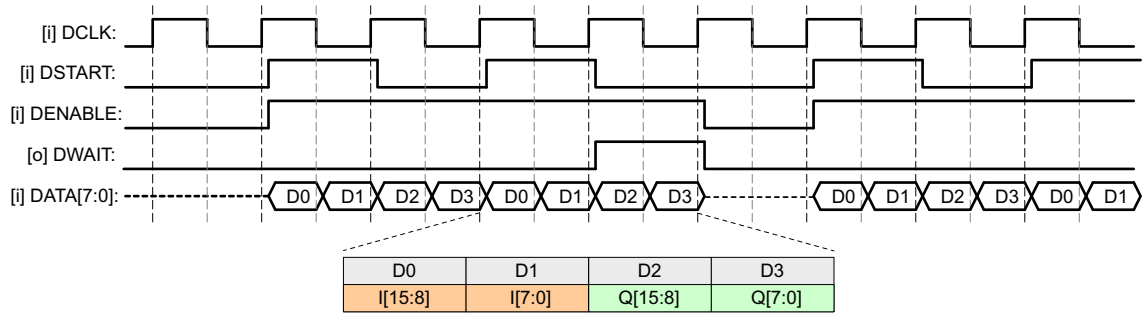


Figure 5-8. TX Data Parallel Interface Waveform

5.5.3 SPI Radio Control Interface

A 4-wire SPI slave interface allows access to internal hardware registers and allows posting of commands to the radio control state machine that controls the operating state of the device (see Figure 5-6).

6 Applications, Implementation, and Layout

6.1 Typical Application

Figure 6-1 shows a typical application circuit using the CC1260 device as a single-chip radio transceiver.

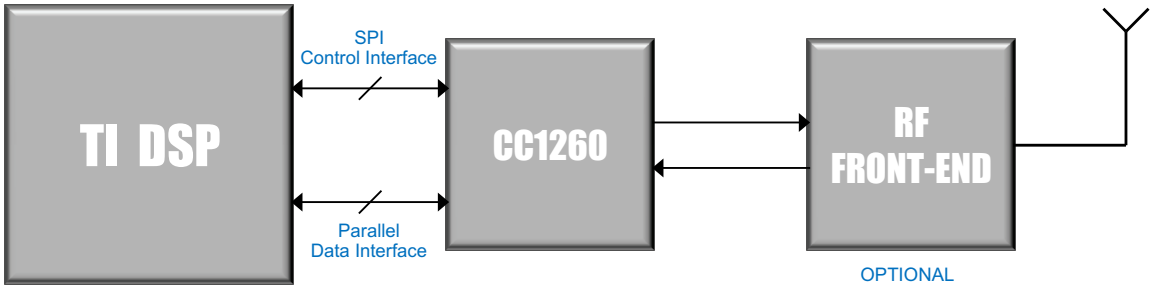


Figure 6-1. Typical Application Circuit Using CC1260 Device as a Single-Chip Radio Transceiver

6.2 Calibration

The CC1260 device includes hardware support for device calibration.

The calibration is split into four categories:

- Synthesizer calibration (see Section 6.2.1, *PLL Calibration (FS_CAL)*)
- TX calibration (see Section 6.2.2, *TX Calibration of I/Q Mismatch and DC Offset*)
- PA gain calibration (see Section 6.2.3, *PA Gain Calibration*)
- RX calibration (see Section 6.2.4, *RX Calibration*)

The synthesizer calibration steps are performed automatically when entering RX or TX, unless the device is configured to do otherwise. TX and RX calibration must be performed manually.

6.2.1 PLL Calibration (FS_CAL)

Calibration of the synthesizer must meet the specified frequency accuracy and phase noise. Nevertheless, if a calibration has been performed recently and a significant change in frequency is not required, calibration of the synthesizer can be skipped to save time and power consumption.

The CC1260 device can be configured to perform the PLL calibration automatically before entering TX or RX.

6.2.2 TX Calibration of I/Q Mismatch and DC Offset

TX calibration can be performed with the assistance of dedicated hardware included on the CC1260 device. This hardware enables accurate measurement of gain and phase imbalance as well as LO leakage, made on the fly without requiring RF measurement equipment.

6.2.3 PA Gain Calibration

In addition to TX I/Q mismatch and DC offset calibration, gain calibration must be performed to meet EVM specifications and to reduce variation in output power. An initial calibration is required to remove differences from part to part, as well as to make adjustments due to temperature and voltage changes.

The initial gain calibration must use an external RF power detector or similar equipment. To make adjustments due to temperature and voltage changes, the temperature and voltage sensors included on the CC1260 device, or elsewhere in the system, can be used.

6.2.4 RX Calibration

RX calibration of the DC offset present in the device is required for applications sensitive to low-frequency noise. Because this offset varies slowly over time, an RX calibration should be performed before entering RX to derive the best possible noise figure. External RF equipment is not required for the RX calibration.

7 Device and Documentation Support

7.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

7.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.4 Glossary

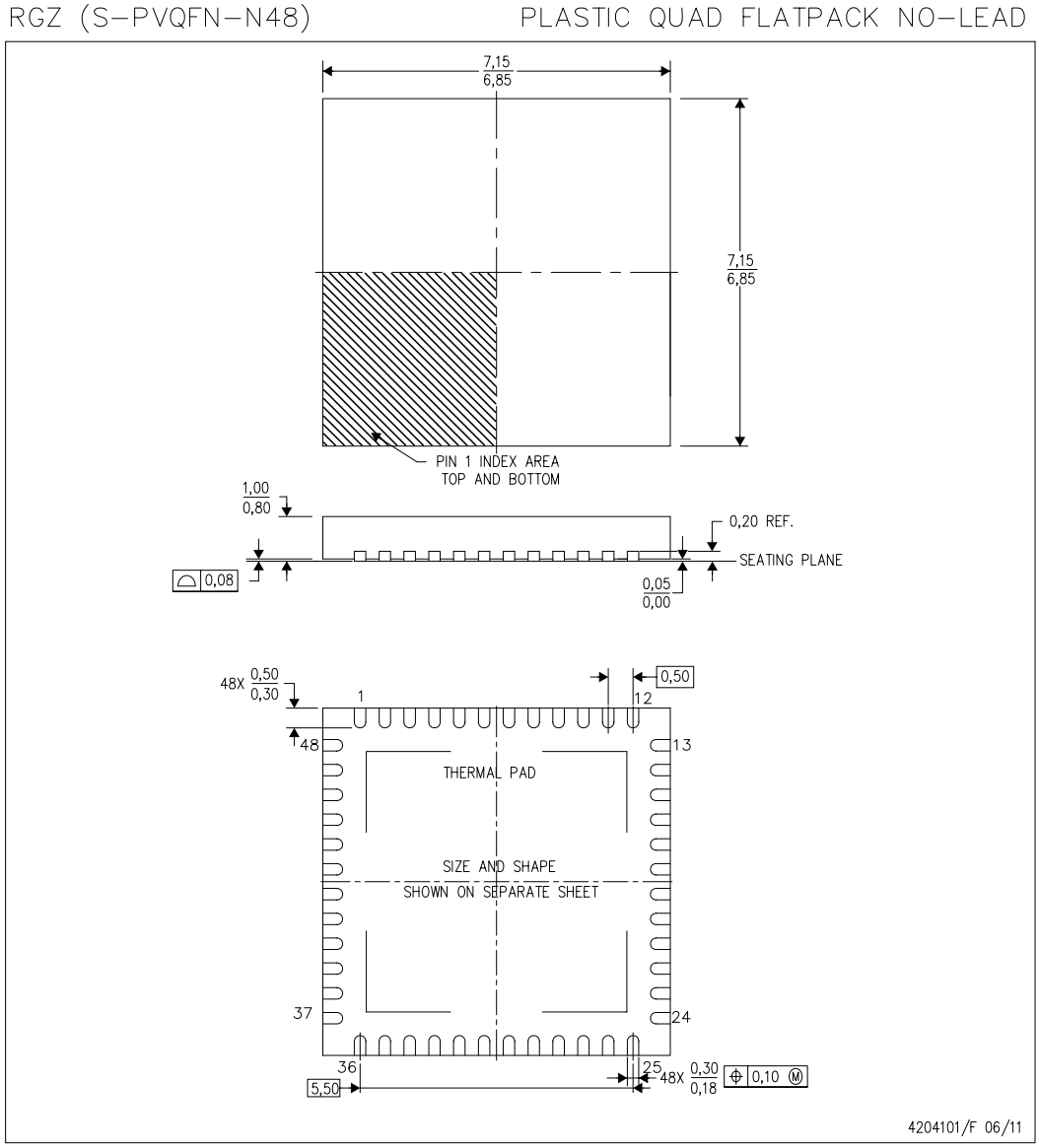
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

This section contains mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

8.1 VQFN Mechanical Data



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

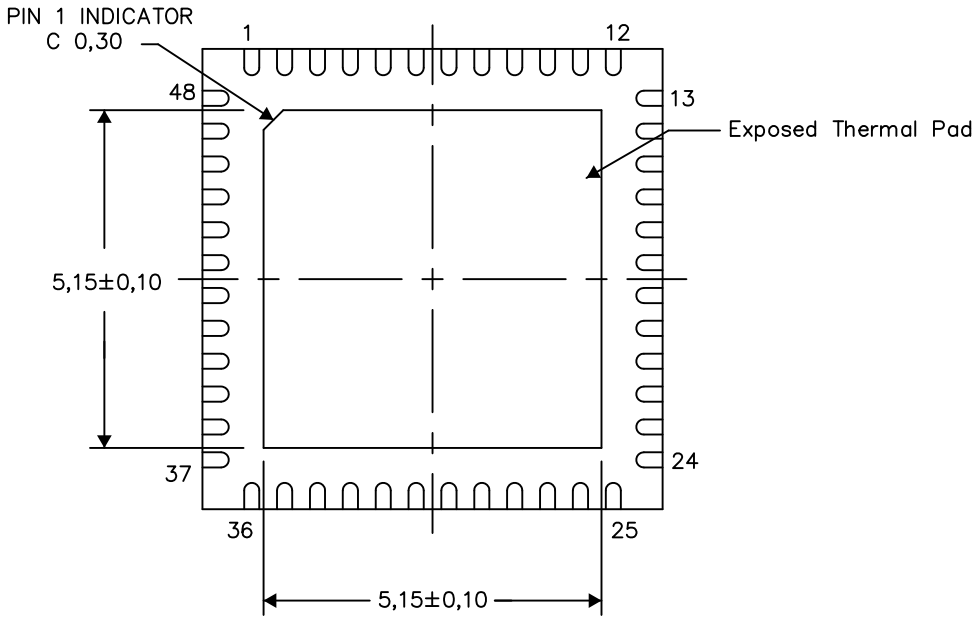
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



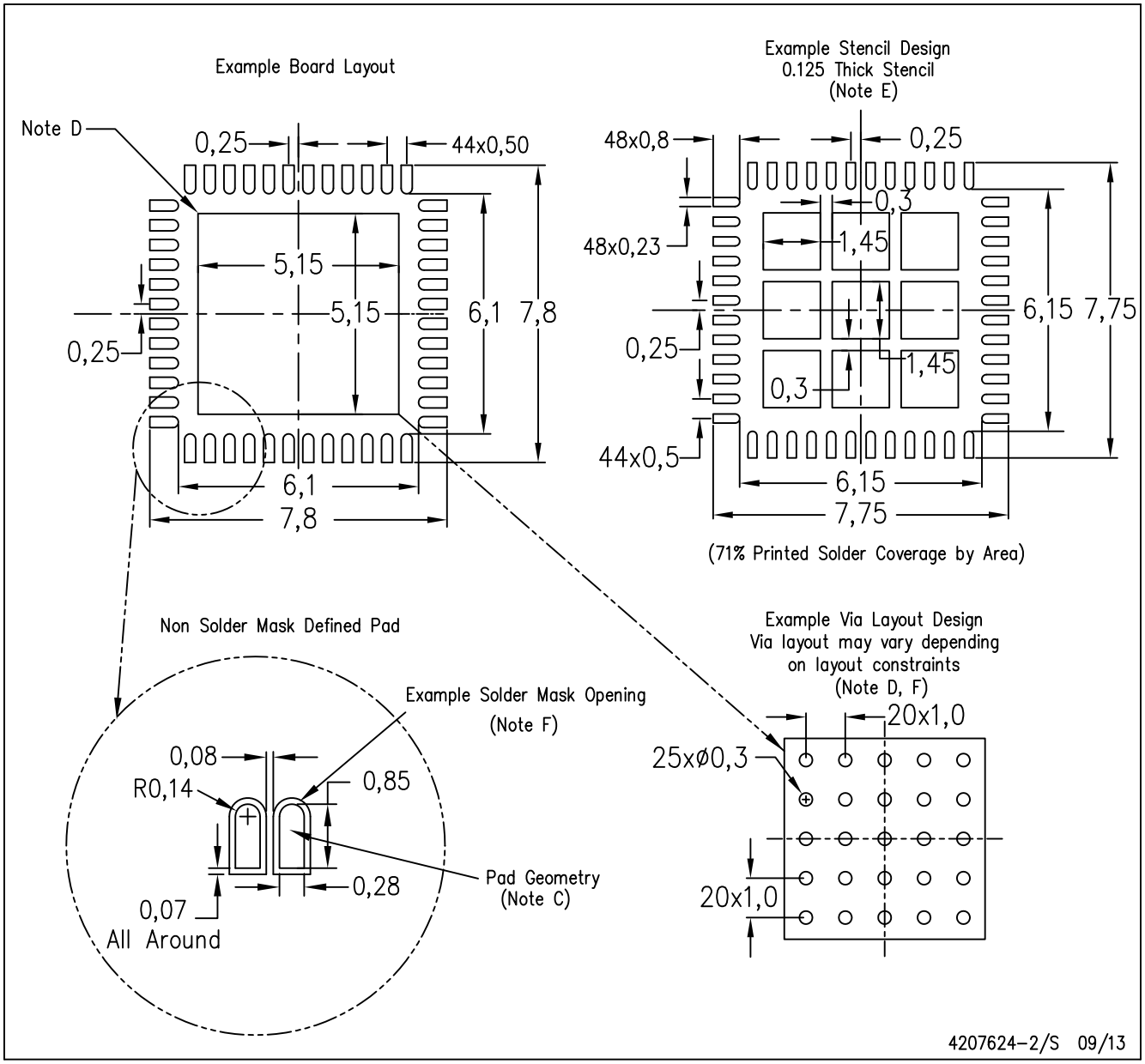
Bottom View

Exposed Thermal Pad Dimensions

4206354–2/X 01/14

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

8.2 Tape and Reel Dimensions

Figure 8-1 shows the tape and reel dimensions.

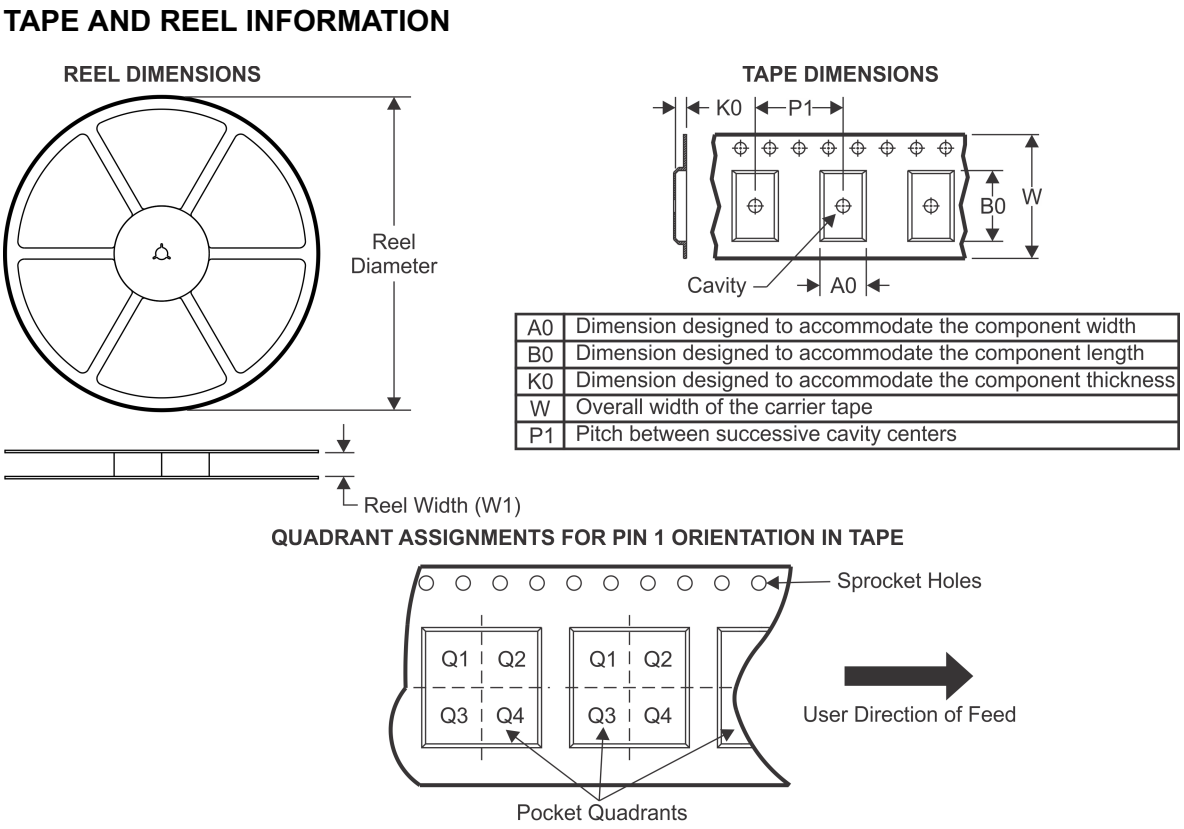


Figure 8-1. Tape and Reel Dimensions

Table 8-1 lists the measurements of the tape and reel dimensions.

Table 8-1. Tape and Reel Dimension Measurements

DEVICE	PKG.	PKG. DWG.	PINS	SPQ	REEL DIA. (mm)	REEL WIDTH W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN 1 QUAD.
CC1260RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CC1260RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

Figure 8-2 shows the dimensions of the tape and reel box.

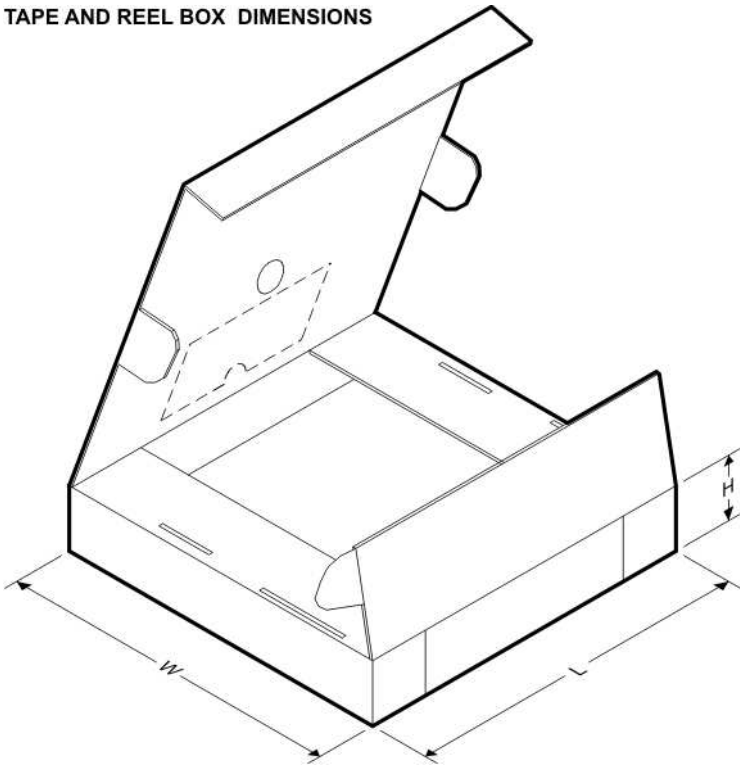


Figure 8-2. Tape and Reel Box Dimensions

Table 8-2 lists the measurements of the tape and reel box dimensions.

Table 8-2. Measurements of the Tape and Reel Box Dimensions(1)

DEVICE	PACKAGE	PACKAGE DRAWING	PINS	SPQ	LENGTH (mm)	WIDTH (mm)	HEIGHT (mm)
CC1260RGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
CC1260RGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

(1) All dimensions are nominal measurements.

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