Integrated Device Technology, Inc.

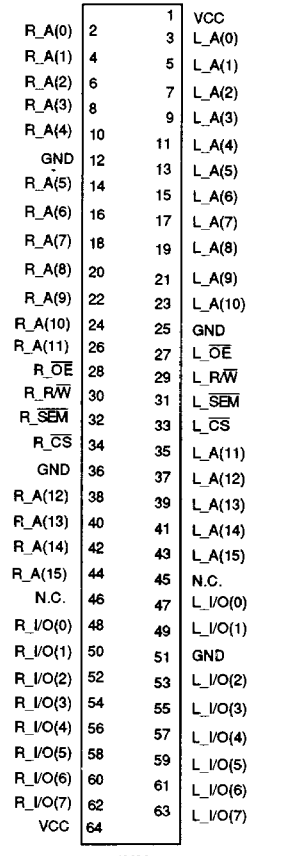
128K/64K x 8 CMOS DUAL-PORT STATIC RAM MODULE

PRELIMINARY
IDT7MP1021
IDT7MP1023

FEATURES

- High density 1M/512K CMOS dual-port static RAM modules
- Fast access times: 25, 30, 35, 40, 50ns
- Fully asynchronous read/write operation from either port
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted plastic components on a 64-lead SIMM (Single In-line Memory Module)
- Multiple Vcc and GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Input/outputs directly TTL compatible

PIN CONFIGURATION



SIMM TOP VIEW

2839 drw 01

DESCRIPTION:

The IDT7MP1021/1023 is a 128K/64K x 8 high-speed CMOS dual-port static RAM module constructed on a multi-layer FR-4 substrate using decode logic and either eight IDT7006 (16K x 8) dual-port RAMs for the 7MP1021 or four IDT7006s for the 7MP1023.

The IDT7MP1021/1023 provide two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via semaphore ($\overline{SEM}$) "handshake" signaling. The IDT7MP1021/1023 modules are designed to be used as stand-alone dual-port RAMs where on-chip hardware port arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7MP1021/1023 modules are packaged on a 64-lead multilayer FR-4 SIMM (Single In-line Memory Module). Maximum access times as fast as 25ns over the commercial temperature range are available.

All inputs and outputs of the IDT7MP1021/1023 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

PIN NAMES

Left Port	Right Port	Description
L_A (0–15)	R_A (0–15)	Address Inputs
L_I/O (0–7)	R_I/O (0–7)	Data Inputs/Outputs
L_R/$\overline{W}$	R_R/$\overline{W}$	Read/Write Enables
L_$\overline{CS}$	R_$\overline{CS}$	Chip Select
L_$\overline{OE}$	R_$\overline{OE}$	Output Enable
L_$\overline{SEM}$	R_$\overline{SEM}$	Semaphore Control
Vcc		Power
GND		Ground

2839 tbl 01

NOTE:
1. For the IDT7MP1023 (64K x 8) version, Pins 45 & 46 must be connected to GND for proper operation of the module. These pins become L_A(16) and R_A(16) respectively for the IDT7MP1021 (128K x 8) version.

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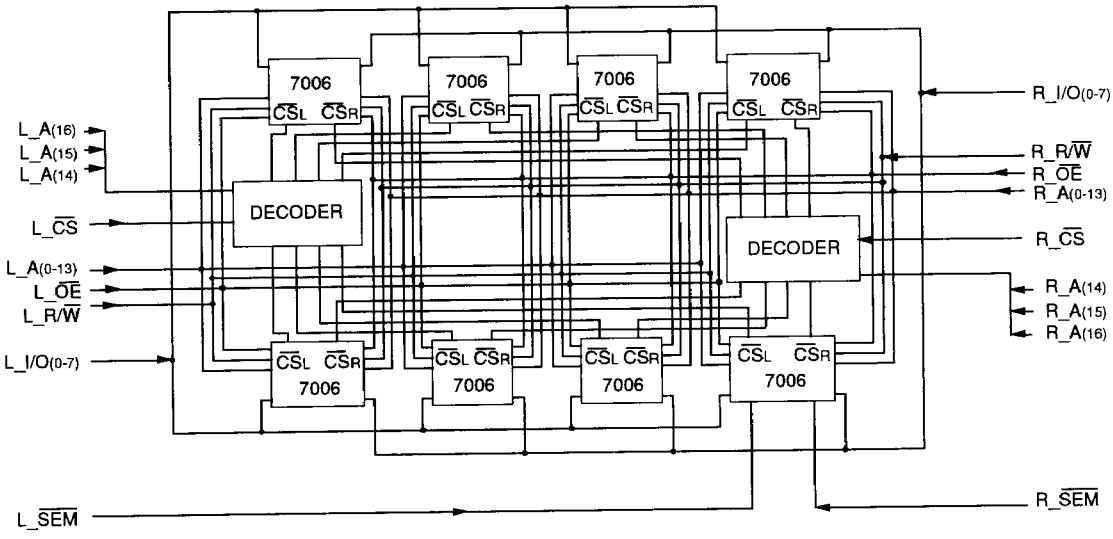
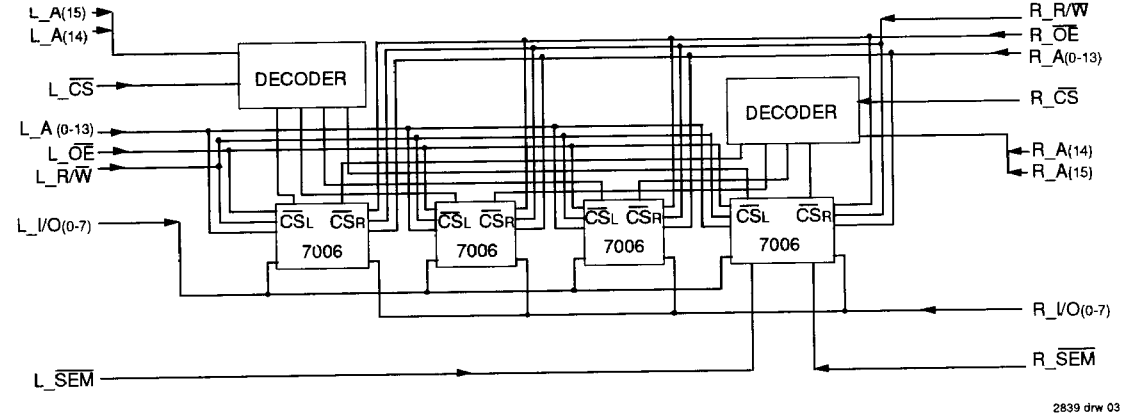
FUNCTIONAL BLOCK DIAGRAM

7MP1021



2839 drw 02

7MP1023



2839 drw 03

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2839 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	Max.	Unit
C_{IN1}	Input Capacitance ($\overline{CS}$ or $\overline{SEM}$)	V_{IN} = 0V	15	pF
C_{IN2}	Input Capacitance (Data, Address, All Other Controls)	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacifance (Data)	V_{OUT} = 0V	100	pF

NOTE:
2839 tbl 03
1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2839 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	-	0.8	V

2839 tbl 05

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A =0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MP1021/1023 Min.	IDT7MP1021/1023 Max.[1]	IDT7MP1021/1023 Max.[2]	Unit
I_{CC2}	Dynamic Operating Current (Both Ports Active)	V_{CC} = Max., $\overline{CS} \le V_{IL}$, $\overline{SEM} \ge V_{IH}$ Outputs Open, f = f_{MAX}	—	940	660	mA
I_{CC1}	Standby Supply Current (One Port Active)	V_{CC} = Max., L_$\overline{CS}$ or R_$\overline{CS} \ge V_{IH}$ Outputs Open, f = f_{MAX}	—	750	470	mA
I_{SB1}	Standby Supply Current (TTL Levels)	V_{CC} = Max., L_$\overline{CS}$ and R_$\overline{CS} \ge V_{IH}$ Outputs Open, f = f_{MAX} L_$\overline{SEM}$ and R_$\overline{SEM} \ge V_{CC}$ –0.2V	—	565	285	mA
I_{SB2}	Full Standby Supply Current (CMOS Levels)	L_$\overline{CS}$ and R_$\overline{CS} \ge V_{CC}$ –0.2V $V_{IN} > V_{CC}$ 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM} \ge V_{CC}$ –0.2V	—	125	65	mA

NOTES:
2839 tbl 06
1. For IDT7MP1021 (128K x 8) version only.
2. For IDT7MP1023 (64K x 8) version only.

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DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = 0°C to +70°C)

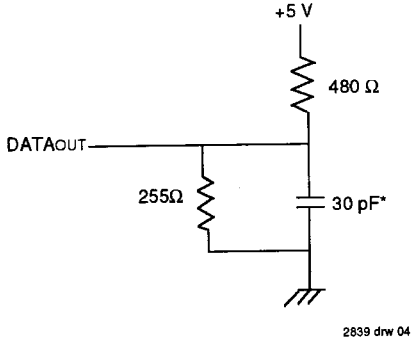
Symbol	Parameter	Test Conditions	IDT7MP1021		IDT7MP1023		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage (Address, Data & Other Controls)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	80	—	40	µA
$\|I_{LI}\|$	Input Leakage ($\overline{CS}$ and $\overline{SEM}$)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	80	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4		2.4	—	V

2839 tbl 07

AC TEST CONDITIONS

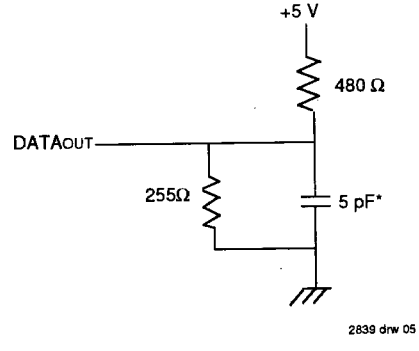
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2839 tbl 08



2839 drw 04

Figure 1. Output Load



2839 drw 05

Figure 2. Output Load
(for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

*Including scope and jig.

7-11-4

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP1023SxxM, 7MP1021SxxM										Unit
		-25[5]		-30[5]		-35[6]		-40		-50		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	50	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	—	50	ns
t_{ACS}[2]	Chip Select Access Time	—	25	—	30	—	35	—	40	—	50	ns
t_{OE}	Output Enable Access Time	—	13	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	12	—	15	—	15	—	15	—	ns
Write Cycle												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	50	—	ns
t_{CW}[2]	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	35	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	18	—	20	—	20	—	20	—	25	ns
t_{OW}[1, 4]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	13	—	15	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	13	—	15	—	15	—	15	—	ns
Port-to-Port Delay Timing												
t_{WDD}[6]	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	—	70	ns
t_{DDD}[6]	Write Data Valid to Read Data Valid	—	35	—	40	—	45	—	50	—	55	ns

2839 tbl 09

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1}= 0 if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR}= 5ns, t_{DH}= 5ns, t_{OW}= 5ns.
5. Preliminary specifications only.
6. Port-to-Port delay through the RAM cells from the writing port to the reading port.

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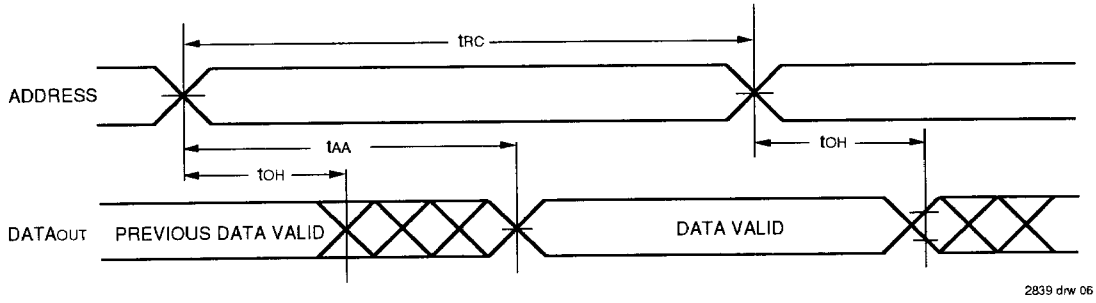
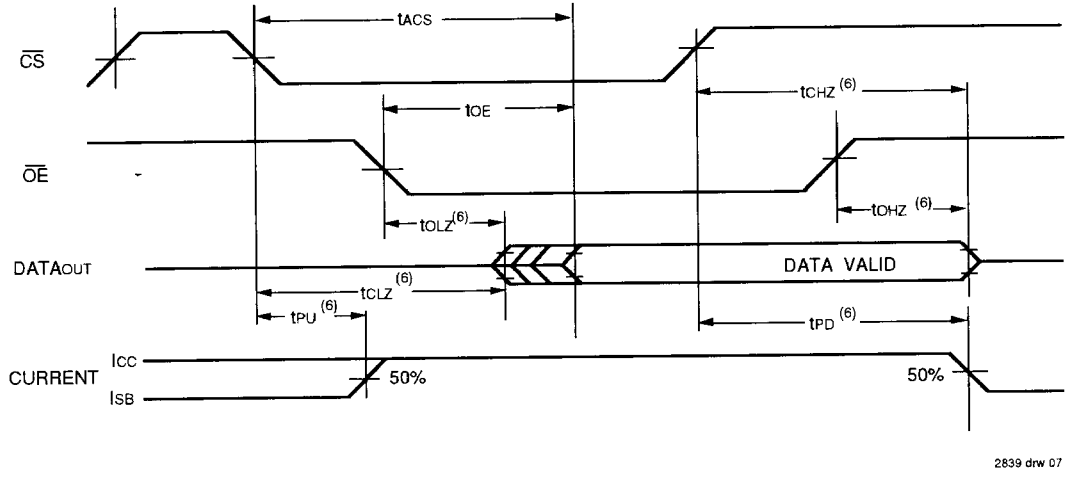
7-11-5

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)(1,2,4)



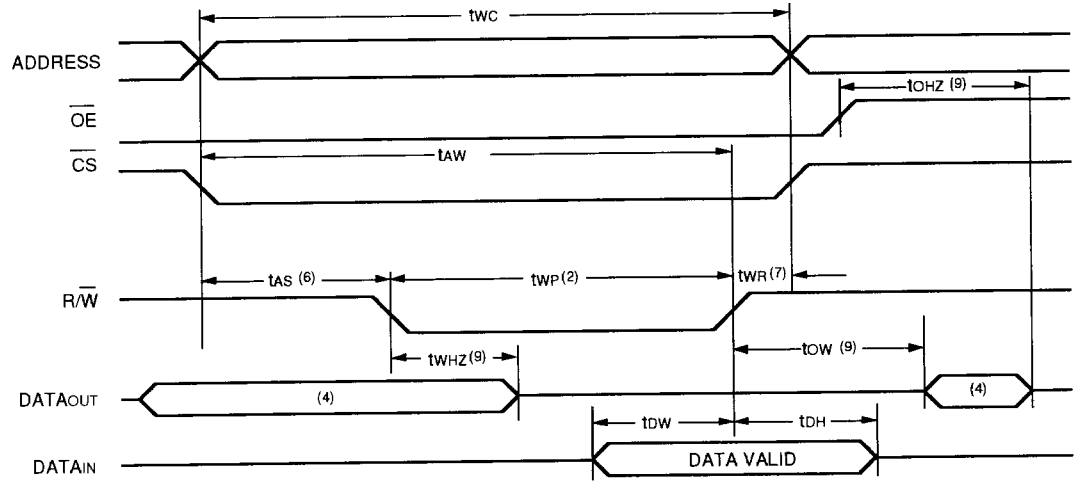
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)(1,3,5)



NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. This parameter is guaranteed by design but not tested.

7-11-6

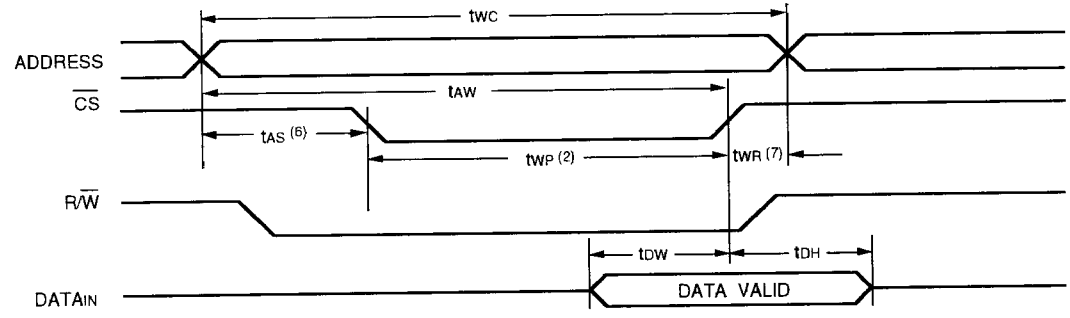
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1,3,5,8)



2839 drw 08

NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is Low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,3,5,8)

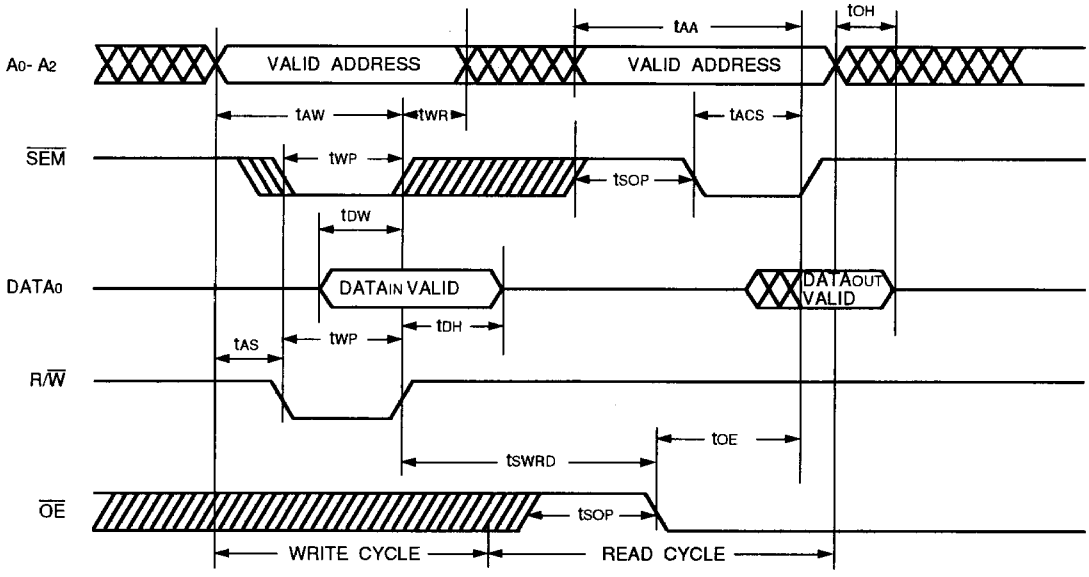


2839 drw 09

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a Low $\overline{CS}$ and a Low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

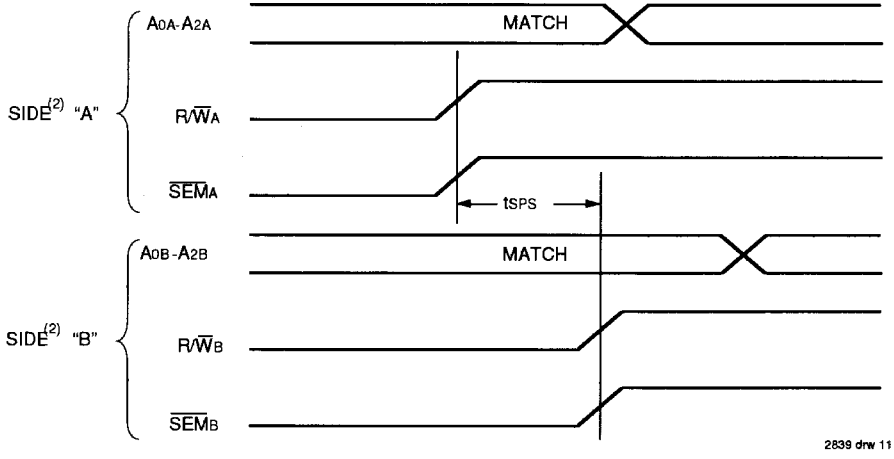
1-11-7

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING (EITHER SIDE)(1)



NOTE:
1. $\overline{CS}$ = High for the duration of the above timing (both write and read cycle).

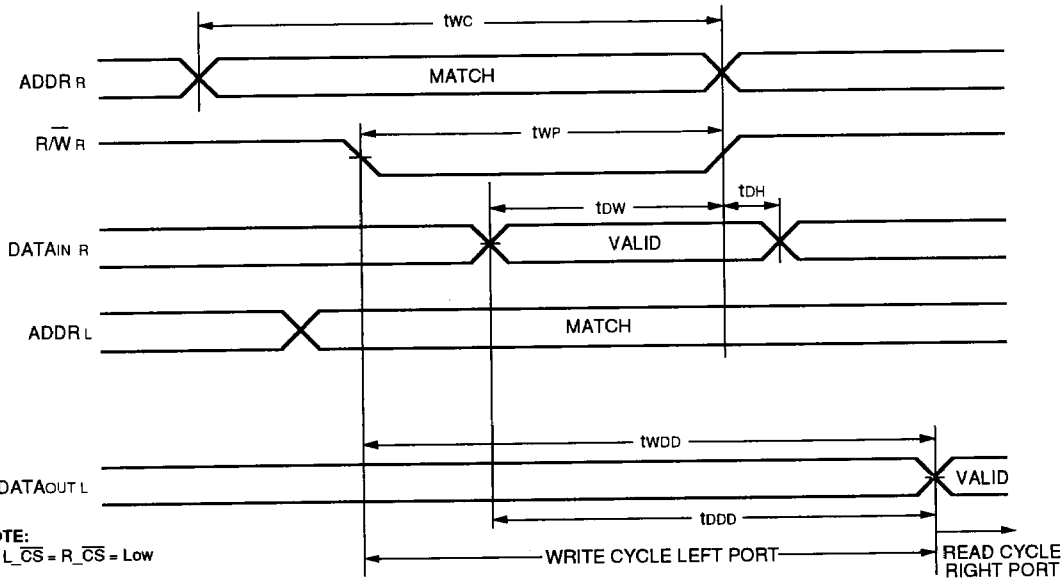
TIMING WAVEFORM OF SEMAPHORE CONTENTION(1,3,4)



NOTES:
1. D_{0R} = D_{0L} = Low, L_$\overline{CS}$ = R_$\overline{CS}$ = High. Semaphore Flag is released form both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going High to R/$\overline{W}_B$ or $\overline{SEM}_B$ going High.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

7-11-8

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY(1)



NOTE:
1. L_CS = R_CS = Low

2839 drw 12

TRUTH TABLES

TABLE I: NON-CONTENTION READ/WRITE CONTROL(1)

Inputs(1)				Outputs	
CS	R/W	OE	SEM	I/O0 - I/O7	Mode
H	X	X	H	Hi-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read from Memory
X	X	H	X	Hi-Z	Outputs Disabled

2839 tbl 10

NOTE:
1. AOL — A12 ≠ AOR — A12R

TABLE II: SEMAPHORE READ/WRITE CONTROL(1)

Inputs				Outputs	
CS	R/W	OE	SEM	I/O0 - I/O7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
X	↓	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2839 tbl 11

NOTE:
1. AOL — A12 ≠ AOR — A12R

SEMAPHORE OPERATION

For more details regarding semaphores & semaphore operations, please consult the IDT7006 datasheet.

PACKAGE DIMENSIONS — PLEASE CONSULT FACTORY

7-11-9