



# M27218 Octal Backplane Transceiver Data Sheet

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# 1 Introduction to the M27218 Transceiver

The M27218 transceiver is a high speed back plane interconnection device for large capacity switches/routers. The M27218 contains a Parallel LVDS (PLVDS) interface and a high-speed Serial LVDS (SLVDS) interface. The SLVDS interface is CML and can interface with LVDS if the link is AC-coupled running at less than 2 Gbps.

On the SLVDS high speed serial side, the M27218 contains eight dedicated SLVDS differential inputs, and eight dedicated SLVDS differential outputs, with each capable of running at data rates from 622 Mbps to 2.488 Gbps, with the transceiver's performance optimized for 2.488 Gbps. The SLVDS interface operates like CML at 2.488 Gbps, and like LVDS at 622 Mbps.

On the parallel side, there are a total of thirty two dedicated PLVDS inputs and 32 dedicated PLVDS outputs, with each section of four PLVDS I/O corresponding to one high speed SLVDS I/O, hence each of the PLVDS I/O runs at 622 Mbps in a typical case. Forwarded clocks to the receive side of PLVDS I/O can be provided together with the incoming data but are not required.

The M27218 uses a 0.18 micron CMOS process and the core voltage supply is 1.8V, with the voltage supply for the control I/O being 3.3V and PLVDS and SLVDS I/O being 1.8 V/1.5 V.

A manual channel alignment function for the sections of four PLVDS I/O is implemented to realign the four PLVDS received data in one section which may have up to 7 bits of skew. A word alignment function for each Serial LVDS receive channel is implemented to find the correct 4-bit boundary. The control of these functions is done internally and the adjustment decision is made by external software based on monitored results from the M27218.

Built-In-Self-Test (BIST) functions are implemented in the M27218 to facilitate the testing of the device. The BIST logic generates and checks the PRBS patterns going through the SLVDS and PLVDS I/O. In order for the BIST checking logic to compare the received data with the right word boundaries, a special word alignment pattern is generated on the pattern generation side and is used to perform word alignment on the receiver side. In addition to the BIST functions, two loopback modes are implemented in the M27218 to separately test the PLVDS I/O portion (Parallel Loopback) and the SLVDS I/O portion (Reverse Loopback) from outside the device with the help of test equipment.

RoHS compliant versions of the M27218 device are available. The RoHS 2.5 Gbps transceiver part number is M27218G-22. These devices share the same features, specifications, and pinouts as the non-RoHS standard devices.

## 2 Features

- Eight channel SerDes with high speed Serial LVDS I/O capable of bit rates equal to 2.488 Gbps.
- Built-in CDR for PLVDS receiver which makes the forwarded clock for PLVDS I/O and the alignment among the incoming PLVDS data not necessary.
- Amplif-Eye3™ signal conditioning circuitry -- pre-emphasis and receive equalization -- enhances the signal integrity over FR-4 material.
- Flexible clocking modes on PLVDS I/O interfaces allows one or more clocks to represent the PLVDS channels.
- SPI (Serial Peripheral Interface) for all the monitoring and control functions of the device.
- Built-in 50 Ohm termination resistors on the SLVDS/CML and PLVDS interfaces.
- Unique multi-tap FIR filter type of pre-emphasis control with multi-levels of strength for SLVDS I/O.
- Programmable equalization on the SLVDS receiver side.
- Low power consumption with an estimated power consumption of 3.3W or less.
- BIST (Built In Self Test) modes with PRBS pattern for self testing the PLVDS and SLVDS I/O.
- Multiple loop back modes (parallel loop back, reversed loop back) for the independent testing of PLVDS I/O, SLVDS I/O and internal logic.
- On chip transmit and receive FIFO's for transmit and receive clock de-skew.
- 0.18 micron CMOS process.
- 324 BGA package with 23x23 mm body size and 1mm ball pitch.
- 1.8V core voltage supply, 1.8V PLVDS and SLVDS I/O voltage supply and 3.3V control I/O voltage supply.
- Available in RoHS compliant packages.

## 3 System Backplane Applications

Figure 1 shows the M27218 in a typical backplane application with interface to a switch fabric card. The M27218 provides the high-speed serial interconnect between the line card and the switch card or other application.

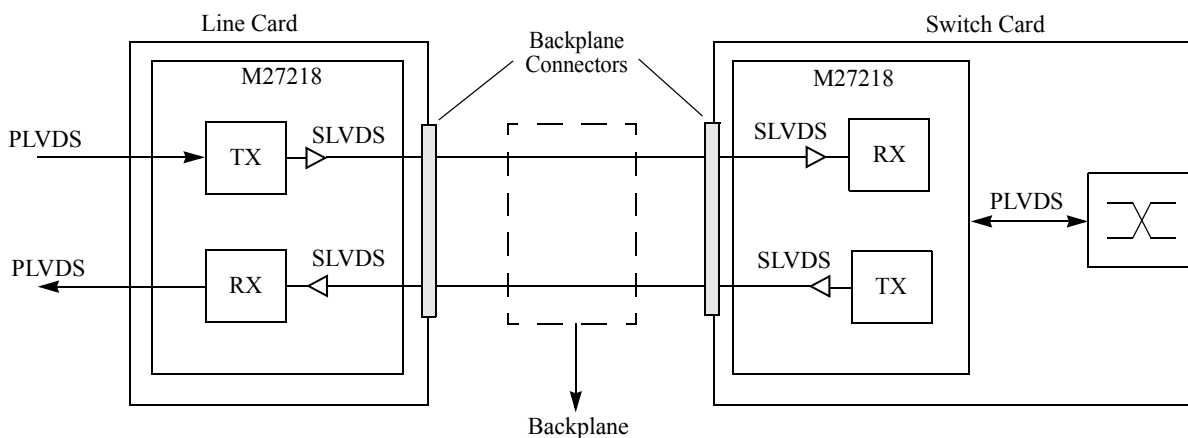


Figure 1 M27218 in a Non-Redundant Backplane Application

### 4 Ordering Information

Part Number	Serial Data Rate	Package	Operating Temperature
M27218-22	2.5 Gbps	324-ball HSBGA 23 mm x 23 mm	-40°C to +85°C
M27218G-22 *	2.5 Gbps	324-ball HSBGA 23 mm x 23 mm, Green	-40°C to +85°C

\* The letter "G" designator after the part number indicates that the device is RoHS-compliant. Refer to [www.mindspeed.com](http://www.mindspeed.com) for additional information.

## 5 Block Diagram

The M27218 contains 32 dedicated PLVDS receive inputs and 32 dedicated PLVDS transmit outputs, referred to as ‘PLVDS channels’. In addition, the device contains 8 SLVDS receive inputs and 8 SLVDS transmit outputs, referred to as ‘SLVDS channels’. [Figure 2](#) shows a device block diagram for the M27218.

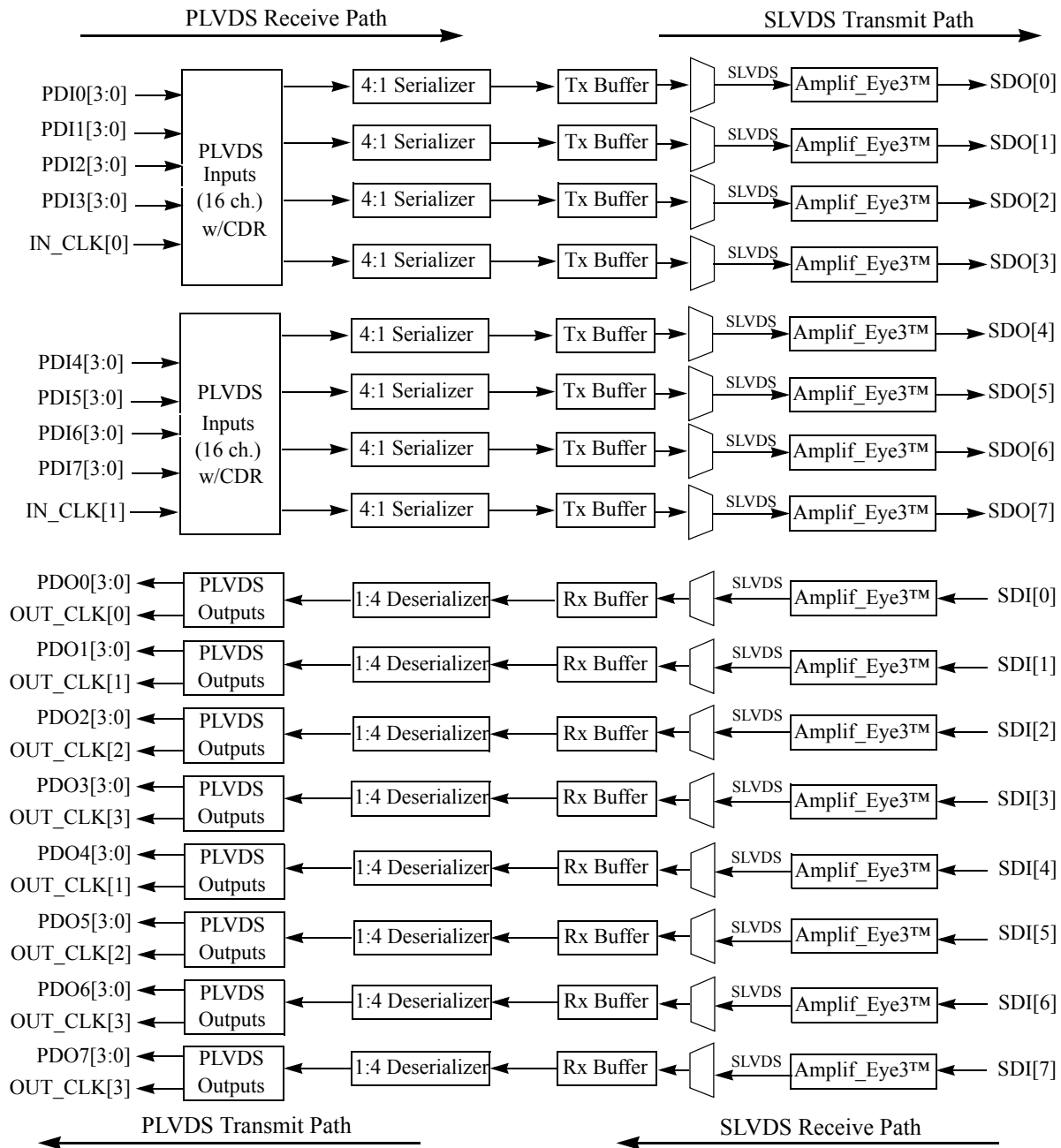


Figure 2 M27218 Device Block Diagram

## 6 Modes of Operation

The M27218 provides two basic modes of operation:

- 2.488 Gbps 4:1 mode
- 622 Mbps 1:1 mode

Throughout this section and the remainder of this document, an ‘LVDS channel’ (either PLVDS or SLVDS) is defined as one LVDS transmit output or receive input. Each ‘channel’ consists of a 2-wire differential pair. For example, in 4:1 mode, there are 4 PLVDS channels per 1 SLVDS channel. This equates to 4 PLVDS inputs (4 differential P/N pairs, or 8 physical pins).

Table 1 shows the relationships between the operating modes listed above.

**Table 1 M27218 Operating Mode Comparison**

SLVDS Receive Bit Rate	PLVDS:SLVDS Channel Ratio	PLVDS Tx/Rx Clock Frequency	PLVDS Data Rate	Bits 5:4 of SLVDS CDR Control Register
2.488 Gbps	4:1	622 MHz	622 Mbps	10
622 Mbps	1:1	622 MHz	622 Mbps	00

In the table above, the SLVDS receive bit rate refers to the SLVDS receive interface (SDI[x]). The bit rate is selected by programming bits 5:4 of the *Serial LVDS CDR Control* register. There is one register for each of the eight SDI[x] channels.

In 4:1 mode, four 622 MHz PLVDS channels (referred to as a ‘section’ throughout this document) are multiplexed onto a single 2.488 Gbps SLVDS channel.

In 1:1 mode, one 622 MHz PLVDS channel is multiplexed onto a single 622 Mbps SLVDS channel.

In all the modes above, the local reference clock is 622 MHz.

Throughout the following subsection, the nomenclature PDIx[x] and PDOx[x] are used to refer to the input and output channels of the PLVDS interface. As stated above, each PLVDS interface (receive and transmit) contains 32 channels divided into eight sections of four channels each. The first number identifies one of 8 sections. The second number refers to the actual PLVDS channel (0 through 3) for that section. For example, PDI3[2] would indicate PLVDS receive section 3, channel 2, PDO6[3] would indicate PLVDS transmit section 6, channel 3, and so on. The following figures show the groupings for each PLVDS interface.

6.1 2.488 Gbps, 4:1 Mode

In this mode the SLVDS channels operate at 2.488 Gbps. The 32 PLVDS channels are divided into eight sections of four channels each. Each LVDS channel operates at 622 Mbps. Each section of 4 channels is processed and driven onto one SLVDS channel. This concept is shown in Figure 3. For more information see “Selecting the PLVDS Input/SLVDS Output Sequence” on page 10 and “Selecting the SLVDS Input/PLVDS Output Sequence” on page 16.

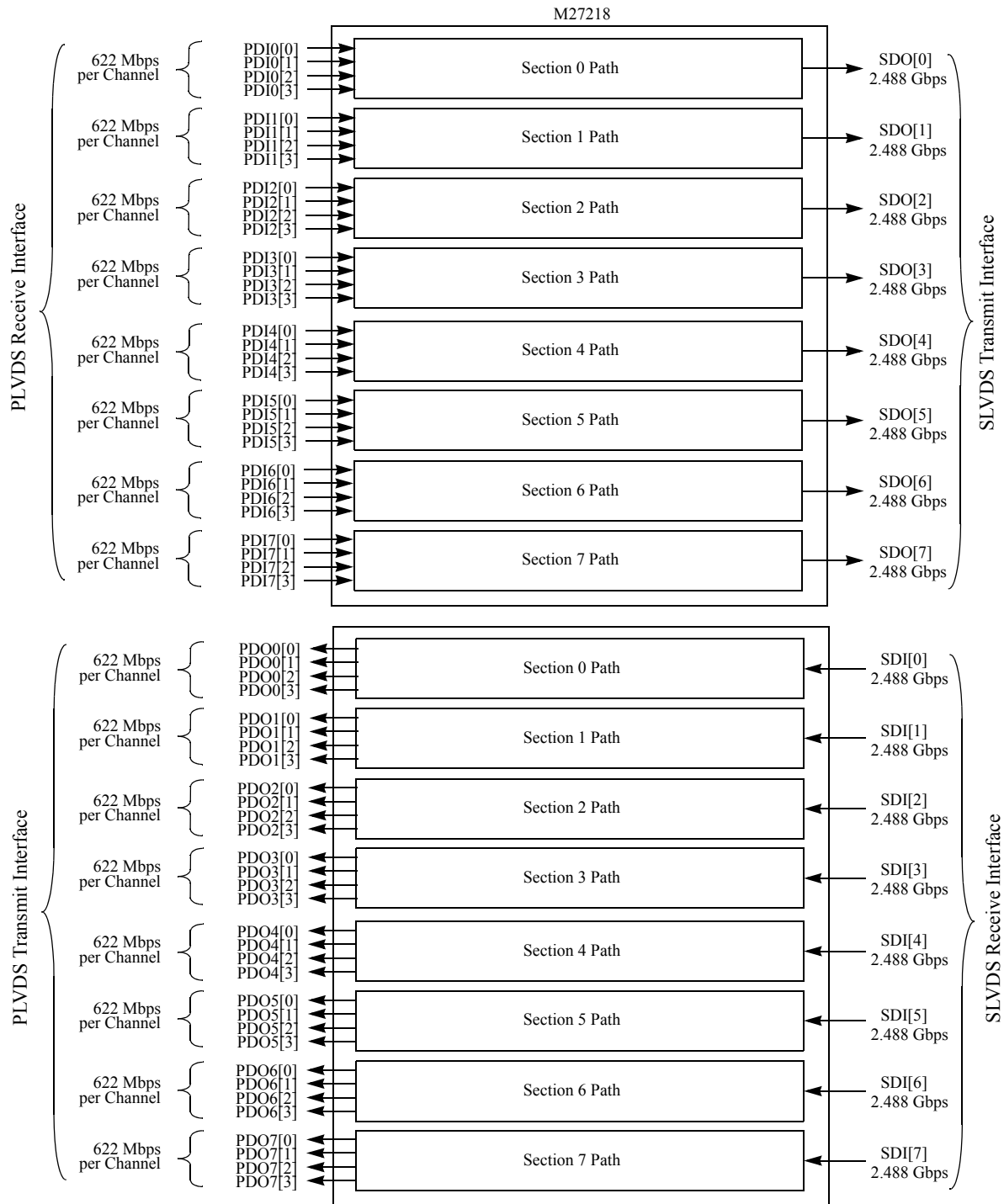


Figure 3 2.488 Gbps 4:1 Mode

6.2 622 Mbps, 1:1 Mode

In this mode the SLVDS channels operate at 622 Mbps. The 32 PLVDS channels are divided into eight sections of four channels each. However, in this mode, within each section of four PLVDS channels, only of the channels is selected, while the other three channels are disabled. For more information see “Selecting the PLVDS Input/SLVDS Output Sequence” on page 10 and “Selecting the SLVDS Input/PLVDS Output Sequence” on page 16. For example, the PDI0[0] can be selected, while PDI0[1], PDI0[2], PDI0[3] are disabled, etc. This mode is also known as “pass-through” mode since there is no muxing or demuxing. This concept is shown in Figure 4.

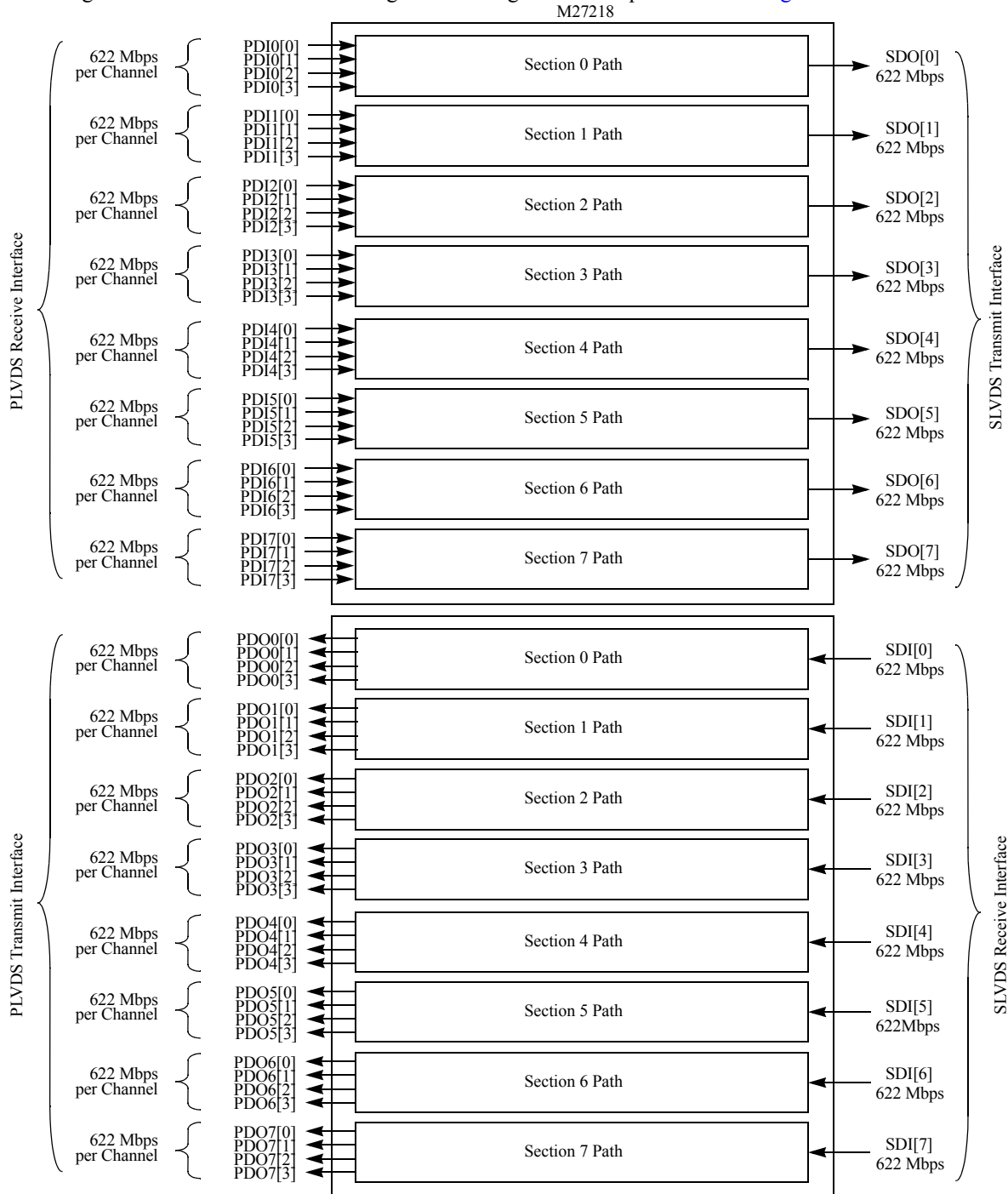


Figure 4 622 Mbps 1:1 Mode

## 7 Clocking Modes

The M27218 uses registers to control the clock characteristics for the PLVDS and SLVDS interfaces as explained in the following subsections.

### 7.1 PLVDS Input Clocking

The *Misc Control* register located at offset address 0x0002 is used to control PLVDS input clocking. The PLVDS receive interface can be clocked using either the IN\_CLK[1:0] pins, or REFCLK. If bit 2 of this register is cleared, IN\_CLK[0] is used to clock PLVDS receive channels 0 through 15. This equates to PDI0[3:0], PDI1[3:0], PDI2[3:0], and PDI3[3:0]. In addition, IN\_CLK[1] is used to clock PLVDS receive channels 16 through 31. This equates to PDI4[3:0], PDI5[3:0], PDI6[3:0], and PDI7[3:0]. No phase relationship is required between the input clock(s) and data since the PLVDS receive channels have CDR. The maximum skew between the PLVDS inputs is 7 bits.

If bit 2 of this register is set, REFCLK is used to clock all 32 PLVDS receive channels. This is shown in [Table 2](#).

**Table 2 PLVDS Receive Interface Clocking**

Bit 2	Input Clock	Channels
0	IN_CLK[0]	PDI0[3:0], PDI1[3:0], PDI2[3:0], PDI3[3:0]
	IN_CLK[1]	PDI4[3:0], PDI5[3:0], PDI6[3:0], PDI7[3:0]
1	REFCLK	PDI0[3:0], PDI1[3:0], PDI2[3:0], PDI3[3:0] PDI4[3:0], PDI5[3:0], PDI6[3:0], PDI7[3:0]

### 7.2 PLVDS Output Clocking

The source for the OUT\_CLK[7:0] signals on the PLVDS transmit interface are selected using bits 1 and 0 of the *Misc Control* register located at offset address 0x0002. Bit 1 is used to enable and disable the output clocks. If this bit is set, output clocking on the PLVDS transmit interface is enabled. If the bit is cleared, output clocking is disabled.

The PLVDS transmit interface has one output clock for each section of four PLVDS channels. The clock pins map to the PLVDS channels as shown in [Table 3](#).

**Table 3 PLVDS Transmit Interface Channels to OUT\_CLK Mapping**

OUT_CLK_x	PLVDS Transmit Channels
0	PDO0[3:0]
1	PDO1[3:0]
2	PDO2[3:0]
3	PDO3[3:0]
4	PDO4[3:0]
5	PDO5[3:0]
6	PDO6[3:0]
7	PDO7[3:0]

If bit 1 of this register is set, the individual serial LVDS recovered clock is used as the PLVDS transmit interface output clock. If this bit is cleared, REFCLK is used. The output clock (OUT\_CLK\_x) is centered with respect to the PLVDS transmit data (PDOx[3:0]).

### 7.3 SLVDS Data Rate

The M27218 transceiver supports data rates of 622 Mbps and 2.488 Gbps on the SLVDS receive interface.

Bits 5:4 in each of the eight *Serial LVDS CDR Control* registers are used to select the SLVDS input data rate. There is one register for each SLVDS channel. These registers are located at the following addresses.

**Table 4 Serial LVDS CDR Control Registers Address Map**

Serial LVDS CDR Control Register	Offset Address
0	0x0103
1	0x0143
2	0x0183
3	0x01B3
4	0x0203
5	0x0243
6	0x0283
7	0x02B3

For any of the above offset addresses, bits 5:4 are encoded as follows to select the SLVDS input data rate.

**Table 5 Encoding Bits 5:4 of the Serial LVDS CDR Control Register**

Bits 5:4	SLVDS Data Rate
00	622 Mbps
01	Reserved
10	2.488 Gbps
11	Reserved

## 8 Selecting the PLVDS Input/SLVDS Output Sequence

The M27218 supports 4:1 and 1:1 PLVDS input channel to SLVDS output channel ratios. The modes are selected using the eight *Parallel to Serial Control* registers. These registers, described in [Section 16.26](#) and [Section 16.27](#), control the wide variety of combinations that can be driven onto the SLVDS channels.

There are two dedicated registers for each 4-channel LVDS section. [Table 6](#) shows the mapping of these registers and corresponding channel sections affected.

**Table 6 Mapping Register Addresses to PLVDS Input Sections/SLVDS Output Channels**

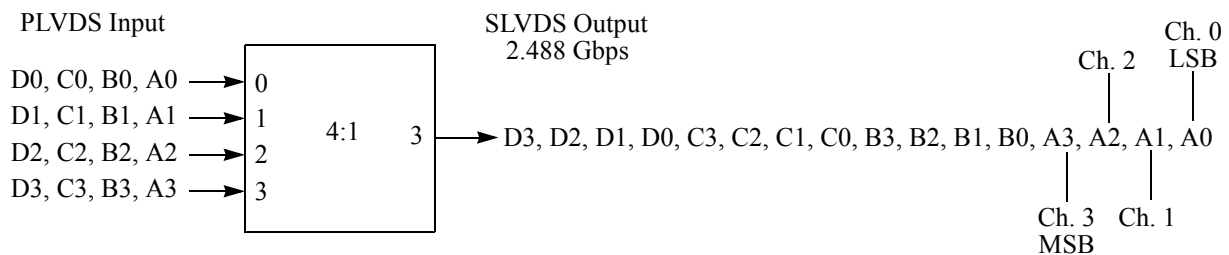
Register Address	Register Bits	PLVDS Section (PDIx)	PLVDS Channel	SLVDS Channel
0x0116	8:5	0	3	0
	3:0	0	2	0
0x0117	8:5	0	1	0
	3:0	0	0	0
0x0156	8:5	1	3	1
	3:0	1	2	1
0x0157	8:5	1	1	1
	3:0	1	0	1
0x0196	8:5	2	3	2
	3:0	2	2	2
0x0197	8:5	2	1	2
	3:0	2	0	2
0x01D6	8:5	3	3	3
	3:0	3	2	3
0x01D7	8:5	3	1	3
	3:0	3	0	3
0x0216	8:5	4	3	4
	3:0	4	2	4
0x0217	8:5	4	1	4
	3:0	4	0	4
0x0256	8:5	5	3	5
	3:0	5	2	5
0x0257	8:5	5	1	5
	3:0	5	0	5
0x0296	8:5	6	3	6
	3:0	6	2	6
0x0297	8:5	6	1	6
	3:0	6	0	6
0x02D6	8:5	7	3	7
	3:0	7	2	7
0x02D7	8:5	7	1	7
	3:0	7	0	7

### 8.1 Selecting the 4:1 PLVDS Input/SLVDS Output Ratio

In the 4:1 mode, the M27218 takes each of the four channels in a section and multiplexes them onto the corresponding SLVDS channel in a sequence determined by programming the appropriate registers. In 4:1 mode each PLVDS channel contains valid data.

#### 8.1.1 Example 1 - 4:1 Mode

The M27218 allows the 4 PLVDS channels in a section to be multiplexed onto the corresponding SLVDS channel in any combination. In [Figure 5](#), the PLVDS interface is programmed to accept channels 0, 1, 2, and 3, serialize them, and drive them onto SLVDS channel 3.



**Figure 5 SLVDS Serial Output Bit Stream Sequence in 4:1 Mode - Example 1**

The SLVDS serial output bit sequence in [Figure 5](#) is accomplished using the Parallel to Serial Control registers described in [Section 16.26](#) and [Section 16.27](#). For example, assume that PLVDS section 3 is to be programmed with the bit stream sequence shown in [Figure 5](#). In this case, the registers would be programmed as shown below:

**Table 7 Programming the PLVDS Section 3 Input Channel Sequence in 4:1 Mode - Example 1**

Register Address	PLVDS Section (PDIx)	PLVDS Channel	Register Bits	Binary Value
0x01D6	3	3	8:5	0011
	3	2	3:0	0010
0x01D7	3	1	8:5	0001
	3	0	3:0	0000

In [Table 7](#), the register field that controls section 3, channel 0 is programmed with a binary value of 0000. As shown in [Section 16.27](#), bits 3:0, this causes the data on PLVDS input channel 0 to be multiplexed onto SLVDS output channel 3 as the first bit in the sequence.

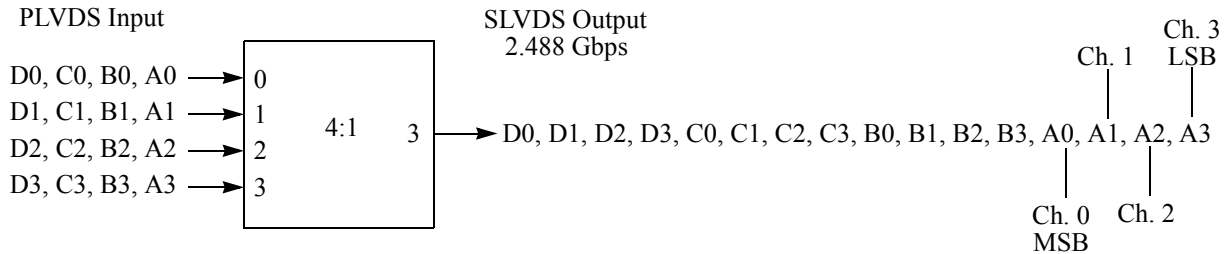
The register field that controls section 3, channel 1 is programmed with a binary value of 0001. As shown in [Section 16.27](#), bits 8:5, this causes the data on PLVDS input channel 1 to be multiplexed onto SLVDS output channel 3 as the second bit in the sequence.

The register field that controls section 3, channel 2 is programmed with a binary value of 0010. As shown in [Section 16.26](#), bits 3:0, this causes the data on PLVDS input channel 2 to be multiplexed onto SLVDS channel 3 as the third bit in the sequence.

The register field that controls section 3, channel 3 is programmed with a binary value of 0011. As shown in [Section 16.26](#), bits 8:5, this causes the data on PLVDS input channel 3 to be multiplexed onto SLVDS channel 3 as the fourth bit in the sequence.

### 8.1.2 Example 2 - 4:1 Mode

In [Figure 6](#), the PLVDS receive interface is programmed to accept channels 3, 2, 1, and 0, serialize them, and drives them onto SLVDS channel 3.



**Figure 6 SLVDS Serial Output Bit Stream Sequence in 4:1 Mode - Example 2**

The SLVDS serial output bit sequence in [Figure 6](#) is accomplished using the Parallel to Serial Control registers described in [Section 16.26](#) and [Section 16.27](#). For example, assume that PLVDS section 3 is to be programmed with the bit stream sequence shown in [Figure 6](#). In this case, the following registers would be programmed as shown below.

**Table 8 Programming the PLVDS Section 3 Input Channel Sequence in 4:1 Mode - Example 2**

Register Address	PLVDS Section (PDIx)	PLVDS Channel	Register Bits	Binary Value
0x01D6	3	3	8:5	0000
	3	2	3:0	0001
0x01D7	3	1	8:5	0010
	3	0	3:0	0011

In [Table 8](#), the register field that controls section 3, channel 0 is programmed with a binary value of 0011. As shown in [Section 16.27](#), bits 3:0, this causes the data on PLVDS input channel 3 to be multiplexed onto SLVDS output channel 3 as the first bit in the sequence.

The register field that controls section 3, channel 1 is programmed with a binary value of 0010. As shown in [Section 16.27](#), bits 8:5, this causes the data on PLVDS input channel 2 to be multiplexed onto SLVDS output channel 3 as the second bit in the sequence.

The register field that controls section 3, channel 2 is programmed with a binary value of 0001. As shown in [Section 16.26](#), bits 3:0, this causes the data on PLVDS input channel 1 to be multiplexed onto SLVDS output channel 3 as the third bit in the sequence.

The register field that controls section 3, channel 3 is programmed with a binary value of 0000. As shown in [Section 16.26](#), bits 8:5, this causes the data on PLVDS input channel 0 to be multiplexed onto SLVDS output channel 3 as the fourth bit in the sequence.

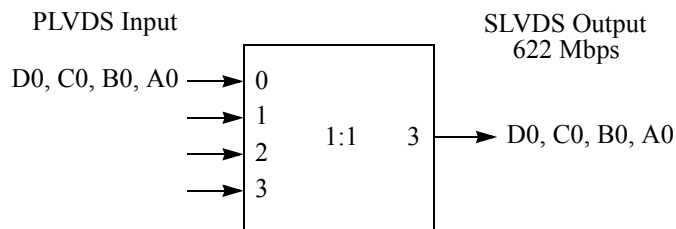
### 8.2 Selecting the 1:1 PLVDS Input/SLVDS Output Ratio

In 1:1 mode, the M27218 allows any PVLDS channels in a section to be multiplexed onto the corresponding SLVDS channel in any combination.

#### 8.2.1 Example 1 - 1:1 Mode

In 1:1 mode, the M27218 allows any PVLDS channels in a section to be multiplexed onto the corresponding SLVDS channel in any combination.

Assume PLVDS channel 0 is contains valid data. The data is then driven onto SLVDS output channel 3. This concept is shown in [Figure 7](#). In this case PLVDS input channels 1, 2, and 3 would be placed in the power-down state by programming the *Power Down* register. Refer to Section 16.4 for more information.



**Figure 7 SLVDS Serial Output Bit Stream Sequence in 1:1 Mode - Example 1**

The SLVDS serial output bit sequence in [Figure 7](#) is accomplished using the Parallel to Serial Control registers described in [Section 16.26](#) and [Section 16.27](#). For example, assume that PLVDS section 3 is to be programmed with the bit stream sequence shown in [Figure 7](#). In this case, the following registers would be programmed as shown below.

**Table 9 Programming the PLVDS Section 3 Input Channel Sequence in 1:1 Mode - Example 1**

Register Address	PLVDS Section (PDIx)	PLVDS Channel	Register Bits	Binary Value
0x01D6	3	3	8:5	0000
	3	2	3:0	0000
0x01D7	3	1	8:5	0000
	3	0	3:0	0000

In [Table 9](#), the register field that controls section 3, channel 0 is programmed with a binary value of 0000. As shown in [Section 16.27](#), bits 3:0, this causes the data on PLVDS input channel 0 to be multiplexed onto SLVDS output channel 3 as the first bit in the sequence.

The register field that controls section 3, channel 1 is programmed with a binary value of 0000. As shown in [Section 16.27](#), bits 8:5, this causes the data on PLVDS input channel 0 to be multiplexed onto SLVDS output channel 3 as the second bit in the sequence. Even though this might appear to be redundant, it is required.

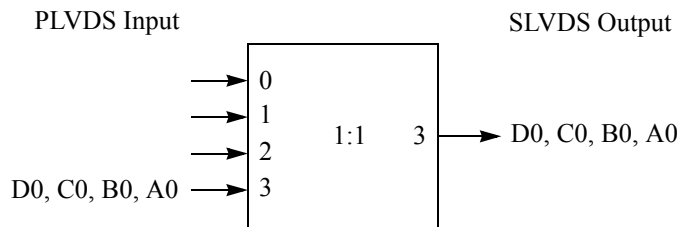
The register field that controls section 3, channel 2 is programmed with a binary value of 0000. As shown in [Section 16.26](#), bits 3:0, this causes the data on PLVDS input channel 0 to be multiplexed onto SLVDS output channel 3 as the third bit in the sequence. Even though this might appear to be redundant, it is required.

The register field that controls section 3, channel 3 is programmed with a binary value of 0000. As shown in [Section 16.26](#), bits 8:5, this causes the data on PLVDS input channel 0 to be multiplexed onto SLVDS output channel 3 as the fourth bit in the sequence. Even though this might appear to be redundant, it is required.

### 8.2.2 Example 2 - 1:1 Mode

As explained in the previous section, when operating on 1:1 mode, the M27218 multiplexes valid data from one PLVDS input channel onto the corresponding SLVDS transmit channel. Any one of the four channels in a given section can be selected as the valid channel.

Assume that PLVDS channel 3 contains valid data. The data is then driven onto SLVDS output channel 3. This concept is shown in [Figure 8](#). In this case PLVDS input channels 0, 1, and 2 would be placed in the power-down state by programming the *Power Down* register. Refer to [Section 16.4](#) for more information.



**Figure 8 SLVDS Serial Output Bit Stream Sequence in 1:1 Mode - Example 2**

The SLVDS serial output bit sequence in [Figure 8](#) is accomplished using the *Parallel to Serial Control* registers described in [Section 16.26](#) and [Section 16.27](#). For example, assume that PLVDS section 3 is to be programmed with the bit stream sequence shown in [Figure 8](#). In this case, the following registers would be programmed as shown below.

**Table 10 Programming the PLVDS Section 3 Input Channel Sequence in 1:1 Mode - Example 2**

Register Address	PLVDS Section (PDIx)	PLVDS Channel	Register Bits	Binary Value
0x01D6	3	3	8:5	0011
	3	2	3:0	0011
0x01D7	3	1	8:5	0011
	3	0	3:0	0011

As shown in [Table 10](#), the register field that controls section 3, channel 0 is programmed with a binary value of 0011. As shown in [Section 16.27](#), bits 3:0, this causes the data on PLVDS input channel 3 to be multiplexed onto SLVDS channel 3 as the first bit in the sequence.

The register field that controls section 3, channel 1 is programmed with a binary value of 0011. As shown in [Section 16.27](#), bits 8:5, this causes the data on PLVDS input channel 3 to be multiplexed onto SLVDS channel 3 as the second bit in the sequence. Even though this might appear to be redundant, it is required.

The register field that controls section 3, channel 2 is programmed with a binary value of 0011. As shown in [Section 16.26](#), bits 3:0, this causes the data on PLVDS input channel 3 to be multiplexed onto SLVDS channel 3 as the third bit in the sequence. Even though this might appear to be redundant, it is required.

## 8 Selecting the PLVDS Input/SLVDS Output Sequence

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The register field that controls section 3, channel 3 is programmed with a binary value of 0011. As shown in [Section 16.26](#), bits 8:5, this causes the data on PLVDS input channel 3 to be multiplexed onto SLVDS channel 3 as the fourth bit in the sequence. Even though this might appear to be redundant, it is required.

## 9 Selecting the SLVDS Input/PLVDS Output Sequence

The M27218 supports 1:4 and 1:1 SLVDS input channel to PLVDS output channel ratios. The modes are selected using the eight *Serial to Parallel Control* registers. These registers control the wide variety of combinations that can be driven onto each 4-channel section of the PLVDS output interface.

The SLVDS input mode is selected using the *Serial to Parallel Control* registers described in [Section 16.28](#) and [Section 16.29](#). There are two dedicated registers for each SLVDS input channel/PLVDS output section. [Table 11](#) shows the mapping of these registers and the corresponding channel sections affected.

**Table 11 Mapping Register Addresses to PLVDS Output Sections/SLVDS Input Channels**

Register Address	Register Bits	PLVDS Section (PDOx)	PLVDS Channel	SLVDS Channel
0x0118	8:5	0	3	0
	3:0	0	2	0
0x0119	8:5	0	1	0
	3:0	0	0	0
0x0158	8:5	1	3	1
	3:0	1	2	1
0x0159	8:5	1	1	1
	3:0	1	0	1
0x0198	8:5	2	3	2
	3:0	2	2	2
0x0199	8:5	2	1	2
	3:0	2	0	2
0x01D8	8:5	3	3	3
	3:0	3	2	3
0x01D9	8:5	3	1	3
	3:0	3	0	3
0x0218	8:5	4	3	4
	3:0	4	2	4
0x0219	8:5	4	1	4
	3:0	4	0	4
0x0258	8:5	5	3	5
	3:0	5	2	5
0x0259	8:5	5	1	5
	3:0	5	0	5
0x0298	8:5	6	3	6
	3:0	6	2	6
0x0299	8:5	6	1	6
	3:0	6	0	6
0x02D8	8:5	7	3	7
	3:0	7	2	7
0x02D9	8:5	7	1	7
	3:0	7	0	7

## 9 Selecting the SLVDS Input/PLVDS Output Sequence

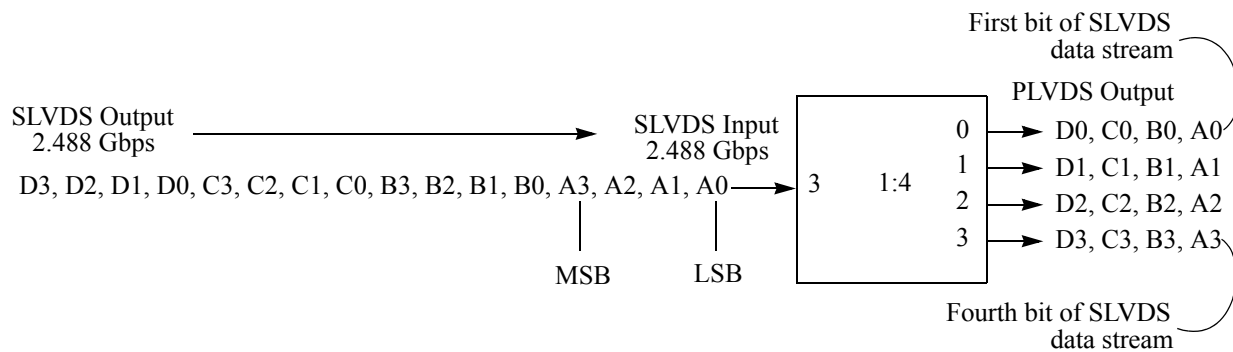
The SLVDS serial input bit stream can be selected at 2.488 Gbps or 622 Mbps depending on the programming of bits 5:4 of the *Serial LVDS CDR Control* register. Refer to [Table 5](#) for more information.

### 9.1 Selecting the 1:4 SLVDS Input/PLVDS Output Ratio

In the 1:4 mode, the M27218 takes the incoming data stream on the incoming SLVDS channel, deserializes it, and drives it onto the corresponding 4-channel PLVDS outputs in a manner determined by programming the appropriate registers. In 1:4 mode each PLVDS output channel contains valid data.

#### 9.1.1 Example 1 - 1:4 Mode

In this example, the M27218 accepts data on SLVDS channel 3. The data stream is demultiplexed onto the 4 PLVDS output channels of section 3 in any combination. This is shown in [Figure 9](#). In this example bits 5:4 of the *Serial LVDS Control* register corresponding to SLVDS channel 3 would be programmed with a value of 0b10, indicating an SLVDS input data rate of 2.488 Gbps.



**Figure 9 PLVDS Output Bit Sequence in 1:4 Mode - Example 1**

The PLVDS parallel output bit sequence in [Figure 9](#) is accomplished using the *Serial to Parallel Control* registers described in [Section 16.28](#) and [Section 16.29](#). For example, assume that PLVDS output section 3 is programmed with the bit stream sequence shown in [Figure 9](#). In this case, the following registers would be programmed as follows:

**Table 12 Programming the PLVDS Section 3 Output Channel Sequence in 1:4 Mode - Example 1**

Register Address	PLVDS Output Section (PDOx)	PLVDS Output Channel	Register Bits	Binary Value
0x01D8	3	3	8:5	0011
	3	2	3:0	0010
0x01D9	3	1	8:5	0001
	3	0	3:0	0000

As shown in [Table 12](#), the register field that controls section 3, channel 0 is programmed with a binary value of 0000. As shown in [Section 16.29](#), bits 3:0, this causes the first bit in the incoming SLVDS bit stream (A0) to be driven onto PLVDS output channel 0.

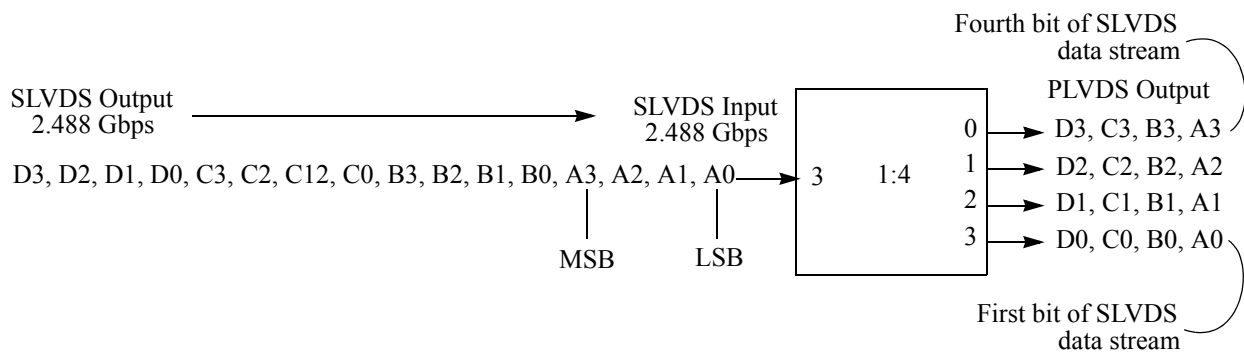
The register field that controls section 3, channel 1 is programmed with a binary value of 0001. As shown in [Section 16.29](#), bits 8:5, this causes the second bit in the incoming SLVDS bit stream (A1) to be driven onto PLVDS output channel 1.

The register field that controls section 3, channel 2 is programmed with a binary value of 0010. As shown in Section 16.28, bits 3:0, this causes the third bit in the incoming SLVDS bit stream (A2) to be driven onto PLVDS output channel 2.

The register field that controls section 3, channel 3 is programmed with a binary value of 0011. As shown in Section 16.28, bits 3:0, this causes the fourth bit in the incoming SLVDS bit stream (A3) to be driven onto PLVDS output channel 3.

**9.1.2 Example 2 - 1:4 Mode**

In Figure 10, the M27218 receives data on SLVDS channel 3, deserializes it, and drives it onto channels 3, 2, 1, and 0 of PLVDS output section 3 as shown. In this example bits 5:4 of the *Serial LVDS Control* register corresponding to SLVDS channel 3 would be programmed with a value of 0b10, indicating an SLVDS input data rate of 2.488 Gbps.



**Figure 10 PLVDS Output Bit Sequence in 1:4 Mode - Example 2**

The PLVDS parallel output bit sequence in Figure 10 is accomplished using the *Serial to Parallel Control* registers described in Section 16.28 and Section 16.29. For example, assume that PLVDS output section 3 is programmed with the bit stream sequence shown in Figure 10. In this case, the registers would be programmed as follows:

**Table 13 Programming the PLVDS Section 3 Output Channel Sequence in 1:4 Mode - Example 2**

Register Address	PLVDS Output Section (PDOx)	PLVDS Output Channel	Register Bits	Binary Value
0x01D8	3	3	8:5	0000
	3	2	3:0	0001
0x01D9	3	1	8:5	0010
	3	0	3:0	0011

As shown in Table 13, the register field that controls section 3, channel 0 is programmed with a binary value of 0011. As shown in Section 16.29, bits 3:0, this causes the fourth bit in the incoming SLVDS bit stream (A3) to be output onto PLVDS output channel 3.

The register field that controls section 3, channel 1 is programmed with a binary value of 0010. As shown in Section 16.29, bits 8:5, this causes the third bit in the incoming SLVDS bit stream (A2) to be output onto PLVDS output channel 2.

## 9 Selecting the SLVDS Input/PLVDS Output Sequence

The register field that controls section 3, channel 2 is programmed with a binary value of 0001. As shown in Section 16.28, bits 3:0, this causes the second bit in the incoming SLVDS bit stream (A1) to be output onto PLVDS output channel 1.

The register field that controls section 3, channel 3 is programmed with a binary value of 0000. As shown in Section 16.28, bits 3:0, this causes the first bit in the incoming SLVDS bit stream (A0) to be output onto PLVDS output channel 0.

### 9.2 Selecting the 1:1 SLVDS Input/PLVDS Output Ratio

In 1:1 mode, the M27218 drives the incoming SLVDS data onto the appropriate PLVDS output channel as determined by register programming. In this mode, the user can select which output is valid. The invalid PLVDS output channels are driven with zero.

#### 9.2.1 Example 1 - 1:1 Mode

In Figure 11, data is received on SLVDS channel 3, deserialized, and driven onto output channel 0 of PLVDS section 3 as shown. In this example bits 5:4 of the Serial LVDS Control register corresponding to SLVDS channel 3 would be programmed with a value of 0b00, indicating an SLVDS input data rate of 622 Mbps.

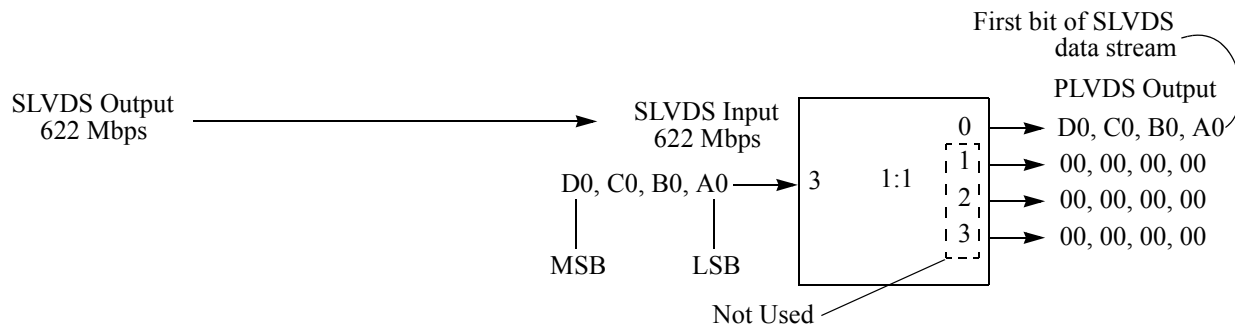


Figure 11 PLVDS Output Bit Sequence in 1:2 Mode - Example 1

The PLVDS parallel output bit sequence in Figure 11 is accomplished using the *Serial to Parallel Control* registers described in Section 16.28 and Section 16.29. For example, assume that PLVDS output section 3 is programmed with the bit stream sequence shown in Figure 11. In this case, the following registers would be programmed as shown below.

Table 14 Programming the PLVDS Section 3 Output Channel Sequence in 1:2 Mode - Example 1

Register Address	PLVDS Output Section (PDOx)	PLVDS Output Channel	Register Bits	Binary Value
0x01D8	3	3	8:5	1000
	3	2	3:0	1000
0x01D9	3	1	8:5	1000
	3	0	3:0	0000

As shown in Table 14, the register field that controls section 3, channel 0 is programmed with a binary value of 0000. As shown in Section 16.29, bits 3:0, this causes the first bit in the incoming SLVDS bit stream (A0) to be output onto PLVDS output channel 0.

The register field that controls section 3, channel 1 is programmed with a binary value of 1000. This causes a value of 00 to be driven onto PLVDS output channel 1.

The register field that controls section 3, channel 2 is programmed with a binary value of 1000. This causes a value of 00 to be driven onto PLVDS output channel 2.

The register field that controls section 3, channel 3 is programmed with a binary value of 1000. This causes a value of 00 to be driven onto PLVDS output channel 3.

### 9.2.2 Example 2 - 1:1 Mode

In Figure 12, data is received on SLVDS channel 3, deserialized, and driven onto output channel 3 of the PLVDS section 3 as shown. In this example bits 5:4 of the Serial LVDS Control register corresponding to SLVDS channel 3 would be programmed with a value of 0b00, indicating an SLVDS input data rate of 622 Mbps.

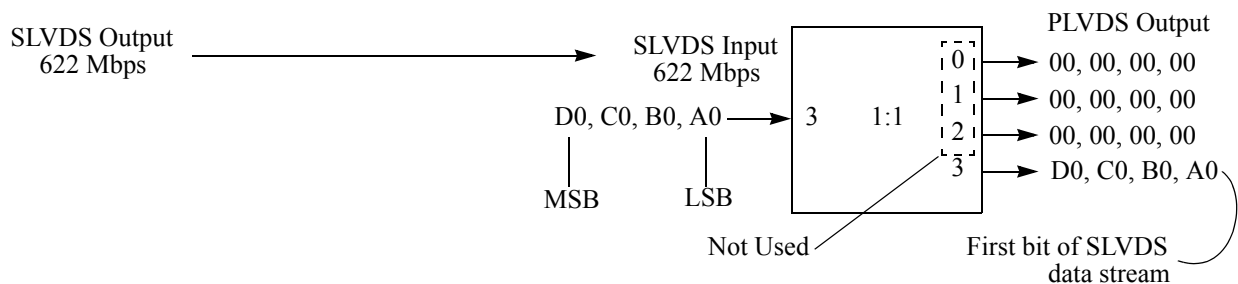


Figure 12 PLVDS Output Bit Sequence in 1:2 Mode - Example 2

The PLVDS parallel output bit sequence in Figure 12 is accomplished using the Serial to Parallel Control registers described in Section 16.28 and Section 16.29. For example, assume that PLVDS output section 3 is programmed with the bit stream sequence shown in Figure 12. In this case, the following registers would be programmed as shown below.

Table 15 Programming the PLVDS Section 3 Output Channel Sequence in 1:2 Mode - Example 2

Register Address	PLVDS Output Section (PDOx)	PLVDS Output Channel	Register Bits	Binary Value
0x01D8	3	3	8:5	0011
	3	2	3:0	1000
0x01D9	3	1	8:5	1000
	3	0	3:0	1000

As shown in Table 15, the register field that controls section 3, channel 0 is programmed with a binary value of 1000. This causes a value of 00 to be driven onto PLVDS output channel 0.

The register field that controls section 3, channel 1 is programmed with a binary value of 1000. This causes a value of 00 to be driven onto PLVDS output channel 1.

## 10 Data Alignment

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The register field that controls section 3, channel 2 is programmed with a binary value of 1000. This causes a value of 00 to be driven onto PLVDS output channel 2.

The register field that controls section 3, channel 3 is programmed with a binary value of 0011. As shown in Section 16.28, bits 3:0, this causes the first bit in the incoming SLVDS bit stream (A0) to be output onto PLVDS output channel 3.

## 10 Data Alignment

Automatic data alignment is a feature not supported by this device. If required, alignment can be achieved by using the manual alignment registers. This requires a software search algorithm to perform frame alignment.

## 11 Power Management

The M27218 contains a flexible power management scheme that allows for the individual power-down of each PLVDS input and output channel on the device. Eight dedicated registers, one per 4-channel PLVDS section (input and output), are used to control the power down function. Table 16 shows the register addresses and the corresponding PLVDS sections and channels.

**Table 16 Power Down Control on the PLVDS Interface**

Register Address	PLVDS Input and Output Section	PLVDS Input Channels	PLVDS Output Channels
0x0100	0	3:0	3:0
0x0140	1	3:0	3:0
0x0180	2	3:0	3:0
0x01B0	3	3:0	3:0
0x0200	4	3:0	3:0
0x0240	5	3:0	3:0
0x0280	6	3:0	3:0
0x21B0	7	3:0	3:0

In addition to the ability to disable each individual PLVDS channel, each register also provides the following capability:

- Reset the entire PLVDS input → SLVDS output logic path by setting one bit.
- Reset the entire SLVDS input → PLVDS output logic path by setting one bit.
- Power down the entire PLVDS input section and corresponding SLVDS output channel by setting one bit.
- Power down the entire PLVDS output section and corresponding SLVDS input channel by setting one bit.

By default, all PLVDS input and output channels are in the power down state at reset. Therefore, software must set the appropriate registers bits to zero to enable them, or write a value of 0x0000 to the register to enable all channels.

For example, assume that software wants to enable PLVDS section 0 as follows:

- enable input channels 0, 1, and 2
- disable input channel 3
- enable output channels 0, 1, and 2

- disable output channel 3

As shown in Section 16.4, "Power Down Control Register" bit 3 controls PLVDS output channel 3, and bit 7 controls PLVDS input channel 3. To disable these two channels and enable all other input and output channels, software would write a value of 0x0088 to this register. This is equivalent to the binary value shown in [Table 17](#).

**Table 17 Placing PLVDS Input Channel 3 and Output Channel 3 in the Power Down State**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
---	---	---	---	R_P2S	R_S2P	P_P2S	P_S2P	I_CH3	I_CH2	I_CH1	I_CH0	O_CH3	O_CH3	O_CH3	O_CH3
0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0

In this example bits 7 and 3 of the register are set, placing input channel 3 and output channel 3 in the power down state.

## 12 Analog Pre-Emphasis and Equalization on the SLVDS Interface

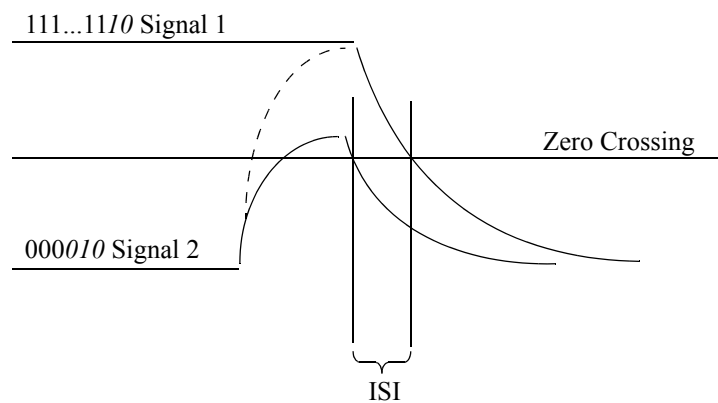
The M27218 provides for analog pre-emphasis on the SLVDS transmit interface, and for equalization on the SLVDS receive interface. These two functions are explained in the following subsections.

If the bit-error rate is not acceptable, it is recommended to use equalization first, and then pre-emphasis.

### 12.1 Definition of Pre-Emphasis

The main factor that limits the maximum length in a transmission line is signal jitter, which is primarily due to inter-symbol interference (ISI). ISI is the net effect of several causes of signal degradation. One cause is the attenuation and the dispersal of frequency components that result from signal propagation down a transmission line. Another cause is the variation of rise and fall times that follow the varying sequences of ones and zeros known as “pattern-dependent skew.”

One way to extend the distance for a given data rate is by reducing the effect of jitter that ISI causes. Pre-emphasis increases the maximum values for data rate and transmission distance. For example, assume a series of ones followed by a series of zeros causes the transmission line voltage at the end of the string of ones to rise to the highest possible level, such as the level of signal 1 in Figure 13 below. A signal at this high level takes the longest time to reach the zero crossing. On the other hand, if the data pattern consists of a string of zeros followed by a one and then a zero, the one-to-zero transition (signal 2 in Figure 13) starts from a voltage much closer to the zero crossing. Therefore, signal 2 takes less time to reach zero crossing. A signal’s propagation delay depends on its preceding bit pattern. This pattern-dependent skew is the ISI.



**Figure 13 Transmission Line Voltages Relative to the Zero Crossing**

Pre-emphasis is necessary only when the data pattern changes and not during the intervals when the signal voltage remain at the same logic level. On the other hand, the need for pre-emphasis is constant for signals with logic-level changes at every bit interval.

### 12.2 Analog Pre-Emphasis on the SLVDS Transmit Interface

Analog emphasis allows hardware to accentuate each initial high-to-low and low-to-high transition on a differential pair. These accentuated voltage swings make it easier for the logic on the receiver to detect high and low transitions on each differential pair. Typically, the longer the length of the differential pairs, the greater the need for analog pre-emphasis.

The analog pre-emphasis function is controlled using bits 4:3 of the *Misc Control* register, and bits 3:0 of the *SLVDS Pre-Emphasis and Equalization Control* register. There is one *SLVDS Pre-Emphasis and Equalization Control* register for each SLVDS output channel.

The 2-bit *Swing* field (bits 4:3) of the *Misc Control* register indicates the overall voltage swing voltage between the SDO[n]P and SDO[n]N wires of the differential pair (where [n] = SLVDS channels 0 through 7). The M27218 supports analog swing voltages of 300, 500, 650, and 800 mV differential peak-to-peak. The 4-bit *Pre-Emph* field (bits 3:0) of the *SLVDS Pre-emphasis and Equalization Control* register allows software to adjust the amount of analog pre-emphasis from weakest (pre-emphasis disabled) to strongest relative to the swing voltage.

Figure 14 shows an oscilloscope waveform with analog pre-emphasis enabled.

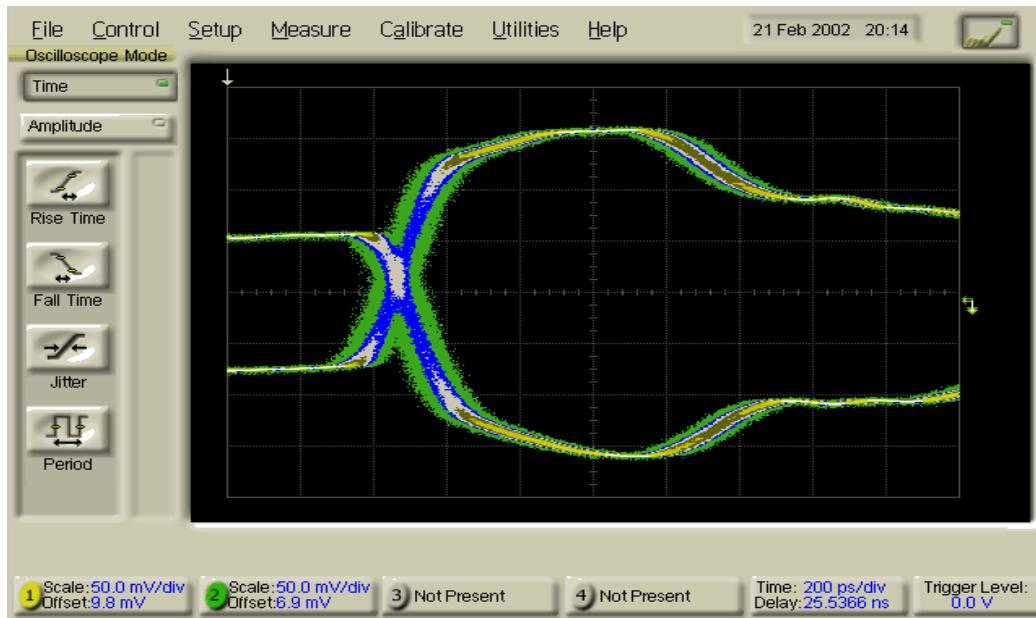


Figure 14 Data Transition on the SLVDS Interface with Analog Emphasis Enabled

Figure 15 shows a typical transition sequence on the SDO[n]P/SDO[n]N differential pair with analog pre-emphasis disabled (Pre\_Emph[3:0] = 0000).

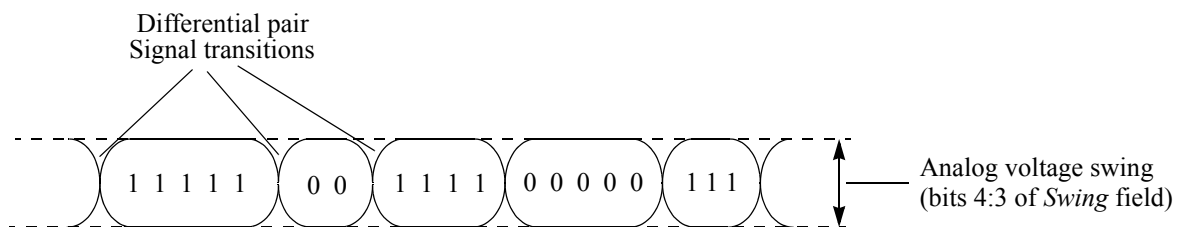
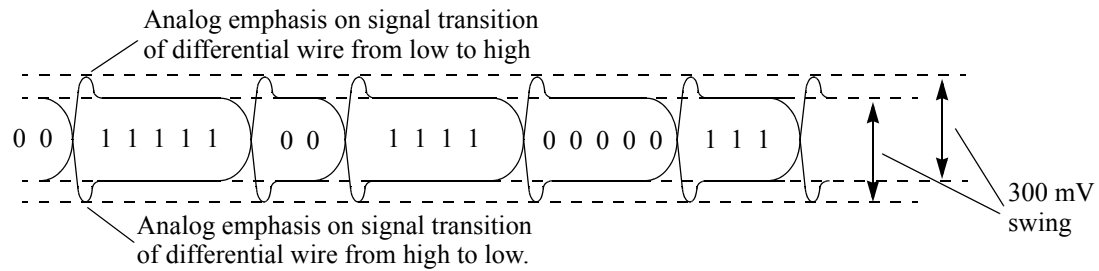


Figure 15 Analog Voltage Swing with Analog Pre-Emphasis Disabled

When analog pre-emphasis is enabled (Pre\_Emph[3:0] is a non-zero value), the value programmed into the 2-bit *Swing* field at reset represents an average swing voltage, rather than an absolute value between two fixed voltage levels when emphasis is disabled (see Figure 15). For example, when a 300 mV average swing is selected by programming the *Swing* field with a value of 00, the resulting waveform is shown in Figure 16.



**Figure 16 Analog Voltage Swing on the SkyRail Interface with Analog Emphasis Enabled**

Each wire of a differential pair transitions from high-to-low or low-to-high each time there is a corresponding data transition from 1 to 0 or 0 to 1. If analog pre-emphasis is enabled, the initial transition is accentuated on both the high and low end to more clearly identify the data transitions. A data transition occurs each time there is a 1 to 0 or 0 to 1 transition as shown in the diagram.

### 12.2.1 Misc Control Register

Bits 4:3 of the *Misc Control* register set the analog swing voltage for the eight SLVDS outputs. The default value is set to 800 mV as shown in [Table 18](#).

**Table 18 Programming the Swing Field of the Misc Control Register**

Register Address	Register Bits	Default	Description	SLVDS Output Channels Affected
0x0002	4:3	0b10	Swing voltage for SDO[x] SLVDS outputs: 00 = 300 mV 01 = 500 mV 10 = 650 mV 11 = 800 mV	0 - 7

### 12.2.2 Pre-Emphasis and Equalization Control Registers

The *Pre-Emphasis and Equalization Control* registers are located at the addresses shown in [Table 19](#).

**Table 19 SLVDS Pre-Emphasis and Equalization Control Registers**

Register Address	SLVDS Output Channel	Register Bits	Description
0x0101	0	5:4	Receive equalization for SLVDS input channel 0.
		3:0	Analog pre-emphasis for SLVDS output channel 0.
0x0141	1	5:4	Receive equalization for SLVDS input channel 1.
		3:0	Analog pre-emphasis for SLVDS output channel 1.
0x0181	2	5:4	Receive equalization for SLVDS input channel 2.
		3:0	Analog pre-emphasis for SLVDS output channel 2.
0x01C1	3	5:4	Receive equalization for SLVDS input channel 3.
		3:0	Analog pre-emphasis for SLVDS output channel 3.

**Table 19 SLVDS Pre-Emphasis and Equalization Control Registers (Continued)**

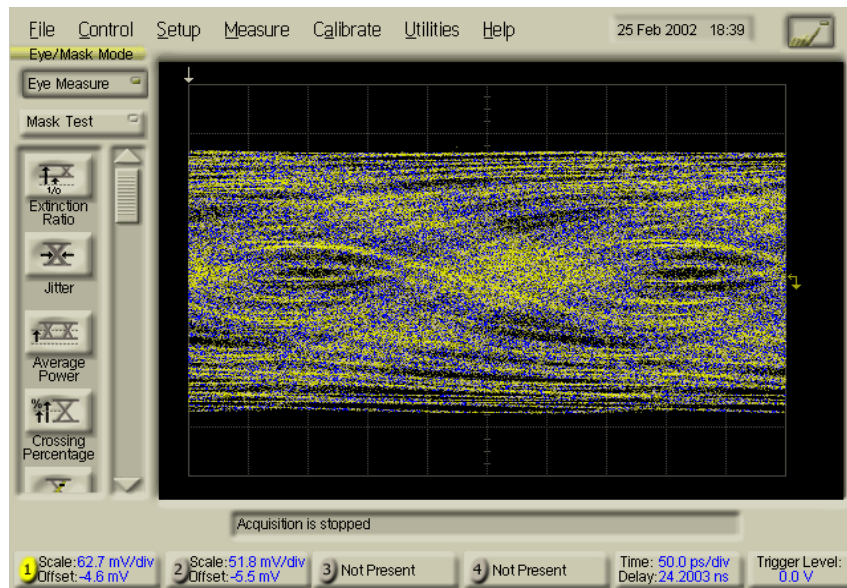
Register Address	SLVDS Output Channel	Register Bits	Description
0x0201	4	5:4	Receive equalization for SLVDS input channel 4.
		3:0	Analog pre-emphasis for SLVDS output channel 4.
0x0241	5	5:4	Receive equalization for SLVDS input channel 5.
		3:0	Analog pre-emphasis for SLVDS output channel 5.
0x0281	6	5:4	Receive equalization for SLVDS input channel 6.
		3:0	Analog pre-emphasis for SLVDS output channel 6.
0x02C1	7	5:4	Receive equalization for SLVDS input channel 7.
		3:0	Analog pre-emphasis for SLVDS output channel 7.

### 12.3 Analog Equalization on the SLVDS Receive Interface

The M27218 provides programmable equalization control for all eight SLVDS receive channels. The receive equalizer compensates each received signal for dielectric and skin losses. In other words, it reduces intersymbol interference (ISI), compensating for frequency-dependent, media induced loss. Moreover, the transmission line can be represented as a low-pass filter, and the receive equalizer amplifies the gain at high-frequencies, compensating for the attenuation.

There are eight registers used to control equalization, one for each SLVDS input as shown in Table 19 above. Bits 5:4 of each register in Table 19 control the level of receive equalization for each SLVDS input channel. A value of 0b00 in this field disables receive equalization, while a value of 11 is the strongest amount of equalization.

Figure 17 shows a data eye of the SLVDS receive interface with equalization disabled.



**Figure 17 SLVDS Input Channel Receive Data with Equalization Disabled**

Figure 18 shows a data eye of the SLVDS receive interface with equalization enabled.

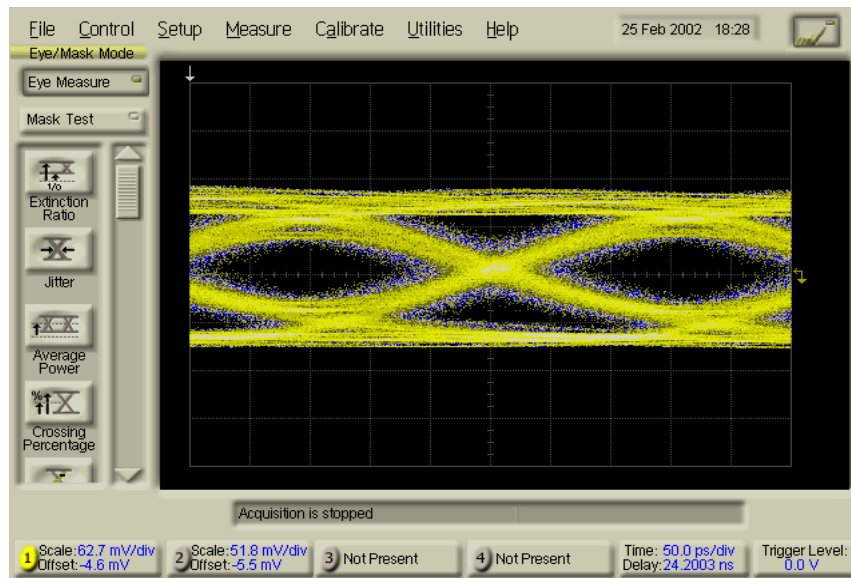


Figure 18 SLVDS Input Channel Receive Data with Equalization Enabled

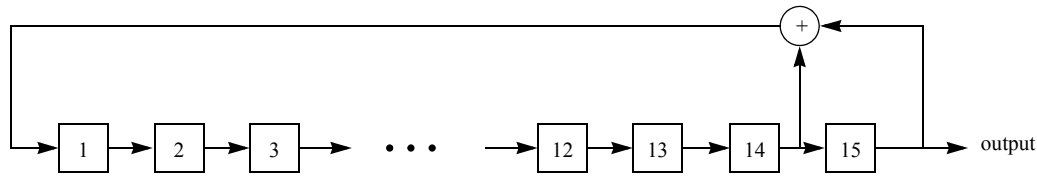
## 13 BIST Modes

The M27218 contains built-in self test (BIST) functions to test the parallel and serial interfaces as well as the related logic without using any external equipment. The BIST logic consists of two major blocks: the BIST pattern generation block and the BIST pattern checking block. The BIST pattern generation and checking are slightly different for Serial LVDS interface and Parallel LVDS interface. The BIST pattern is organized in a proprietary frame structure, which includes a fixed frame header, followed by a sequence of CID (Contiguous Identical Digit, “0” or “1”) with programmable length (in bytes or dual bits) and then followed by a fixed-length PRBS (Pseudo Random Binary Sequence).

The frame header is defined to be 16 “1” followed by 16 “0”. This is a unique 4-byte sequence which is guaranteed not to appear in the CID sequence and PRBS, such that it can be used by the checker to do the frame synchronization before checking for CID and PRBS.

The CID is a sequence of contiguous “1” or “0” defined by the BIST control registers. The length of the CID sequence (in bytes or dual bits) is also defined in those registers.

The PRBS is generated using the following polynomial:  $x^{15} + x^{14} + 1$ . Theoretically this sequence may be generated in a fifteen-stage shift register whose 15<sup>th</sup> and 14<sup>th</sup> stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage. The initial states of the shift registers can be programmed through registers (see BIST PRBS Seed Register 1 and BIST PRBS Seed Register 0) and the default are all 1’s. This concept is shown in [Figure 19](#).



**Figure 19 PRBS Pattern Generation**

The length of the PRBS pattern in each frame is  $2^{15}$  bits and the same frame will be repeated as long as the BIST function is enabled.

On the BIST pattern check side, the checker first looks for the frame header, then checks for the known length of the all “0” or all “1”, 8 bits at a time in the case of serial interface BIST or 2 bits at a time in the case of parallel interface BIST, and then checks for the PRBS pattern (self generated), also 8 bits at a time in the case of serial interface BIST or 2 bits at a time in the case of parallel interface BIST.

## 14 Loop Back Modes

The M27218 provides two loopback modes to facilitate testing of the device using external testing equipment: Parallel Loopback and Reverse Loopback. These two loopback modes can be set independently for each individual section through the control registers for Parallel to Serial Output Bit-Sequence, Serial Input Bit-Sequence to Parallel Outputs and Serial LVDS BIST control registers.

In the Parallel Loopback mode, data received from the Parallel LVDS receivers is sent back to the Parallel LVDS transmitters without going through the SLVDS transmit logic. In this mode, bit 2 of the *Misc Control* register must be set to select REFCLK as the PLVDS clock source. Refer to [Section 7.1](#) for more information.

In the Reverse Loopback mode, data received from the Serial LVDS receiver is sent back to the Serial LVDS transmitter without going through the PLVDS transmit logic.

Note that loopback modes cannot be turned on at the same time as the BIST functions are turned on (BIST mode has priority over Loopback modes).

The Parallel Loopback channel sequence is shown in [Table 20](#).

**Table 20 Parallel Loopback Channel Sequence**

PLVDS Section	Incoming PLVDS Channel	Outgoing PLVDS Channel
0	PDI0[0]	PDO0[0]
	PDI0[1]	PDO0[1]
	PDI0[2]	PDO0[2]
	PDI0[3]	PDO0[3]
1	PDI1[0]	PDO1[0]
	PDI1[1]	PDO1[1]
	PDI1[2]	PDO1[2]
	PDI1[3]	PDO1[3]

Table 20 Parallel Loopback Channel Sequence (Continued)

PLVDS Section	Incoming PLVDS Channel	Outgoing PLVDS Channel
2	PDI2[0]	PDO2[0]
	PDI2[1]	PDO2[1]
	PDI2[2]	PDO2[2]
	PDI2[3]	PDO2[3]
3	PDI3[0]	PDO3[0]
	PDI3[1]	PDO3[1]
	PDI3[2]	PDO3[2]
	PDI3[3]	PDO3[3]
4	PDI4[0]	PDO4[0]
	PDI4[1]	PDO4[1]
	PDI4[2]	PDO4[2]
	PDI4[3]	PDO4[3]
5	PDI5[0]	PDO5[0]
	PDI5[1]	PDO5[1]
	PDI5[2]	PDO5[2]
	PDI5[3]	PDO5[3]
6	PDI6[0]	PDO6[0]
	PDI6[1]	PDO6[1]
	PDI6[2]	PDO6[2]
	PDI6[3]	PDO6[3]
7	PDI7[0]	PDO7[0]
	PDI7[1]	PDO7[1]
	PDI7[2]	PDO7[2]
	PDI7[3]	PDO7[3]

The Reverse Parallel Loopback channel sequence is shown in [Table 21](#).

Table 21 Reverse Parallel Loopback Channel Sequence

SLVDS Channel	Incoming SLVDS Channel	Outgoing SLVDS Channel
0	SDI[0]	SDO[0]
1	SDI[1]	SDO[1]
2	SDI[2]	SDO[2]
3	SDI[3]	SDO[3]
4	SDI[0]	SDO[0]
5	SDI[1]	SDO[1]
6	SDI[2]	SDO[2]
7	SDI[3]	SDO[3]

## 15 SPI Interface

Every M27218 device (Slave) on a card, is managed by an external controller (Master) through SPI control interface.

The protocol requires the following signals:

- **Chip Select:** every device has an associated chip select that is driven by Master as a consequence of a command (active low).
- **Tx data:** it carries the serial messages transmitted by SPI Master to every SPI Slave.
- **Rx data:** it carries the serial messages transmitted by the selected SPI Slave to SPI Master. If a Slave is not selected this output signal is forced in a high impedance state.
- **SPI clock:** it is a clock provided by SPI master, in the frequency range 100 KHz to 100 MHz. This clock is active only when a message must be exchanged; otherwise it is set to low level.

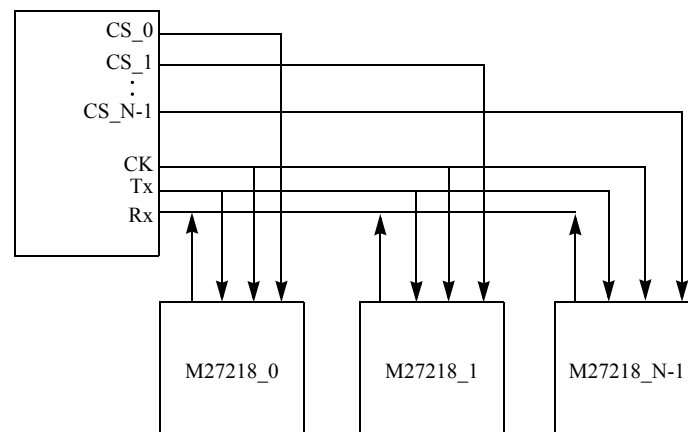


Figure 20 Links between SPI Master and (N) M27218 Slaves

### 15.1 Structure of SPI Message

The protocol is based on serial messages of 16 bits, divided into three fields:

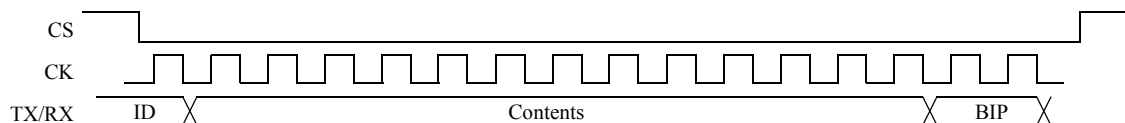


Figure 21 SPI Message Structure

**ID:** message identifier

Two kind of messages have been foreseen:

ID = 0 an address message, carrying the address of a Register

ID = 1 a data message, carrying data to be written into addressed Register.

**Contents:** message contents.

This field contains the value of transmitted address or data.

**BIP:** message BIP.

Bit 1 carries the even parity calculated on odd bits (15, 13, 11, 9, 7, 5 and 3);

That bit makes the total number of “1” bits, calculated on odd bits (bit number one included) an even number.

Bit 0 carries the odd parity calculated on even bits (14, 12, 10, 8, 6, 4 and 2);

That bit makes the total number of “1” bits, calculated on even bits (bit number zero included) an odd number.

BIP errors will be handled in the following ways. For write operation, if the address message has BIP error, the data message or messages (in the case of multiple write on consecutive addresses) will be ignored; if data message has BIP error, that particular data message and the data messages following it in the same burst will be ignored. For read operation, if the address message has BIP error, the returned data message(s) will be all “1” (including the parity bits).

Any write action to undefined registers will be ignored. Any read action to undefined registers will return all “0” (only the 13 bit content part, with the correct parity bits).

### 15.2 Basic Operations

The SPI messages allow to perform the following basic operation:

Write operation on a Register

Read operation on a Register.

#### 15.2.1 Write Operation

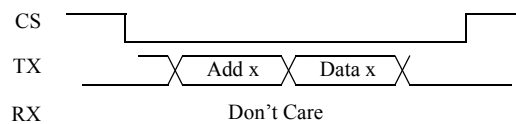
A simple write operation is performed by means of an address message followed by a data message; the first one provides the address of register to be written while the second one provides the data to be written.

A multiple write operation on not consecutive registers requires n couples of address/data messages (n=number of registers to be written).

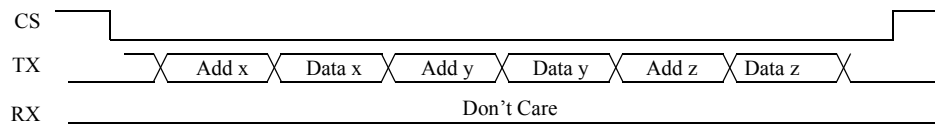
A multiple write operation on consecutive registers can be performed in a simpler way according to the following rules:

- a. The first message carries the address of the first register to be written; the address value is loaded into an internal counter.
- b. The second message carries the data to be written into the first register; at the end of this write operation the internal address counter is automatically increased and the next register is addressed.
- c. The following messages carry the data to be written in the following registers.

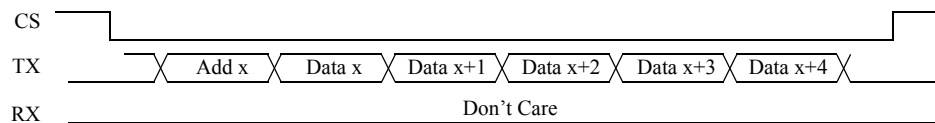
The following figures depict some examples of write operations (clock signal is not reported).



**Figure 22 Single Write Operation**



**Figure 23 Multiple Write Operation on not Consecutive Registers**



**Figure 24 Multiple Write Operation on Consecutive Registers**

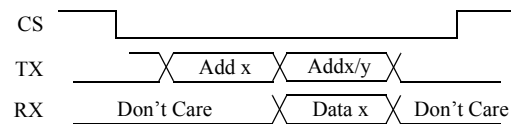
### 15.2.2 Read Operation

A simple read operation is performed by means of two address messages.

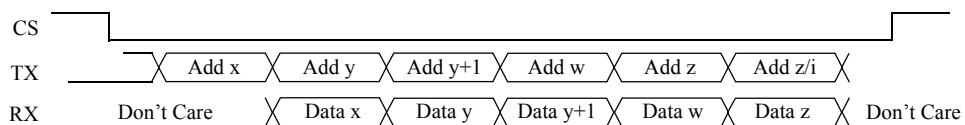
The first one provides the address of register to be read; the data of the addressed register are provided with the following message so a second meaningless address message is required.

A multiple read operation on  $n$  registers requires  $n+1$  address messages; it does not matter if the addresses are consecutive or not.

The following figures depict some examples of Read operations (clock signal is not reported).



**Figure 25 Single Read Operation**



**Figure 26 Multiple Read Operation**

### 15.2.3 Combined Operations

Read and Write operations during one continuous Chip Select active period are possible combining basic Read and Write operations described above.

## 16 Registers

The following SPI registers or register bits can have one or more of the following types: RW, RO, LH, LL, SC, RC. RW is for read and write. RO is for read only. LH is for latching high. LL is for latching low. SC is for self clear. RC is for clear on read. All the write command to the undefined registers or the reserved bits in the defined registers should be ignored. All the read command to the undefined registers or the reserved bits in the defined registers should return 0x0.

### 16.1 Device Identification Register (address = 0x0000)

Bit	Name	Type	Default Value	Description
12:8	Device_ID	RO	0x15	Device identifier
7:0	Version_ID	RO	0x0	Version identifier

### 16.2 SPI Parity Error Register (address = 0x0001)

Bit	Name	Type	Default Value	Description
12:1	Reserved			
0	Error_Flag	RO, LH, RC	0x0	Parity error flag for SPI protocol. 1 = one or more parity errors on SPI; 0 = no parity error on SPI.

### 16.3 Misc Control Register (address = 0x0002)

Bit	Name	Type	Default Value	Description
12:7	Reserved		0	
6	EQ_OffSet_PD	RW	0x0	Receiver Equalizer offset control power down control bit. 0 = not power down; 1 = power down.
5	CDR_CTRL_MODE	RW	0x0	Serial LVDS CDR phase adjustment mode control bit for all sections. 0 = normal mode. 1 = moving window mode.
4:3	Swing	RW	0x2	Swing control bits for Serial LVDS output signal. 00 = 300 mV; 01 = 500 mV; 10 = 650 mV; 11 = 800 mV.
2	CDR_Clk_Sel	RW	0x1	Parallel LVDS receiver's CDR input reference clock source selection bit. 0 = IN_CLK0 is used for PLVDS channel 0 to 15, IN_CLK1 is used for PLVDS channel 16 to 31; 1 = REFCLK is used for PLVDS channel 0 to 31;
1	Out_Clk_EN	RW	0x0	Output clock enable bit for pins OUT_CLKx (x = 0, 1, ... 7). 1 = output clocks are enabled; 0 = output clocks are not enabled.
0	Out_Clk_Sel	RW	0x0	Output clock source selection bit for pins OUT_CLKx (x = 0, 1, ... 7) as well as the clock for the logic on the receive path. 0 = local reference clock; 1 = individual Serial LVDS receiver's recovered clock.

## 16.4 Power Down Control Register

The M27218 contains 8 Power Down Control register, one for each PLVDS input and output section. For example, the register located at address 0x0180 in [Table 22](#) below contains the ability to power down any or all channels of either PLVDS input section 2, or PLVDS output section 2.

**Table 22 Power Down Control Register Addresses**

Address	PLVDS Section	Address	PLVDS Section
0x0100	0	0x0200	4
0x0140	1	0x0240	5
0x0180	2	0x0280	6
0x01C0	3	0x02C0	7

The bit assignments for these registers are shown below.

Bit	Name	Type	Default Value	Description
12	Reserved			
11	RESET_P2S	RW, SC	0	Reset control bit for the parallel to serial path (logic only, not including registers). 1 = reset; 0 = not reset.
10	RESET_S2P	RW, SC	0	Reset control bit for the serial to parallel path (logic only, not including registers). 1 = reset; 0 = not reset.
9	PWDN_P2S	RW	0x1	Power down control bit for the whole path from four Parallel LVDS input to serial LVDS output. 1 = power down; 0 = power up.
8	PWDN_S2P	RW	0x1	Power down control bit for the whole path from serial LVDS input to four Parallel LVDS output. 1 = power down; 0 = power up.
7	PD_IN_CH3	RW	0x1	Power down control bit of the input of Channel 3 of the four PLVDS I/O. 1 = power down; 0 = power up.
6	PD_IN_CH2	RW	0x1	Power down control bit of the input of Channel 2 of the four PLVDS I/O. 1 = power down; 0 = power up.
5	PD_IN_CH1	RW	0x1	Power down control bit of the input of Channel 1 of the four PLVDS I/O. 1 = power down; 0 = power up.
4	PD_IN_CH0	RW	0x1	Power down control bit of the input of Channel 0 of the four PLVDS I/O. 1 = power down; 0 = power up.
3	PD_OUT_CH3	RW	0x1	Power down control bit of the output of Channel 3 of the four PLVDS I/O. 1 = power down; 0 = power up.
2	PD_OUT_CH2	RW	0x1	Power down control bit of the output of Channel 2 of the four PLVDS I/O. 1 = power down; 0 = power up.
1	PD_OUT_CH1	RW	0x1	Power down control bit of the output of Channel 1 of the four PLVDS I/O. 1 = power down; 0 = power up.
0	PD_OUT_CH0	RW	0x1	Power down control bit of the output of Channel 0 of the four PLVDS I/O. 1 = power down; 0 = power up.

### 16.5 Serial LVDS I/O Pre-emphasis, Swing and Equalization Control Register

For Section “i” (address = 0x0101 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:6	Reserved			
5:4	Equalization	RW	0x0	Equalization level control bits for Serial LVDS input signal. 00 = weakest; ...; 11 = strongest.
3:0	Pre_Emphasis	RW	0x0	Pre-emphasis control bits for Serial LVDS output signal. 0000 = weakest; ...; 1111 = strongest.

### 16.6 Parallel LVDS CDR Control Register

For Section “i” (address = 0x0102+0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:3	Reserved			
2	Adj_Mode	RW	0x0	1 = Manual Alignment Mode.
1	Adj_Dir	RW	0x0	Phase adjustment direction control bit for PLVDS receiver’s CDR. When Adj_Mode = 1, 1 = adjust to the forward direction in time; 0 = adjust to the backward direction in time.
0	Adjust	RW, SC	0x0	Phase adjustment activate control bit for PLVDS receiver’s CDR. When Adj_Mode = 1, writing a “1” to this bit will cause the CDR to adjust the recovered clock phase by about 25 ps; writing a “0” is ignored. When Adj_Mode = 0, this is a don’t care bit. This bit is a self clear bit.

## 16.7 Serial LVDS CDR Control Register

For Section “i” (address = 0x0103+0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:7	Reserved			
6	VTRX_DIS- CONN	RW	0x0	VTRX (receive termination voltage) disconnect control bit. 1 = disconnect (VTRX is not applied to the receive termination resistors). This mode is used when interfacing with an LVDS transmitter; 0 = connect (VTRX is applied to the receive termination resistors). This mode is used when interfacing with a CML transmitter.
5:4	Data_Rate	RW	0x2	00 = serial interface @622Mbps 01 = reserved 10 = serial interface @2.488Gbps 11 = Reserved
3	Byte_Align	RW, SC	0x0	CDR big phase adjustment of one bit for byte alignment control bit. Writing a “1” to this bit causes the Serial LVDS receive channel of this section to shift its “byte” boundary (4 bits of 2.488G is one byte in Full Speed mode) for serial to parallel conversion by one bit.
2	Adj_Mode	RW	0x0	1 = Manual Alignment Mode.
1	Adj_Dir	RW	0x0	Phase adjustment direction control bit for SLVDS receiver’s CDR. When Adj_Mode = 1, 1 = adjust to the forward direction in time; 0 = adjust to the backward direction in time. When Adj_Mode = 0, this is a don’t care bit.
0	Adjust	RW, SC	0x0	Phase adjustment activate control bit for SLVDS receiver’s CDR. When Adj_Mode = 1, writing a “1” to this bit will cause the CDR to adjust the recovered clock phase by 25 ps; writing a “0” is ignored. When Adj_Mode = 0, this is a don’t care bit. This bit is a self clear bit.

## 16.8 Parallel to Serial Path Bit Aligner Control Register

For Section “i” (address = 0x0104 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	Reserved			
11:9	CH3_Shift	RW	0x0	Channel 3 bit shift value control bits. 000 = shift 0 bit; . . . ; 111 = shift 7 bits.
8:6	CH2_Shift	RW	0x0	Channel 2 bit shift value control bits. 000 = shift 0 bit; . . . ; 111 = shift 7 bits.
5:3	CH1_Shift	RW	0x0	Channel 1 bit shift value control bits. 000 = shift 0 bit; . . . ; 111 = shift 7 bits.
2:0	CH0_Shift	RW	0x0	Channel 0 bit shift value control bits. 000 = shift 0 bit; . . . ; 111 = shift 7 bits.

### 16.9 Serial to Parallel Path Bit Aligner Control Register

For Section “i” (address = 0x0105 + 0x0040\*i, i = 0 ...7)

Bit	Name	Type	Default Value	Description
12	Reserved			
11:9	CH3_Shift	RW	0x0	Channel 3 bit shift value control bits. 000 = shift 0 bit; ...; 111 = shift 7 bits.
8:6	CH2_Shift	RW	0x0	Channel 2 bit shift value control bits. 000 = shift 0 bit; ...; 111 = shift 7 bits.
5:3	CH1_Shift	RW	0x0	Channel 1 bit shift value control bits. 000 = shift 0 bit; ...; 111 = shift 7 bits.
2:0	CH0_Shift	RW	0x0	Channel 0 bit shift value control bits. 000 = shift 0 bit; ...; 111 = shift 7 bits.

### 16.10 Parallel to Serial Path Bit Counter Control Register 1

For Section “i” (address = 0x0106 + 0x0040\*i, i = 0 ... 7)

Bit	Name	Type	Default Value	Description
12	Monitor_EN	RW	0x0	Enable control bit for the monitoring function on parallel to serial path for this section. 1 = enabled; 0 = disabled (clock input to the Bit Monitoring related logic is stopped). A zero to one transition on this bit will reset the NewData_Flag and Bit Counter to zero.
11	Reserved			
10	Force_Reset	RW		0x0 Bit Counter force reset control bit. 1 = reset the Bit Counter to zero; 0 = not reset the Bit Counter to zero.
9	Frame_Sync_Reset_EN	RW	0x0	Bit Counter reset by external Frame Sync signal (pin FRAME_SYNC) enable control bit. 1 = enable the reset of the Bit Counter by the Frame Sync signal; 0 = disable the reset of the Bit Counter by the Frame Sync signal.
8:5	Reserved			
4:0	Reset_Value_17_13	RW	0x09	Bit [17:13] of the 18 bit Bit Counter reset value. After the Bit Counter reaches this value (combined with Register 0), it wraps around to zero.

### 16.11 Parallel to Serial Path Bit Counter Control Register 0

For Section “i” (address = 0x0107 + 0x0040\*i, i = 0 ... 7)

Bit	Name	Type	Default Value	Description
12:0	Reset_Value_12_0	RW	0x0FBF	Bit [12:0] of the 18 bit Bit Counter reset value. After the Bit Counter reaches this value (combined with Register 1), it wraps around to zero.

### 16.12 Serial to Parallel Path Bit Counter Control Register 1

For Section “i” (address = 0x0108 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	Monitor_EN	RW	0x0	Enable control bit for the monitoring function on serial to parallel path for this section. 1 = enabled; 0 = disabled (clock input to the Bit Monitoring related logic is stopped). A zero to one transition on this bit will reset the NewData_Flag and Bit Counter to zero.
11	Reserved			
10	Force_Reset	RW	0x0	Bit Counter force reset control bit. 1 = reset the Bit Counter to zero; 0 = not reset the Bit Counter to zero.
9	Frame_Sync_Reset_EN	RW	0x0	Bit Counter reset by external Frame Sync signal (pin FRAME_SYNC) enable control bit. 1 = enable the reset of the Bit Counter by the Frame Sync signal; 0 = disable the reset of the Bit Counter by the Frame Sync signal.
8:5	Reserved			
4:0	Reset_Value_17_13	RW	0x09	Bit [17:13] of the 18 bit Bit Counter reset value. After the Bit Counter reaches this value (combined with Register 0), it wraps around to zero.

### 16.13 Serial to Parallel Path Bit Counter Control Register 0

For Section “i” (address = 0x0109 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:0	Reset_Value_12_0	RW	0x0FBF	Bit [12:0] of the 18 bit Bit Counter reset value. After the Bit Counter reaches this value (combined with Register 1), it wraps around to zero.

### 16.14 Parallel to Serial Path Bit Monitor Trigger Position Register 1

For Section “i” (address = 0x010A + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:5	Reserved			
4:0	TRIG_POS_17_13	RW	0x0	Bit [17:13] of the 18 bit Bit Monitor trigger position. When the Bit Counter reaches this value (combined with Register 0), the current 12 bit value of each of the four Parallel LVDS channel will be latched to Bit Monitor Registers.

**16.15 Parallel to Serial Path Bit Monitor Trigger Position Register 0**

For Section “i” (address = 0x010B + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:0	TRIG_POS_12_0	RW	0x0	Bit [12:0] of the 18 bit Bit Monitor trigger position. When the Bit Counter reaches this value (combined with Register 1), the current 12 bit value of each of the four Parallel LVDS channel will be latched to Bit Monitor Registers.

**16.16 Serial to Parallel Path Bit Monitor Trigger Position Register 1**

For Section “i” (address = 0x010C + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:5	Reserved			
4:0	TRIG_POS_17_13	RW	0x0	Bit [17:13] of the 18 bit Bit Monitor trigger position. When the Bit Counter reaches this value (combined with Register 0), the current 12 bit value of each of the four Parallel LVDS channel will be latched to Bit Monitor Registers.

**16.17 Serial to Parallel Path Bit Monitor Trigger Position Register 0**

For Section “i” (address = 0x010D + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:0	TRIG_POS_12_0	RW	0x0	Bit [12:0] of the 18 bit Bit Monitor trigger position. When the Bit Counter reaches this value (combined with Register 1), the current 12 bit value of each of the four Parallel LVDS channel will be latched to Bit Monitor Registers.

**16.18 Parallel to Serial Bit Monitor Register**

For Channel 3 of Section “i” (address = 0x010E + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	NewData_Flag	RO	0x0	Flag bit for newly latched data in the bit [11:0] of this register. A change from “0” to “1” or from “1” to “0” on this bit indicate that a new set of data (12 bit) is latched in.
11:0	Latched_Data	RO	0x0	12 bit data captured for this channel after the trigger position is reached for this section.

### 16.19 Parallel to Serial Bit Monitor Register

For Channel 2 of Section “i” (address = 0x010F + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	NewData_Flag	RO	0x0	Flag bit for newly latched data in the bit [11:0] of this register. A change from “0” to “1” or from “1” to “0” on this bit indicate that a new set of data (12 bit) is latched in.
11:0	Latched_Data	RO	0x0	12 bit data captured for this channel after the trigger position is reached for this section.

### 16.20 Parallel to Serial Bit Monitor Register

For Channel 1 of Section “i” (address = 0x0110 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	NewData_Flag	RO	0x0	Flag bit for newly latched data in the bit [11:0] of this register. A change from “0” to “1” or from “1” to “0” on this bit indicate that a new set of data (12 bit) is latched in.
11:0	Latched_Data	RO	0x0	12 bit data captured for this channel after the trigger position is reached for this section.

### 16.21 Parallel to Serial Bit Monitor Register

For Channel 0 of Section “i” (address = 0x0111 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	NewData_Flag	RO	0x0	Flag bit for newly latched data in the bit [11:0] of this register. A change from “0” to “1” or from “1” to “0” on this bit indicate that a new set of data (12 bit) is latched in.
11:0	Latched_Data	RO	0x0	12 bit data captured for this channel after the trigger position is reached for this section.

### 16.22 Serial to Parallel Bit Monitor Register

For Channel 3 of Section “i” (address = 0x0112 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	NewData_Flag	RO	0x0	Flag bit for newly latched data in the bit [11:0] of this register. A change from “0” to “1” or from “1” to “0” on this bit indicate that a new set of data (12 bit) is latched in.
11:0	Latched_Data	RO	0x0	12 bit data captured for this channel after the trigger position is reached for this section.

### 16.23 Serial to Parallel Bit Monitor Register

For Channel 2 of Section “i” (address = 0x0113 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	NewData_Flag	RO	0x0	Flag bit for newly latched data in the bit [11:0] of this register. A change from “0” to “1” or from “1” to “0” on this bit indicate that a new set of data (12 bit) is latched in.
11:0	Latched_Data	RO	0x0	12 bit data captured for this channel after the trigger position is reached for this section.

### 16.24 Serial to Parallel Bit Monitor Register

For Channel 1 of Section “i” (address = 0x0114 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	NewData_Flag	RO	0x0	Flag bit for newly latched data in the bit [11:0] of this register. A change from “0” to “1” or from “1” to “0” on this bit indicate that a new set of data (12 bit) is latched in.
11:0	Latched_Data	RO	0x0	12 bit data captured for this channel after the trigger position is reached for this section.

### 16.25 Serial to Parallel Bit Monitor Register

For Channel 0 of Section “i” (address = 0x0115 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	NewData_Flag	RO	0x0	Flag bit for newly latched data in the bit [11:0] of this register. A change from “0” to “1” or from “1” to “0” on this bit indicate that a new set of data (12 bit) is latched in.
11:0	Latched_Data	RO	0x0	12 bit data captured for this channel after the trigger position is reached for this section.

## 16.26 Parallel to Serial Output Bit-Sequence Control Register - PLVDS Input Channels 3 & 2

Of Section “i” (address = 0x0116 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:9	Reserved			
8:5	Input_Sel3	RW	0x3	Input PLVDS data channel select for [bit 3] (MSB) of the SLVDS 4-bit sequence. When BIST_GEN = 1 for this Section, these bits are don't care bits. 0000 = select input channel 0 0001 = select input channel 1 0010 = select input channel 2 0011 = select input channel 3 0100 = select reverse loopback channel 0 0101 = select reverse loopback channel 1 0110 = select reverse loopback channel 2 0111 = select reverse loopback channel 3 1000 = select all “0” as the output data
4	Reserved			
3:0	Input_Sel2	RW	0x2	Input PLVDS data channel select for [bit 2] of the SLVDS 4-bit sequence. When BIST_GEN = 1 for this Section, these bits are don't care bits. 0000 = select input channel 0 0001 = select input channel 1 0010 = select input channel 2 0011 = select input channel 3 0100 = select reverse loopback channel 0 0101 = select reverse loopback channel 1 0110 = select reverse loopback channel 2 0111 = select reverse loopback channel 3 1000 = select all “0” as the output data

SLVDS 4-bit sequence is defined as: [bit<sub>3(msb)</sub>] [bit<sub>2</sub>] [bit<sub>1</sub>] [bit<sub>0(lsb)</sub>], data moving from left to right.

... c<sub>3</sub> c<sub>2</sub> c<sub>1</sub> c<sub>0</sub> b<sub>3</sub> b<sub>2</sub> b<sub>1</sub> b<sub>0</sub> a<sub>3</sub> a<sub>2</sub> a<sub>1</sub> a<sub>0</sub>

## 16.27 Parallel to Serial Output Bit-Sequence Control Register - PLVDS Input Channels 1 &amp; 0

Of section “i” (address = 0x0117 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:9	Reserved			
8:5	Input_Sel1	RW	0x1	Input PLVDS data channel select for [bit 1] of the SLVDS 4-bit sequence. When BIST_GEN = 1 for this Section, these bits are don't care bits. 0000 = select input channel 0 0001 = select input channel 1 0010 = select input channel 2 0011 = select input channel 3 0100 = select reverse loopback channel 0 0101 = select reverse loopback channel 1 0110 = select reverse loopback channel 2 0111 = select reverse loopback channel 3 1000 = select all “0” as the output data
4	Reserved			
3:0	Input_Sel0	RW	0x0	Input PLVDS data channel select for [bit 0] (LSB) of the SLVDS 4-bit sequence. When BIST_GEN = 1 for this Section, these bits are don't care bits. 0000 = select input channel 0 0001 = select input channel 1 0010 = select input channel 2 0011 = select input channel 3 0100 = select reverse loopback channel 0 0101 = select reverse loopback channel 1 0110 = select reverse loopback channel 2 0111 = select reverse loopback channel 3 1000 = select all “0” as the output data

SLVDS 4-bit sequence is defined as: [bit<sub>3(msb)</sub>] [bit<sub>2</sub>] [bit<sub>1</sub>] [bit<sub>0(lsb)</sub>], data moving from left to right.

... c<sub>3</sub> c<sub>2</sub> c<sub>1</sub> c<sub>0</sub> b<sub>3</sub> b<sub>2</sub> b<sub>1</sub> b<sub>0</sub> a<sub>3</sub> a<sub>2</sub> a<sub>1</sub> a<sub>0</sub>

## 16.28 Serial Input Bit-Sequence to Parallel Outputs Control Register - Output Channels 3 & 2

Of Section “i” (address = 0x0118 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:9	Reserved			
8:5	Output_Sel3	RW	0x3	Output PLVDS data channel select for [bit 3] (MSB) of the SLVDS 4-bit sequence. 0000 = select output channel 0 0001 = select output channel 1 0010 = select output channel 2 0011 = select output channel 3 0100 = select parallel loopback channel 0 0101 = select parallel loopback channel 1 0110 = select parallel loopback channel 2 0111 = select parallel loopback channel 3 1000 = select all “0” as the output data
4	Reserved			
3:0	Output_Sel2	RW	0x2	Output PLVDS data channel select for [bit 2] of the SLVDS 4-bit sequence. 0000 = select output channel 0 0001 = select output channel 1 0010 = select output channel 2 0011 = select output channel 3 0100 = select parallel loopback channel 0 0101 = select parallel loopback channel 1 0110 = select parallel loopback channel 2 0111 = select parallel loopback channel 3 1000 = select all “0” as the output data

SLVDS 4-bit sequence is defined as: [bit<sub>3(msb)</sub>] [bit<sub>2</sub>] [bit<sub>1</sub>] [bit<sub>0(lsb)</sub>], data moving from left to right.

... c<sub>3</sub> c<sub>2</sub> c<sub>1</sub> c<sub>0</sub> b<sub>3</sub> b<sub>2</sub> b<sub>1</sub> b<sub>0</sub> a<sub>3</sub> a<sub>2</sub> a<sub>1</sub> a<sub>0</sub>

### 16.29 Serial Input Bit-Sequence to Parallel Outputs Control Register - Output Channels 1 & 0

Of Section “i” (address = 0x0119 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:9	Reserved			
8:5	Output_Sel1	RW	0x1	Output PLVDS data channel select for [bit 1] of the SLVDS 4-bit sequence. 0000 = select output channel 0 0001 = select output channel 1 0010 = select output channel 2 0011 = select output channel 3 0100 = select parallel loopback channel 0 0101 = select parallel loopback channel 1 0110 = select parallel loopback channel 2 0111 = select parallel loopback channel 3 1000 = select all “0” as the output data
4	Reserved			
3:0	Output_Sel0	RW	0x0	Output PLVDS data channel select for [bit 0] (LSB) of the SLVDS 4-bit sequence. 0000 = select output channel 0 0001 = select output channel 1 0010 = select output channel 2 0011 = select output channel 3 0100 = select parallel loopback channel 0 0101 = select parallel loopback channel 1 0110 = select parallel loopback channel 2 0111 = select parallel loopback channel 3 1000 = select all “0” as the output data

SLVDS 4-bit sequence is defined as: [bit<sub>3(msb)</sub>] [bit<sub>2</sub>] [bit<sub>1</sub>] [bit<sub>0(lsb)</sub>], data moving from left to right.

... c<sub>3</sub> c<sub>2</sub> c<sub>1</sub> c<sub>0</sub> b<sub>3</sub> b<sub>2</sub> b<sub>1</sub> b<sub>0</sub> a<sub>3</sub> a<sub>2</sub> a<sub>1</sub> a<sub>0</sub>

### 16.30 Parallel LVDS BIST Pattern Generation Control Register

For Section “i” (address = 0x011A+0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:5	Reserved			
4	BIST_GEN_SECT	RW	0x0	All channels in the section BIST pattern generation control bit. 1 = generate BIST pattern; 0 = not generate BIST pattern.
3	BIST_GEN_CH3	RW	0x0	Channel 3 BIST pattern generation control bit. 1 = generate BIST pattern; 0 = not generate BIST pattern.
2	BIST_GEN_CH2	RW	0x0	Channel 2 BIST pattern generation control bit. 1 = generate BIST pattern; 0 = not generate BIST pattern.
1	BIST_GEN_CH1	RW	0x0	Channel 1 BIST pattern generation control bit. 1 = generate BIST pattern; 0 = not generate BIST pattern.
0	BIST_GEN_CH0	RW	0x0	Channel 0 BIST pattern generation control bit. 1 = generate BIST pattern; 0 = not generate BIST pattern.

### 16.31 Parallel LVDS BIST Pattern CID (Contiguous Identical Digit) Insertion Control Register

For Section “i” (address = 0x011B+0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	Zero_Insert	RW	0x0	“0” insertion control bit in BIST pattern generation. 1 = insert a sequence of “0x00” in-between the frame header and payload in the BIST pattern and the length of the sequence is defined by CID_LENGTH in the same register. If both Zero_Insert and One_Insert are “1”, 0xFF will be inserted.
11	One_Insert	RW	0x0	“1” insertion control bit in BIST pattern generation. 1 = insert a sequence of “0xFF” in-between the frame header and payload in the BIST pattern and the length of the sequence is defined by CID_LENGTH in the same register. If both Zero_Insert and One_Insert are “1”, 0xFF will be inserted.
10	Reserved			
9:0	CID_LENGTH	RW	0x000	Number of bytes of CID (0’s or 1’s) to be inserted into BIST pattern when either Zero_Insert or One_Insert is “1”.

### 16.32 Parallel LVDS BIST Pattern Checking Control Register

For Section “i” (address = 0x011C + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:4	Reserved			
3	BIST_CHK_CH3	RW	0x0	Channel 3 BIST pattern checking control bit. 1 = check for BIST pattern; 0 = not check for BIST pattern. If more than one channel’s BIST pattern checking is turned on, only the checking for the channel with the smaller channel index will be performed.
2	BIST_CHK_CH2	RW	0x0	Channel 2 BIST pattern checking control bit. 1 = check for BIST pattern; 0 = not check for BIST pattern. If more than one channel’s BIST pattern checking is turned on, only the checking for the channel with the smaller channel index will be performed.
1	BIST_CHK_CH1	RW	0x0	Channel 1 BIST pattern checking control bit. 1 = check for BIST pattern; 0 = not check for BIST pattern. If more than one channel’s BIST pattern checking is turned on, only the checking for the channel with the smaller channel index will be performed.
0	BIST_CHK_CH0	RW	0x0	Channel 0 BIST pattern checking control bit. 1 = check for BIST pattern; 0 = not check for BIST pattern. If more than one channel’s BIST pattern checking is turned on, only the checking for the channel with the smaller channel index will be performed.

### 16.33 Parallel LVDS BIST Pattern CID (Contiguous Identical Digit) Checking Control Register

For Section “i” (address = 0x011D+0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	Zero_Insert	RW	0x0	“0” insertion check control bit in BIST pattern checking. 1 = check for sequence of “0x00” in-between the frame header and payload in the BIST pattern and the length of the sequence is defined by CID_LENGTH in the same register. If both Zero_Insert and One_Insert are “1”, 0xFF will be checked for.
11	One_Insert	RW	0x0	“1” insertion check control bit in BIST pattern checking. 1 = check for sequence of “0xFF” in-between the frame header and payload in the BIST pattern and the length of the sequence is defined by CID_LENGTH in the same register. If both Zero_Insert and One_Insert are “1”, 0xFF will be checked for.
10	Reserved			
9:0	CID_LENGTH	RW	0x000	Number of bytes of CID (0’s or 1’s) to be checked for in BIST pattern when either Zero_Insert or One_Insert is “1”.

### 16.34 Parallel BIST Error Counter Register

For Section “i” (address = 0x011E + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:0	Err_Count	RO, WC	0x0	Parallel BIST error counter. BIST error counter contains the number of erroneous dual-bit (2 bits to be compared at each clock) accumulated since the last time the BIST checking is turned on (at which time the counter is reset to zero) for a channel or since the last time this counter is written with any value (at which time the counter is also reset to zero). This counter should keep the value and not wrap around to zero after it reaches its maximal value.

### 16.35 Parallel BIST Frame Loss Flag Register

For Section “i” (address = 0x011F + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:1	Reserved			
0	LOF_Flag	RO, LH, WC	0x0	Loss of frame flag bit. 1 = at least one frame header did not appear at the expected position or not a single frame header has been detected since last time the BIST checking is turned on (at which time this bit is set to “1” and reset to “0” after the first frame header is found) for this channel or this bit is written with any value at which time this bit is cleared. 0 = all the frame headers appear at the expected positions.

### 16.36 Serial BIST Pattern Generation Control Register

For Section “i” (address = 0x0120 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	BIST_GEN	RW	0x0	BIST pattern generation control bit for the section. 1 = generate BIST pattern; 0 = not generate BIST pattern.
11	Zero_Insert	RW	0x0	“0” insertion control bit in BIST pattern generation. 1 = insert a sequence of “0x00” in-between the frame header and payload in the BIST pattern and the length of the sequence is defined by CID_LENGTH in the same register. If both Zero_Insert and One_Insert are “1”, 0xFF will be inserted.
10	One_Insert	RW	0x0	“1” insertion control bit in BIST pattern generation. 1 = insert a sequence of “0xFF” in-between the frame header and payload in the BIST pattern and the length of the sequence is defined by CID_LENGTH in the same register. If both Zero_Insert and One_Insert are “1”, 0xFF will be inserted.
9:0	CID_LENGTH	RW	0x000	Number of bytes of CID (0’s or 1’s) to be inserted into BIST pattern when either Zero_Insert or One_Insert is “1”.

### 16.37 Serial BIST Pattern Checking Control Register

For Section “i” (address = 0x0121 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12	BIST_CHK	RW	0x0	BIST pattern checking control bit for the section. 1 = check for BIST pattern; 0 = not check for BIST pattern.
11	Zero_Insert	RW	0x0	“0” insertion control bit in BIST pattern checking. 1 = check for sequence of “0x00” in-between the frame header and payload in the BIST pattern and the length of the sequence is defined by CID_LENGTH in the same register. If both Zero_Insert and One_Insert are “1”, 0xFF will be checked for.
10	One_Insert	RW	0x0	“1” insertion control bit in BIST pattern checking. 1 = check for sequence of “0xFF” in-between the frame header and payload in the BIST pattern and the length of the sequence is defined by CID_LENGTH in the same register. If both Zero_Insert and One_Insert are “1”, 0xFF will be checked for.
9:0	CID_LENGTH	RW	0x000	Number of bytes of CID (0’s or 1’s) to be checked for in BIST pattern when either Zero_Insert or One_Insert is “1”.

### 16.38 Serial BIST Error Counter Register

For Section “i” (address = 0x0122 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:0	Err_Count	RO, WC	0x0	Serial BIST error counter. BIST error counter contains the number of erroneous bytes accumulated since the last time the BIST checking is turned on (at which time the counter is reset to zero) or since the last time this counter is written with any value (at which time the counter is also reset to zero). This counter should keep the value and not wrap around to zero after it reaches its maximal value.

### 16.39 Serial BIST Frame Loss Flag Register

For Section “i” (address = 0x0123 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:1	Reserved			
0	LOF_Flag	RO, LH, WC	0x0	Loss of frame flag bit. 1 = at least one frame header did not appear at the expected position or not a single frame header has been detected since last time the BIST checking is turned on (at which time this bit is set to “1” and reset to “0” after the first frame header is found) or this bit is written with any value at which time this bit is cleared. 0 = all the frame headers appear at the expected positions.

### 16.40 BIST PRBS Seed Register 1

For Section “i” (address = 0x0125 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:2	Reserved			
1:0	SEED_14_13	RW	0x3	Bit [14:13] of BIST PRBS seed value. All “0” in Seed Register 1 and 0 is illegal.

### 16.41 BIST PRBS Seed Register 0

For Section “i” (address = 0x0126 + 0x0040\*i, i = 0 . . . 7)

Bit	Name	Type	Default Value	Description
12:0	SEED_12_0	RW	0x1fff	Bit [12:0] of BIST PRBS seed value. All “0” in Seed Register 1 and 0 is illegal.

## 17 Pin Definitions

Table 23 lists the external pins of the M27218 device.

**Table 23 Pin Definitions**

Name	Type	I/O	Default Value	Description
<b>Parallel LVDS Signal Pins</b>				
PDO0[0]P PDO0[0]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 0 of section 0.
PDO0[1]P PDO0[1]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 1 of section 0.
PDO0[2]P PDO0[2]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 2 of section 0.
PDO0[3]P PDO0[3]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 3 of section 0.
PDO1[0]P PDO1[0]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 0 of section 1.
PDO1[1]P PDO1[1]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 1 of section 1.
PDO1[2]P PDO1[2]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 2 of section 1.
PDO1[3]P PDO1[3]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 3 of section 1.
PDO2[0]P PDO2[0]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 0 of section 2.
PDO2[1]P PDO2[1]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 1 of section 2.
PDO2[2]P PDO2[2]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 2 of section 2.
PDO2[3]P PDO2[3]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 3 of section 2.
PDO3[0]P PDO3[0]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 0 of section 3.
PDO3[1]P PDO3[1]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 1 of section 3.
PDO3[2]P PDO3[2]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 2 of section 3.
PDO3[3]P PDO3[3]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 3 of section 3.
PDO4[0]P PDO4[0]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 0 of section 4.
PDO4[1]P PDO4[1]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 1 of section 4.
PDO4[2]P PDO4[2]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 2 of section 4.
PDO4[3]P PDO4[3]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 3 of section 4.
PDO5[0]P PDO5[0]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 0 of section 5.

Table 23 Pin Definitions (Continued)

Name	Type	I/O	Default Value	Description
PDO5[1]P PDO5[1]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 1 of section 5.
PDO5[2]P PDO5[2]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 2 of section 5.
PDO5[3]P PDO5[3]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 3 of section 5.
PDO6[0]P PDO6[0]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 0 of section 6.
PDO6[1]P PDO6[1]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 1 of section 6.
PDO6[2]P PDO6[2]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 2 of section 6.
PDO6[3]P PDO6[3]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 3 of section 6.
PDO7[0]P PDO7[0]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 0 of section 7.
PDO7[1]P PDO7[1]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 1 of section 7.
PDO7[2]P PDO7[2]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 2 of section 7.
PDO7[3]P PDO7[3]N	LVDS	O	N/A	Differential transmit data for PLVDS output channel 3 of section 7.
PDI0[0]P PDI0[0]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 0 of Section 0.
PDI0[1]P PDI0[1]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 1 of Section 0.
PDI0[2]P PDI0[2]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 2 of Section 0.
PDI0[3]P PDI0[3]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 3 of Section 0.
PDI1[0]P PDI1[0]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 0 of Section 1.
PDI1[1]P PDI1[1]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 1 of Section 1.
PDI1[2]P PDI1[2]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 2 of Section 1.
PDI1[3]P PDI1[3]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 3 of Section 1.
PDI2[0]P PDI2[0]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 0 of Section 2.
PDI2[1]P PDI2[1]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 1 of Section 2.
PDI2[2]P PDI2[2]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 2 of Section 2.
PDI2[3]P PDI2[3]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 3 of Section 2.

Table 23 Pin Definitions (Continued)

Name	Type	I/O	Default Value	Description
PDI3[0]P PDI3[0]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 0 of Section 3.
PDI3[1]P PDI3[1]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 1 of Section 3.
PDI3[2]P PDI3[2]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 2 of Section 3.
PDI3[3]P PDI3[3]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 3 of Section 3.
PDI4[0]P PDI4[0]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 0 of Section 4.
PDI4[1]P PDI4[1]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 1 of Section 4.
PDI4[2]P PDI4[2]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 2 of Section 4.
PDI4[3]P PDI4[3]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 3 of Section 4.
PDI5[0]P PDI5[0]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 0 of Section 5.
PDI5[1]P PDI5[1]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 1 of Section 5.
PDI5[2]P PDI5[2]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 2 of Section 5.
PDI5[3]P PDI5[3]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 3 of Section 5.
PDI6[0]P PDI6[0]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 0 of Section 6.
PDI6[1]P PDI6[1]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 1 of Section 6.
PDI6[2]P PDI6[2]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 2 of Section 6.
PDI6[3]P PDI6[3]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 3 of Section 6.
PDI7[0]P PDI7[0]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 0 of Section 7.
PDI7[1]P PDI7[1]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 1 of Section 7.
PDI7[2]P PDI7[2]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 2 of Section 7.
PDI7[3]P PDI7[3]N	LVDS	I	N/A	Differential receive data for PLVDS input channel 3 of Section 7.
IN_CLK0P IN_CLK0N	LVDS	I	N/A	Differential input reference clock for CDR of Channel 0 to 15 of Parallel LVDS receivers when CDR_Clk_Sel = 0. The frequency should be the same as the data rate on one LVDS channel. For example, if the data rate on one LVDS channel is 622 Mbps, the frequency of this clock should be 622 MHz. When CDR_Clk_Sel = 1 there are don't care pins.

Table 23 Pin Definitions (Continued)

Name	Type	I/O	Default Value	Description
IN_CLK1P IN_CLK1N	LVDS	I	N/A	Differential input reference clock for CDR of Channel 16 to 31 of Parallel LVDS receivers when CDR_Clk_Sel = 0. The frequency should be the same as the data rate on one LVDS channel. For example, if the data rate on one LVDS channel is 622 Mbps, the frequency of this clock should be 622 MHz. When CDR_Clk_Sel = 1 there are don't care pins.
OUT_CLK0P OUT_CLK0N	LVDS	O	N/A	Differential output clock for Channel 0 to 3 of the 32 LVDS channels' transmit data. The frequency should be the same as the data rate on one LVDS channel. For example, if the data rate on one LVDS channel is 622 Mbps, the frequency of this clock should be 622 MHz.
OUT_CLK1P OUT_CLK1N	LVDS	O	N/A	Differential output clock for Channel 4 to 7 of the 32 LVDS channels' transmit data. The frequency should be the same as the data rate on one LVDS channel. For example, if the data rate on one LVDS channel is 622 Mbps, the frequency of this clock should be 622 MHz.
OUT_CLK2P OUT_CLK2N	LVDS	O	N/A	Differential output clock for Channel 8 to 11 of the 32 LVDS channels' transmit data. The frequency should be the same as the data rate on one LVDS channel. For example, if the data rate on one LVDS channel is 622 Mbps, the frequency of this clock should be 622 MHz.
OUT_CLK3P OUT_CLK3N	LVDS	O	N/A	Differential output clock for Channel 12 to 15 of the 32 LVDS channels' transmit data. The frequency should be the same as the data rate on one LVDS channel. For example, if the data rate on one LVDS channel is 622 Mbps, the frequency of this clock should be 622 MHz.
OUT_CLK4P OUT_CLK4N	LVDS	O	N/A	Differential output clock for Channel 16 to 19 of the 32 LVDS channels' transmit data. The frequency should be the same as the data rate on one LVDS channel. For example, if the data rate on one LVDS channel is 622 Mbps, the frequency of this clock should be 622 MHz.
OUT_CLK5P OUT_CLK5N	LVDS	O	N/A	Differential output clock for Channel 20 to 23 of the 32 LVDS channels' transmit data. The frequency should be the same as the data rate on one LVDS channel. For example, if the data rate on one LVDS channel is 622 Mbps, the frequency of this clock should be 622 MHz.
OUT_CLK6P OUT_CLK6N	LVDS	O	N/A	Differential output clock for Channel 24 to 27 of the 32 LVDS channels' transmit data. The frequency should be the same as the data rate on one LVDS channel. For example, if the data rate on one LVDS channel is 622 Mbps, the frequency of this clock should be 622 MHz.
OUT_CLK7P OUT_CLK7N	LVDS	O	N/A	Differential output clock for Channel 28 to 31 of the 32 LVDS channels' transmit data. The frequency should be the same as the data rate on one LVDS channel. For example, if the data rate on one LVDS channel is 622 Mbps, the frequency of this clock should be 622 MHz.
REFCLKP REFCLKN	LVDS	I	N/A	Differential local reference clock input. The frequency of this clock should be one-fourth of the data rate on one Serial LVDS channel. For example, if the data rate on one Serial LVDS channel is 2.488 Gbps, the frequency of this clock should be 622MHz.
<b>Serial LVDS Signal Pins</b>				
SDO0P SDO0N	LVDS	O	N/A	Differential transmit data for SLVDS output channel 0.
SDO1P SDO1N	LVDS	O	N/A	Differential transmit data for SLVDS output channel 1.

Table 23 Pin Definitions (Continued)

Name	Type	I/O	Default Value	Description
SDO2P SDO2N	LVDS	O	N/A	Differential transmit data for SLVDS output channel 2.
SDO3P SDO3N	LVDS	O	N/A	Differential transmit data for SLVDS output channel 3.
SDO4P SDO4N	LVDS	O	N/A	Differential transmit data for SLVDS output channel 4.
SDO5P SDO5N	LVDS	O	N/A	Differential transmit data for SLVDS output channel 5.
SDO6P SDO6N	LVDS	O	N/A	Differential transmit data for SLVDS output channel 6.
SDO7P SDO7N	LVDS	O	N/A	Differential transmit data for SLVDS output channel 7.
SDI0P SDI0N	LVDS	I	N/A	Differential receive data for SLVDS input channel 0.
SDI1P SDI1N	LVDS	I	N/A	Differential receive data for SLVDS input channel 1.
SDI2P SDI2N	LVDS	I	N/A	Differential receive data for SLVDS input channel 2.
SDI3P SDI3N	LVDS	I	N/A	Differential receive data for SLVDS input channel 3.
SDI4P SDI4N	LVDS	I	N/A	Differential receive data for SLVDS input channel 4.
SDI5P SDI5N	LVDS	I	N/A	Differential receive data for SLVDS input channel 5.
SDI6P SDI6N	LVDS	I	N/A	Differential receive data for SLVDS input channel 6.
SDI7P SDI7N	LVDS	I	N/A	Differential receive data for SLVDS input channel 7.
<b>LVTTTL Control Signal Pins</b>				
SPI_CS	LVTTTL	I	1	SPI Chip Select signal pin. 0 = chip is selected; 1 = chip is not selected.
SPI_CLK	LVTTTL	I	1	SPI clock input pin. The frequency of this clock may range from 100 KHz to 100 MHz. This clock is considered valid only when SPI_CS is 0.
SPI_RX	LVTTTL	O, TRI	1	SPI serial receive data pin (from SPI master point of view).
SPI_TX	LVTTTL	I	1	SPI serial transmit data pin (from SPI master point of view).
TDI	LVTTTL	I	N/A	JTAG data input
TDO	LVTTTL	O, TRI	N/A	JTAG data output
TCK	LVTTTL	I	N/A	JTAG clock input
TMS	LVTTTL	I	1	JTAG test mode select, 0 = normal mode, 1 = test mode.
TRSTN	LVTTTL	I	0	JTAG reset pin, 0 = reset, 1 = not reset.
TEST_EN	LVTTTL	I	N/A	Pull-down to ground (VSS) with a 1.2k Ohm resistor.
RESETN	LVTTTL	I	1	Chip reset pin, 0 = reset, 1 = not reset.

Table 23 Pin Definitions (Continued)

Name	Type	I/O	Default Value	Description
<b>Power and Ground Pins</b>				
AVDDR <sub>X</sub>	PWR	I	N/A	Analog receive power (1.8 V).
AVDDT <sub>X</sub>	PWR	I	N/A	Analog transmit power (1.8 V).
AVSS	GND	I	N/A	Analog ground.
VDD	PWR	I	N/A	Core power supply (1.8 V).
VDD3	PWR	I	N/A	LVTTL power supply (3.3 V).
VDDQ <sub>R</sub>	PWR	I	N/A	PLVDS receive power supply (1.8 V).
VDDQ <sub>T</sub>	PWR	I	N/A	PLVDS transmit power supply (1.8 V).
VSS	GND	I	N/A	Core ground.
VTR <sub>X</sub>	PWR	I	N/A	SLVDS/CML receive termination voltage (1.8 or 1.5 V).
VTT <sub>X</sub>	PWR	I	N/A	SLVDS/CML transmit termination voltage (1.8 or 1.5 V).
<b>Reserved Pins</b>				
RES0	LVTTL	I	N/A	Pull-down to ground (VSS) with a 1.2k Ohm resistor.
RES1	LVTTL	I	N/A	Pull-down to ground (VSS) with a 1.2k Ohm resistor.
DELAY_IN	LVTTL	I	N/A	Reserved.
DELAY_OUT	LVTTL	O	N/A	Reserved.
THERMAL_IN		I	N/A	Reserved.
THERMAL_OUT		O	N/A	Reserved.
FRAME_SYNC	LVTTL	I	0	Pull-down to ground (VSS) with a 1.2k Ohm resistor.

## 18 Electrical Specifications

This sections provides electrical specification information for the M27218 transceiver and consists of the following sections.

- Section 18.1, "Absolute Maximum Ratings"
- Section 18.2, "Recommended Operating Conditions"
- Section 18.3, "Reference Clock Requirements (REFCLKN/REFCLKP)"
- Section 18.4, "LVTTL Electrical Characteristics"
- Section 18.5, "SLVDS/CML Interface AC Characteristics"
- Section 18.6, "PLVDS Interface AC Characteristics"

### 18.1 Absolute Maximum Ratings

Table 24 contains stress ratings for the M27218 transceiver. Functional operation outside the absolute maximum and minimum ratings is neither implied nor guaranteed. The M27218 operating conditions are given in the AC and DC tables. Extended exposure to the maximum ratings can affect device reliability. Note that although the M27218 transceiver contains protective circuitry to resist damage from static discharge, exposure to high static voltages or electric fields must be avoided.

**Table 24 M27218 Absolute Maximum Ratings**

Parameter	Min.	Max.	Unit
Supply voltage (VDD)	1.7	1.89	V
Input voltage (LVTTL)	3.0	3.6	V
Differential input voltage (SLVDS/CML)	100		mV
Differential input voltage (PLVDS)	100		mV
Output LVTTL current		100	mA
Output SLVDS/CML current		36	mA
Output PLVDS current - drivers short together		12	mA
Output PLVDS current - drivers short to GND		40	mA
Storage temperature	-65	+150	°C
Relative humidity (Storage)	0	95	%
Relative humidity (Operating)	8	80	%
Maximum input ESD (HBM)	—	1500	V

### 18.2 Recommended Operating Conditions

Table 25 contains the recommended operating conditions for the M27218 transceiver.

**Table 25 M27218 Recommended Operating Conditions**

Parameter/Symbol	Condition	Min.	Typ.	Max.	Unit
Core supply voltage (VDD)		1.71	1.8	1.89	V
Analog supply voltage (VDDA)	SLVDS/CML	1.71	1.8	1.89	V
	PLVDS	1.71	1.8	1.89	V
	LVTTTL	3.14	3.3	3.47	V
Core supply current (IDD)	All I/O power-down		420	550	mA
Analog supply current (IDDA)	SLVDS/CML		130	150	mA
	PLVDS		500	650	mA
Power Consumption	4:1 mode @ 2.5 Gbps		3.3		W
Ambient Temperature	-22 with heatsink	-40		+85	°C

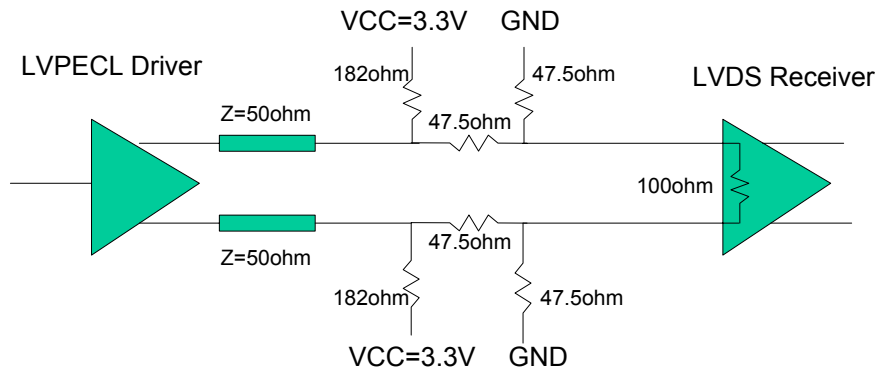
### 18.3 Reference Clock Requirements (REFCLKN/REFCLKP)

Table 26 contains the REFCLK reference clock (LVDS) requirements for the M27218 transceiver.

**Table 26 M27218 REFCLK Specifications**

Parameter/Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency	Must match the PLVDS data rate		622		MHz
Duty cycle		45	50	55	%
Jitter	BW = 10 Hz to 20 MHz		15		ps (RMS)
	BW = 12 KHz to 80 MHz		1		ps (RMS)
Differential input voltage	peak-to-peak	100			mV

It is recommended to use the 3.3V Voltage Controlled Crystal Oscillator (VCXO) from Connor Winfield ([www.conwin.com](http://www.conwin.com), VPLB54TE). The recommended VCXO has PECL differential outputs and a conversion circuit (PECL to LVDS) is required. Single chips that perform the function below are also available.



## 18.4 LVTTL Electrical Characteristics

Table 27 contains the LVTTL electrical characteristics for the M27218 transceiver.

**Table 27 M27218 LVTTL Interface AC Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input low voltage	VIL	0		0.8	V
Input high voltage	VIH	2.0			V
Output high voltage	VOH	2.40			V
Output low voltage	VOL			0.4	V
Output high current	IOH	-16			mA
Output low current	IOL	16			mA

## 18.5 SLVDS/CML Interface AC Characteristics

Table 28 contains the SLVDS serial interface AC characteristics for the M27218 transceiver.

**Table 28 M27218 SLVDS/CML Interface AC Characteristics**

Parameter/Symbol	Condition	Min.	Typ.	Max.	Unit
Differential output voltage (p-p)	Reg=00		300		mV
	Reg=01		500		mV
	Reg=10		650		mV
	Reg=11		800		mV
Output High Voltage	Reg = 00 $V_T = 1.8$	$V_{DD} - 0.018$		$V_{DD} - 0.005$	mV
	Reg = 01 $V_T = 1.8$	$V_{DD} - 0.01$		$V_{DD}$	mV
	Reg = 10 $V_T = 1.8$	$V_{DD} - 0.015$		$V_{DD}$	mV
	Reg = 11 $V_T = 1.8$	$V_{DD} - 0.005$		$V_{DD}$	mV
Output Low Voltage	Reg = 00 $V_T = 1.8$	$V_{DD} - 0.37$		$V_{DD} - 0.37$	mV
	Reg = 01 $V_T = 1.8$	$V_{DD} - 0.58$		$V_{DD} - 0.57$	mV
	Reg = 10 $V_T = 1.8$	$V_{DD} - 0.7$		$V_{DD} - 0.65$	mV
	Reg = 11 $V_T = 1.8$	$V_{DD} - 0.96$		$V_{DD} - 0.91$	mV
Differential input voltage (peak-to-peak)	with equalization off-set OFF	200			mV
Input voltage range	$V_{DD} = 1.8V$	0.7		1.7	V
Output common mode voltage (Offset output voltage)	$V_T = 1.8 V$		1.63		V
Output current	Drivers short to GND $V_T = 1.8 V$			36	mA
Differential output impedance		80	100	120	Ohms
Differential input impedance		80	100	120	Ohms
Jitter Generation	with $2^7$ PRBS		0.16		UI
Jitter Tolerance	@6 MHz Modulation		0.32	0.45	UI
Rise time (20% to 80%)			145	185	ps
Fall time (20% to 80%)			145	185	ps

**Table 28 M27218 SLVDS/CML Interface AC Characteristics (Continued)**

<b>Parameter/Symbol</b>	<b>Condition</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Unit</b>
Serial SLVDS to Parallel PLVDS Latency	With Alignment 622 MHz REFCLK	47	51	55	ns
Serial SLVDS to Parallel PLVDS Latency	Without Alignment 622 MHz REFCLK	37	41	45	ns

## 18.6 PLVDS Interface AC Characteristics

The M27218 PLVDS interface is compliant with IEEE LVDS General Purpose Link (IEEE Std. 1596.3-1996)

Table 29 contains the PLVDS serial interface AC characteristics for the M27218 transceiver.

**Table 29 M27218 PLVDS Interface AC Characteristics**

Parameter/Symbol	Condition	Min.	Typ.	Max.	Unit
Differential output voltage (p-p)			600		mV
Output high voltage				1.6	V
Output low voltage		0.925			V
Differential input voltage (Input sensitivity)		140			mV
Input voltage range		0		1.8	V
Output common mode voltage (Offset output voltage)	VDDQT, VDDQR = 1.8V	1.125	1.2	1.275	V
Output current	Drivers short together			12	mA
	Drivers short to GND			40	mA
Differential output impedance		80	100	120	Ohms
Differential input impedance		80	100	120	Ohms
Jitter Generation	with 2 <sup>7</sup> PRBS		0.07		UI
Rise time (20% to 80%)			120		ps
Fall time (80% to 20%)			120		ps
Parallel PLVDS to Serial SLVDS Latency	With Alignment 622 MHz REFCLK	59	61	63	ns
Parallel PLVDS to Serial SLVDS Latency	Without Alignment 622 MHz REFCLK	27	29	31	ns

# 19 Mechanical Specifications

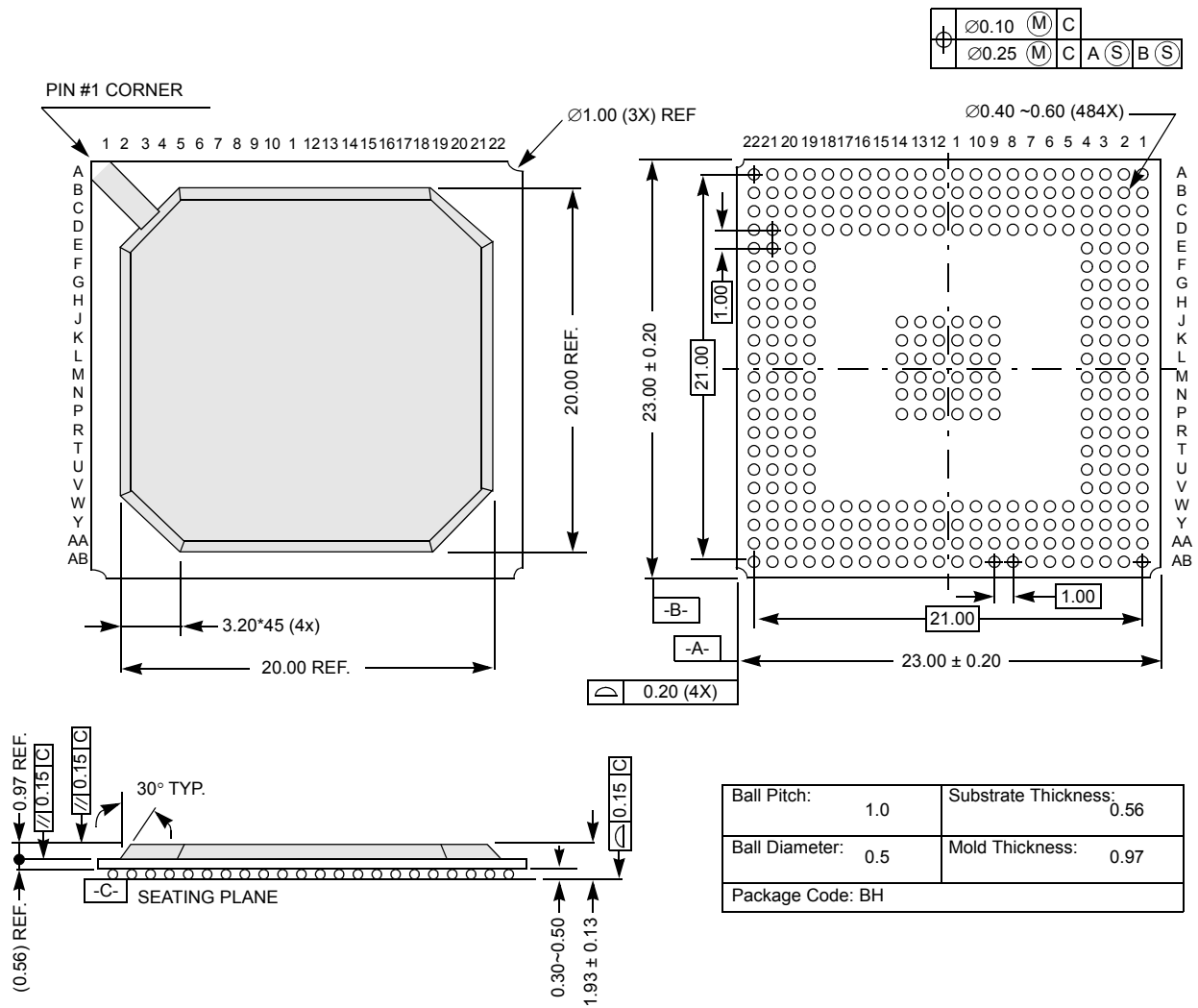


Figure 27 M27218 Mechanical Specifications

## 20 Thermal Guidelines

$T_{j_{max}} = 125 \text{ }^{\circ}\text{C}$  (Maximum junction temperature of the device)

$\theta_{jc} = 7.4 \text{ }^{\circ}\text{C/W}$  (Junction to case - defined by package and device. It does not change with airflow or heat-sink)

$\theta_{ja} = 19.4 \text{ }^{\circ}\text{C/W @ 0m/s}$  (Junction to ambient - defined by application environment, e.g.,  $T_a = +85 \text{ }^{\circ}\text{C}$ )

$\theta_{ja} = 17.5 \text{ }^{\circ}\text{C/W @ 1m/s}$  (Junction to ambient - defined by application environment, e.g.,  $T_a = +85 \text{ }^{\circ}\text{C}$ )

$\theta_{ja} = 15.8 \text{ }^{\circ}\text{C/W @ 2m/s}$  (Junction to ambient - defined by application environment, e.g.,  $T_a = +85 \text{ }^{\circ}\text{C}$ )

$P = 3.3\text{W}$  (Power dissipation)

There are two ways to calculate the maximum junction temperature of the device

(1)

$$T_{j_{max}} = T_c + \theta_{jc} * P$$

where  $T_c$  (Case temperature) and  $P$  (Power dissipation)

$$T_{j_{max}} = 85 + 7.4 * 3.3 = 104 \text{ }^{\circ}\text{C} < 125 \text{ }^{\circ}\text{C} \text{ (meets requirement)}$$

(2)

$$T_{j_{max}} = T_a + \theta_{ja} * P$$

where  $T_a$  (Ambient temperature) and  $P$  (Power dissipation)

$$T_{j_{max}} = 85 + 15.8 * 3.3 = 126 \text{ }^{\circ}\text{C} > 125 \text{ }^{\circ}\text{C} \text{ (marginal, does NOT meet the requirement)}$$

(to meet this requirement, either  $\theta_{ja}$  has to be reduced by using heat-sink or the  $T_a$  must be reduced)

Therefore, the maximum allowable ambient temperature without heat-sink is

$$T_{a_{max}} = 125 - 15.8 * 3.3 = 84 \text{ }^{\circ}\text{C} \text{ (without heat-sink)}$$

Recommended Heat-Sink Vendors:

Wakefield ([www.wakefield.com](http://www.wakefield.com))

Aavid ([www.aavid.com](http://www.aavid.com))

Advanced thermal solutions ( [www.qats.com](http://www.qats.com))

## 21 Package Pinouts

### 21.1 Numerical Pin Listing

Table 30 lists the M27218 pins in numerical order.

**Table 30 M27218 Numerical Pin Listing**

Ball #	Name	Type	Ball #	Name	Type	Ball #	Name	Type
A1	VSS	GND	B12	OUT_CLK4N	LVDS	D1	TMS	LVTTL
A2	TRSTN	LVTTL	B13	PDO4[3]N	LVDS	D2	VSS	GND
A3	OUT_CLK7P	LVDS	B14	PDO4[1]N	LVDS	D3	VDD	PWR
A4	PDO7[3]P	LVDS	B15	OUT_CLK3N	LVDS	D4	PDO7[2]N	LVDS
A5	PDO7[1]P	LVDS	B16	PDO3[3]N	LVDS	D5	PDO7[0]N	LVDS
A6	OUT_CLK6P	LVDS	B17	PDO3[1]N	LVDS	D6	VDDQ	PWR
A7	PDO6[3]P	LVDS	B18	OUT_CLK2N	LVDS	D7	PDO6[2]N	LVDS
A8	PDO6[1]P	LVDS	B19	PDO2[3]N	LVDS	D8	PDO6[0]N	LVDS
A9	OUT_CLK5P	LVDS	B20	PDO2[2]N	LVDS	D9	VDDQ	PWR
A10	PDO5[3]P	LVDS	B21	PDO2[0]N	LVDS	D10	PDO5[2]N	LVDS
A11	PDO5[1]P	LVDS	B22	PDO2[0]P	LVDS	D11	PDO[0]N	LVDS
A12	OUT_CLK4P	LVDS	C1	TCK	LVTTL	D12	VDDQ	PWR
A13	PDO4[3]P	LVDS	C2	VDD3	PWR	D13	PDO4[2]N	LVDS
A14	PDO4[1]P	LVDS	C3	RESETN	LVTTL	D14	PDO4[0]N	LVDS
A15	OUT_CLK3P	LVDS	C4	PDO7[2]P	LVDS	D15	VDDQ	PWR
A16	PDO3[3]P	LVDS	C5	PDO7[0]P	LVDS	D16	PDO3[2]N	LVDS
A17	PDO3[1]P	LVDS	C6	VSS	GND	D17	PDO3[0]N	LVDS
A18	OUT_CLK2P	LVDS	C7	PDO6[2]P	LVDS	D18	VDDQ	PWR
A19	PDO2[3]P	LVDS	C8	PDO6[0]P	LVDS	D19	PDO1[2]N	LVDS
A20	PDO2[2]P	LVDS	C9	VSS	GND	D20	PDO1[2]P	LVDS
A21	PDO2[1]N	LVDS	C10	PDO5[2]P	LVDS	D21	PDO1[3]N	LVDS
A22	PDO2[1]P	LVDS	C11	PDO5[0]P	LVDS	D22	PDO1[3]P	LVDS
B1	TDO	LVTTL	C12	VSS	GND	E1	SDI[7]P	LVDS
B2	TDI	LVTTL	C13	PDO4[2]P	LVDS	E2	SDI[7]N	LVDS
B3	OUT_CLK7N	LVDS	C14	PDO4[0]P	LVDS	E3	AVSS	GND
B4	PDO7[3]N	LVDS	C15	VSS	GND	E4	AVDD	PWR
B5	PDO7[1]N	LVDS	C16	PDO3[2]P	LVDS	E19	PDO1[0]N	LVDS
B6	OUT_CLK6N	LVDS	C17	PDO3[0]P	LVDS	E20	PDO1[0]P	LVDS
B7	PDO6[3]N	LVDS	C18	VSS	GND	E21	PDO1[1]N	LVDS
B8	PDO6[1]N	LVDS	C19	VDDQ	PWR	E22	PDO1[1]P	LVDS
B9	OUT_CLK5N	LVDS	C20	VSS	GND	F1	SDI[6]P	LVDS
B10	PDO5[3]N	LVDS	C21	OUT_CLK1N	LVDS	F2	SDI[6]N	LVDS
B11	PDO5[1]N	LVDS	C22	OUT_CLK1P	LVDS	F3	AVSS	GND

Table 30 M27218 Numerical Pin Listing (Continued)

Ball #	Name	Type	Ball #	Name	Type	Ball #	Name	Type
F4	SVRTX		K4	SVTRX		M22	VSS	GND
F19	VDDQ	PWR	K9	VSS	GND	N1	AVSS	GND
F20	VSS	GND	K10	VSS	GND	N2	AVSS	GND
F21	OUT_CLK0N	LVDS	K11	VSS	GND	N3	AVSS	GND
F22	OUT_CLK0P	LVDS	K12	VSS	GND	N4	AVSS	GND
G1	SDI[5]P	LVDS	K13	VSS	GND	N9	VSS	GND
G2	SDI[5]N	LVDS	K14	VSS	GND	N10	VSS	GND
G3	AVSS	GND	K19	PDI7[0]N	LVDS	N11	VSS	GND
G4	AVDD	PWR	K20	PDI7[0]P	LVDS	N12	VSS	GND
G19	PDO0[2]N	LVDS	K21	PDI7[1]N	LVDS	N13	VSS	GND
G20	PDO0[2]P	LVDS	K22	PDI7[1]P	LVDS	N14	VSS	GND
G21	PDO0[3]N	LVDS	L1	SDI[1]P	LVDS	N19	PDI6[0]N	LVDS
G22	PDO0[3]P	LVDS	L2	SDI[1]N	LVDS	N20	PDI6[0]P	LVDS
H1	SDI[4]P	LVDS	L3	AVSS	GND	N21	PDI6[1]N	LVDS
H2	SDI[4]N	LVDS	L4	AVDD	PWR	N22	PDI6[1]P	LVDS
H3	AVSS	GND	L9	VSS	GND	P1	SDO[7]P	LVDS
H4	SVTRX		L10	VSS	GND	P2	SDO[7]N	LVDS
H19	PDO0[0]N	LVDS	L11	VSS	GND	P3	AVSS	GND
H20	PDO0[0]P	LVDS	L12	VSS	GND	P4	SVTTX	
H21	PDO0[1]N	LVDS	L13	VSS	GND	P9	VSS	GND
H22	PDO0[1]P	LVDS	L14	VSS	GND	P10	VSS	GND
J1	SDI[3]P	LVDS	L19	PDI7[2]N	LVDS	P11	VSS	GND
J2	SDI[3]N	LVDS	L20	PDI7[2]P	LVDS	P12	VSS	GND
J3	AVSS	GND	L21	PDI7[3]N	LVDS	P13	VSS	GND
J4	AVDD	PWR	L22	PDI7[3]P	LVDS	P14	VSS	GND
J9	VSS	GND	M1	SDI[0]P	LVDS	P19	PDI6[2]N	LVDS
J10	VSS	GND	M2	SDI[0]N	LVDS	P20	PDI6[2]P	LVDS
J11	VSS	GND	M3	AVSS	GND	P21	PDI6[3]N	LVDS
J12	VSS	GND	M4	SVTRX		P22	PDI6[3]P	LVDS
J13	VSS	GND	M9	VSS	GND	R1	SDO[6]P	LVDS
J14	VSS	GND	M10	VSS	GND	R2	SDO[6]N	LVDS
J19	VDD	PWR	M11	VSS	GND	R3	AVSS	GND
J20	VSS	GND	M12	VSS	GND	R4	AVDD	PWR
J21	VDDQ	PWR	M13	VSS	GND	R19	VDDQ	PWR
J22	VSS	GND	M14	VSS	GND	R20	VSS	GND
K1	SDI[2]P	LVDS	M19	VDDQ	PWR	R21	IN_CLK1N	LVDS
K2	SDI[2]N	LVDS	M20	VSS	GND	R22	IN_CLK1P	LVDS
K3	AVSS	GND	M21	VDDQ	PWR	T1	SDO[5]P	LVDS

## 21 Package Pinouts

**Table 30 M27218 Numerical Pin Listing (Continued)**

Ball #	Name	Type	Ball #	Name	Type	Ball #	Name	Type
T2	SDO[5]N	LVDS	W15	PDI3[2]N	LVDS	AA8	VDDQ	PWR
T3	AVSS	GND	W16	PDI3[0]N	LVDS	AA9	PDI1[3]N	LVDS
T4	SVTTX		W17	TEST_EN	LVTTTL	AA10	PDI1[1]N	LVDS
T19	PDI5[0]N	LVDS	W18	VDD	PWR	AA11	IN_CLK0N	LVDS
T20	PDI5[0]P	LVDS	W19	PDI4[0]N	LVDS	AA12	PDI2[3]N	LVDS
T21	PDI5[1]N	LVDS	W20	PDI4[0]P	LVDS	AA13	PDI2[1]N	LVDS
T22	PDI5[1]P	LVDS	W21	PDI4[1]N	LVDS	AA14	VDDQ	PWR
U1	SDO[4]P	LVDS	W22	PDI4[1]P	LVDS	AA15	PDI3[3]N	LVDS
U2	SDO[4]N	LVDS	Y1	SDO[1]P	LVDS	AA16	PDI3[1]N	LVDS
U3	AVSS	GND	Y2	SDO[1]N	LVDS	AA17	VDD3	PWR
U4	AVDD	PWR	Y3	AVSS	GND	AA18	DELAY_OUT	LVTTTL
U19	PDI5[2]N	LVDS	Y4	SVTTX		AA19	SPI_CS	LVTTTL
U20	PDI5[2]P	LVDS	Y5	VSS	GND	AA20	SPI_TX	LVTTTL
U21	PDI5[3]N	LVDS	Y6	PDI0[2]P	LVDS	AA21	THERMAL_OUT	
U22	PDI5[3]P	LVDS	Y7	PDI0[0]P	LVDS	AA22	RES0	LVTTTL
V1	SDO[3]P	LVDS	Y8	VSS	GND	AB1	AVSS	GND
V2	SDP[3]N	LVDS	Y9	PDI1[2]P	LVDS	AB2	AVSS	GND
V3	AVSS	GND	Y10	PDI1[0]P	LVDS	AB3	REFCLKN	LVDS
V4	SVTTX		Y11	VSS	GND	AB4	REFCLKP	LVDS
V19	VDDQ	PWR	Y12	PDI2[2]P	LVDS	AB5	VSS	GND
V20	VSS	GND	Y13	PDI2[0]P	LVDS	AB6	PDI0[3]P	LVDS
V21	VDDQ	PWR	Y14	VSS	GND	AB7	PDI0[1]P	LVDS
V22	VSS	GND	Y15	PDI3[2]P	LVDS	AB8	VSS	GND
W1	SDO[2]P	LVDS	Y16	PDI3[0]P	LVDS	AB9	PDI1[3]P	LVDS
W2	SDO[2]N	LVDS	Y17	DELAY_IN	LVTTTL	AB10	PDI1[1]P	LVDS
W3	AVSS	GND	Y18	VSS	GND	AB11	IN_CLK0P	LVDS
W4	AVDD	PWR	Y19	PDI4[2]N	LVDS	AB12	PDI2[3]P	LVDS
W5	VDD	PWR	Y20	PDI4[2]P	LVDS	AB13	PDI2[1]P	LVDS
W6	PDI0[2]N	LVDS	Y21	PDI4[3]N	LVDS	AB14	VSS	GND
W7	PDI0[0]N	LVDS	Y22	PDI4[3]P	LVDS	AB15	PDI3[3]P	LVDS
W8	VDDQ	PWR	AA1	SDO[0]P	LVDS	AB16	PDI3[1]P	LVDS
W9	PDI1[2]N	LVDS	AA2	SDO[0]N	LVDS	AB17	VSS	GND
W10	PDI1[0]N	LVDS	AA3	AVSS	GND	AB18	FRAME_SYNC	LVTTTL
W11	VDDQ	PWR	AA4	AVDD	PWR	AB19	SPI_CLK	LVTTTL
W12	PDI2[2]N	LVDS	AA5	VDDQ	PWR	AB20	SPI_RX	LVTTTL
W13	PDI2[0]N	LVDS	AA6	PDI0[3]N	LVDS	AB21	THERMAL_IN	
W14	VDDQ	PWR	AA7	PDI0[1]N	LVDS	AB22	RES1	LVTTTL

## 21.2 Alphabetical Pin Listing

Table 31 lists the pins in alphabetical order.

**Table 31 M27218 Alphabetical Pin Listing**

Ball #	Name	Type	Ball #	Name	Type	Ball #	Name	Type
E4	AVDDR_X	PWR	R21	IN_CLK1N	LVDS	W13	PDI2[0]N	LVDS
G4	AVDDR_X	PWR	R22	IN_CLK1P	LVDS	Y13	PDI2[0]P	LVDS
J4	AVDDR_X	PWR	F21	OUT_CLK0N	LVDS	AA13	PDI2[1]N	LVDS
L4	AVDDR_X	PWR	F22	OUT_CLK0P	LVDS	AB13	PDI2[1]P	LVDS
R4	AVDDTX	PWR	C21	OUT_CLK1N	LVDS	W12	PDI2[2]N	LVDS
U4	AVDDTX	PWR	C22	OUT_CLK1P	LVDS	Y12	PDI2[2]P	LVDS
W4	AVDDTX	PWR	B18	OUT_CLK2N	LVDS	AA12	PDI2[3]N	LVDS
AA4	AVDDTX	PWR	A18	OUT_CLK2P	LVDS	AB12	PDI2[3]P	LVDS
E3	AVSS	GND	B15	OUT_CLK3N	LVDS	W16	PDI3[0]N	LVDS
F3	AVSS	GND	A15	OUT_CLK3P	LVDS	Y16	PDI3[0]P	LVDS
G3	AVSS	GND	B12	OUT_CLK4N	LVDS	AA16	PDI3[1]N	LVDS
H3	AVSS	GND	A12	OUT_CLK4P	LVDS	AB16	PDI3[1]P	LVDS
J3	AVSS	GND	B9	OUT_CLK5N	LVDS	W15	PDI3[2]N	LVDS
K3	AVSS	GND	A9	OUT_CLK5P	LVDS	Y15	PDI3[2]P	LVDS
L3	AVSS	GND	B6	OUT_CLK6N	LVDS	AA15	PDI3[3]N	LVDS
M3	AVSS	GND	A6	OUT_CLK6P	LVDS	AB15	PDI3[3]P	LVDS
N1	AVSS	GND	B3	OUT_CLK7N	LVDS	W19	PDI4[0]N	LVDS
N2	AVSS	GND	A3	OUT_CLK7P	LVDS	W20	PDI4[0]P	LVDS
N3	AVSS	GND	W7	PDI0[0]N	LVDS	W21	PDI4[1]N	LVDS
N4	AVSS	GND	Y7	PDI0[0]P	LVDS	W22	PDI4[1]P	LVDS
P3	AVSS	GND	AA7	PDI0[1]N	LVDS	Y19	PDI4[2]N	LVDS
R3	AVSS	GND	AB7	PDI0[1]P	LVDS	Y20	PDI4[2]P	LVDS
T3	AVSS	GND	W6	PDI0[2]N	LVDS	Y21	PDI4[3]N	LVDS
U3	AVSS	GND	Y6	PDI0[2]P	LVDS	Y22	PDI4[3]P	LVDS
V3	AVSS	GND	AA6	PDI0[3]N	LVDS	T19	PDI5[0]N	LVDS
W3	AVSS	GND	AB6	PDI0[3]P	LVDS	T20	PDI5[0]P	LVDS
Y3	AVSS	GND	W10	PDI1[0]N	LVDS	T21	PDI5[1]N	LVDS
AA3	AVSS	GND	Y10	PDI1[0]P	LVDS	T22	PDI5[1]P	LVDS
AB1	AVSS	GND	AA10	PDI1[1]N	LVDS	U19	PDI5[2]N	LVDS
Y17	DELAY_IN	LVTTL	AB10	PDI1[1]P	LVDS	U20	PDI5[2]P	LVDS
AA18	DELAY_OUT	LVTTL	W9	PDI1[2]N	LVDS	U21	PDI5[3]N	LVDS
AB18	FRAME_SYNC	LVTTL	Y9	PDI1[2]P	LVDS	U22	PDI5[3]P	LVDS
AA11	IN_CLK0N	LVDS	AA9	PDI1[3]N	LVDS	N19	PDI6[0]N	LVDS
AB11	IN_CLK0P	LVDS	AB9	PDI1[3]P	LVDS	N20	PDI6[0]P	LVDS

Table 31 M27218 Alphabetical Pin Listing (Continued)

Ball #	Name	Type	Ball #	Name	Type	Ball #	Name	Type
N21	PDI6[1]N	LVDS	A19	PDO2[3]P	LVDS	D4	PDO7[2]N	LVDS
N22	PDI6[1]P	LVDS	D17	PDO3[0]N	LVDS	C4	PDO7[2]P	LVDS
P19	PDI6[2]N	LVDS	C17	PDO3[0]P	LVDS	B4	PDO7[3]N	LVDS
P20	PDI6[2]P	LVDS	B17	PDO3[1]N	LVDS	A4	PDO7[3]P	LVDS
P21	PDI6[3]N	LVDS	A17	PDO3[1]P	LVDS	AB5	VSS	GND
P22	PDI6[3]P	LVDS	D16	PDO3[2]N	LVDS	AB2	AVSS	GND
K19	PDI7[0]N	LVDS	C16	PDO3[2]P	LVDS	AB3	REFCLKN	LVDS
K20	PDI7[0]P	LVDS	B16	PDO3[3]N	LVDS	AB4	REFCLKP	LVDS
K21	PDI7[1]N	LVDS	A16	PDO3[3]P	LVDS	AA22	RES0	LVTTTL
K22	PDI7[1]P	LVDS	D14	PDO4[0]N	LVDS	AB22	RES1	LVTTTL
L19	PDI7[2]N	LVDS	C14	PDO4[0]P	LVDS	C3	RESETN	LVTTTL
L20	PDI7[2]P	LVDS	B14	PDO4[1]N	LVDS	M2	SDI_0N	LVDS
L21	PDI7[3]N	LVDS	A14	PDO4[1]P	LVDS	M1	SDI_0P	LVDS
L22	PDI7[3]P	LVDS	D13	PDO4[2]N	LVDS	L2	SDI_1N	LVDS
H19	PDO0[0]N	LVDS	C13	PDO4[2]P	LVDS	L1	SDI_1P	LVDS
H20	PDO0[0]P	LVDS	B13	PDO4[3]N	LVDS	K2	SDI_2N	LVDS
H21	PDO0[1]N	LVDS	A13	PDO4[3]P	LVDS	K1	SDI_2P	LVDS
H22	PDO0[1]P	LVDS	D11	PDO5[0]N	LVDS	J2	SDI_3N	LVDS
G19	PDO0[2]N	LVDS	C11	PDO5[0]P	LVDS	J1	SDI_3P	LVDS
G20	PDO0[2]P	LVDS	B11	PDO5[1]N	LVDS	H2	SDI_4N	LVDS
G21	PDO0[3]N	LVDS	A11	PDO5[1]P	LVDS	H1	SDI_4P	LVDS
G22	PDO0[3]P	LVDS	D10	PDO5[2]N	LVDS	G2	SDI_5N	LVDS
E19	PDO1[0]N	LVDS	C10	PDO5[2]P	LVDS	G1	SDI_5P	LVDS
E20	PDO1[0]P	LVDS	B10	PDO5[3]N	LVDS	F2	SDI_6N	LVDS
E21	PDO1[1]N	LVDS	A10	PDO5[3]P	LVDS	F1	SDI_6P	LVDS
E22	PDO1[1]P	LVDS	D8	PDO6[0]N	LVDS	E2	SDI_7N	LVDS
D19	PDO1[2]N	LVDS	C8	PDO6[0]P	LVDS	E1	SDI_7P	LVDS
D20	PDO1[2]P	LVDS	B8	PDO6[1]N	LVDS	AA2	SDO_0N	LVDS
D21	PDO1[3]N	LVDS	A8	PDO6[1]P	LVDS	AA1	SDO_0P	LVDS
D22	PDO1[3]P	LVDS	D7	PDO6[2]N	LVDS	Y2	SDO_1N	LVDS
B21	PDO2[0]N	LVDS	C7	PDO6[2]P	LVDS	Y1	SDO_1P	LVDS
B22	PDO2[0]P	LVDS	B7	PDO6[3]N	LVDS	W2	SDO_2N	LVDS
A21	PDO2[1]N	LVDS	A7	PDO6[3]P	LVDS	W1	SDO_2P	LVDS
A22	PDO2[1]P	LVDS	D5	PDO7[0]N	LVDS	V2	SDO_3N	LVDS
B20	PDO2[2]N	LVDS	C5	PDO7[0]P	LVDS	V1	SDO_3P	LVDS
A20	PDO2[2]P	LVDS	B5	PDO7[1]N	LVDS	U2	SDO_4N	LVDS
B19	PDO2[3]N	LVDS	A5	PDO7[1]P	LVDS	U1	SDO_4P	LVDS

Table 31 M27218 Alphabetical Pin Listing (Continued)

Ball #	Name	Type	Ball #	Name	Type	Ball #	Name	Type
T2	SDO_5N	LVDS	D18	VDDQT	PWR	L9	VSS	GND
T1	SDO_5P	LVDS	F19	VDDQT	PWR	L10	VSS	GND
R2	SDO_6N	LVDS	J21	VDDQT	PWR	L11	VSS	GND
R1	SDO_6P	LVDS	M19	VDDQR	PWR	L12	VSS	GND
P2	SDO_7N	LVDS	M21	VDDQR	PWR	L13	VSS	GND
P1	SDO_7P	LVDS	R19	VDDQR	PWR	L14	VSS	GND
AB19	SPI_CLK	LVTTTL	V19	VDDQR	PWR	M9	VSS	GND
AA19	SPI_CS	LVTTTL	V21	VDDQR	PWR	M10	VSS	GND
AB20	SPI_RX	LVTTTL	W8	VDDQR	PWR	M11	VSS	GND
AA20	SPI_TX	LVTTTL	W11	VDDQR	PWR	M12	VSS	GND
F4	VTRX	PWR	W14	VDDQR	PWR	M13	VSS	GND
H4	VTRX	PWR	AA5	VDDQR	PWR	M14	VSS	GND
K4	VTRX	PWR	AA8	VDDQR	PWR	M20	VSS	GND
M4	VTRX	PWR	AA14	VDDQR	PWR	M22	VSS	GND
P4	VTX	PWR	A1	VSS	GND	N9	VSS	GND
T4	VTX	PWR	C6	VSS	GND	N10	VSS	GND
V4	VTX	PWR	C9	VSS	GND	N11	VSS	GND
Y4	VTX	PWR	C12	VSS	GND	N12	VSS	GND
C1	TCK	LVTTTL	C15	VSS	GND	N13	VSS	GND
B2	TDI	LVTTTL	C18	VSS	GND	N14	VSS	GND
B1	TDO	LVTTTL	C20	VSS	GND	P9	VSS	GND
W17	TEST_EN	LVTTTL	D2	VSS	GND	P10	VSS	GND
AB21	THERMAL_IN		F20	VSS	GND	P11	VSS	GND
AA21	THERMAL_OUT		J9	VSS	GND	P12	VSS	GND
D1	TMS	LVTTTL	J10	VSS	GND	P13	VSS	GND
A2	TRSTN	LVTTTL	J11	VSS	GND	P14	VSS	GND
D3	VDD	PWR	J12	VSS	GND	R20	VSS	GND
J19	VDD	PWR	J13	VSS	GND	V20	VSS	GND
W5	VDD	PWR	J14	VSS	GND	V22	VSS	GND
W18	VDD	PWR	J20	VSS	GND	Y5	VSS	GND
C2	VDD3	PWR	J22	VSS	GND	Y8	VSS	GND
AA17	VDD3	PWR	K9	VSS	GND	Y11	VSS	GND
C19	VDDQT	PWR	K10	VSS	GND	Y14	VSS	GND
D6	VDDQT	PWR	K11	VSS	GND	Y18	VSS	GND
D9	VDDQT	PWR	K12	VSS	GND	AB8	VSS	GND
D12	VDDQT	PWR	K13	VSS	GND	AB14	VSS	GND
D15	VDDQT	PWR	K14	VSS	GND	AB17	VSS	GND

## 22 Glossary

The following is a glossary of acronyms and terms used in this document.

<b>Term</b>	<b>Description</b>
AC	Alternating Current
BIST	Built-In Self Test
CID	Contiguous Identical Digit
CDR	Clock and Data Recovery
CMOS	Complimentary Metal Oxide Semiconductor
FIFO	First In First Out
Gbps	Gigabits per Second
HSBGA	High-Speed Ball Grid Array
IEEE	Institute of Electrical and Electronics Engineers
ISI	Inter-Symbol Interference
JTAG	Joint Test Action Group
KHz	KiloHertz
LVDS	Low Voltage Differential Signaling
MHz	MegaHertz
PLVDS	Parallel Low Voltage Digital Signal
PRBS	Pseudo-Random Bit Sequence
SDH	Synchronous Digital Hierarchy
SerDes	Serializer/Deserializer
SLVDS	Serial Low Voltage Digital Signal
SONET	Synchronous Optical Network
SPI	Serial Peripheral Interface

## 23 Revision History

Date	Revision Number	Revision Content
March 28, 2002	Revision 1.0	Initial revision.
April 24, 2002	Revision 1.1	Author: Zhi Wong.
August 28, 2002	Revision 1.6	<p>Z. W.            Created Appendix B, which describes Thermal Diode (V, I, T) curve.            Created Appendix C, which describes the miscellaneous reserved pins.            Updated P2S and S2P latency data.            Added sentence in the OUT_CLK_x section to indicate that output clock is centered wrt data.            Added sentence in the PLVDS clock input section to indicate that there is no phase relationship required between the clock and data.            Enhanced the SLVDS to PLVDS bit alignment section.            Updated AC specifications.</p>
September 20, 2002	Revision 1.7	<p>Updated features list.            Added discussion about reference clock operation range (400 to 622 MHz).            Added sentence about maximum skew between PLVDS inputs.            Miscellaneous corrections per R.W. inputs.</p>
December 02, 2002	Revision 1.8	<p>Increased power dissipation numbers to 3.0W.            Changed input impedance from single-ended to differential.</p>
June, 2004	Revision 1.9	
September, 2004	Revision 2.0	<p>Added misc. details            Removed auto align, added manual align.</p>
May, 2006	Revision E	Updated for RoHS compliant packaging option.

### Appendix A JTAG Support

The M27218 processor implements JTAG boundary scan to facilitate board testing. The JTAG interface is fully compliant with the IEEE 1149.1 standard and supports the following mandatory boundary scan instructions:

- BYPASS
- EXTEST
- SAMPLE

In addition to the mandatory instructions, the M27218 also supports the following optional JTAG instructions:

- IDCODE
- CLAMP
- HIGHZ

After power is applied to the part, internal power-on-reset logic resets the JTAG function and the function remains reset until TMS is asserted and TCK is running.

The normal reset sequence, which involves the assertion of RESETN, does not initialize the JTAG function. This is in compliance with the IEEE 1149.1 standard which does not allow a device reset to initialize the JTAG logic.

#### A.1 Test Data Registers

The M27218 processor test logic contains three registers; Bypass, Boundary Scan, and Instruction.

##### A.1.1 Bypass Register

The bypass register is a one-bit shift register that provides a connection between the Test Data In (TDI) and Test Data Out (TDO) pins when no other test data registers are selected. The Bypass register allows for the rapid movement of test data to and from other board components without affecting the normal operation of these components. When using the Bypass register, data is transferred without inversion from TDI to TDO.

##### A.1.2 Boundary Scan Register

The Boundary Scan register is a single shift-register containing cells which connect to all of the input and output pins of the M27218. This register allows for the testing of board interconnections to detect defects such as opens circuits and short circuits. [Figure A-1](#) shows the logical structure of the Boundary Scan register.

Input cells only capture data and do not affect processor operation. Data is transferred without inversion from TDI to TDO through the Boundary Scan register during scanning. The Boundary Scan register is operated using the EXTEST and SAMPLE /PRELOAD instructions.

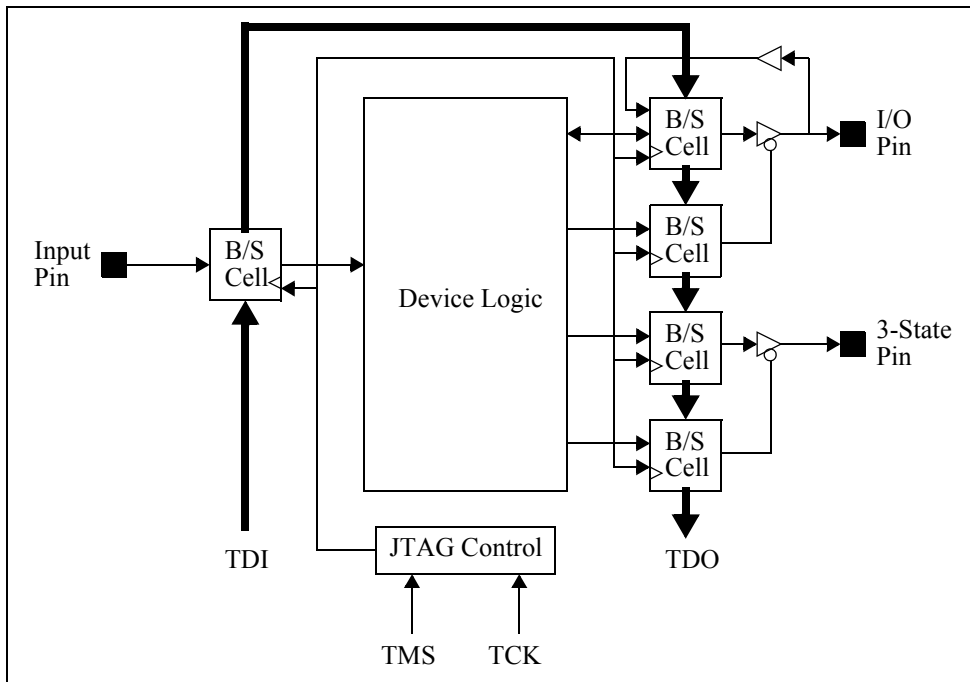


Figure A-1 JTAG Boundary Scan Cell Organization

### A.1.3 Instruction Register

The 4-bit wide Instruction register selects the boundary scan test to be performed and the test data register to be accessed. The execution of the boundary scan instructions is controlled by the Test Access Port (TAP) controller. Refer to [Section A.4](#) for more information on the TAP controller and its states.

[Table A-1](#) shows the encoding of the instructions supported by the M27218. All binary values not shown are reserved.

Table A-1 JTAG Instruction Register Encoding

Instruction Code	Instruction	Type
0000	EXTEST	Mandatory
0010	CLAMP	Optional
1011	SAMPLE	Mandatory
1101	IDCODE	Optional
1110	HIGHZ	Optional
1111	BYPASS	Mandatory

## A.2 Mandatory Boundary Scan Instructions

The M27218 supports three mandatory instructions; EXTEST, SAMPLE, and BYPASS. These instructions are encoded in the instruction register as shown in [Table A-1](#). The following subsections describe these instructions in more detail.

### A.2.1 EXTEST

The EXTEST instruction selects the boundary scan cells to be connected between TDI and TDO. Execution of the EXTEST instruction causes the output boundary scan cells to drive the output pins of the M27218. Values scanned into the register become the output values. The input boundary scan cells sample the input pins of the M27218. Bidirectional pins can be either inputs or outputs depending on their control setting.

- The EXTEST instruction uses the following TAP controller states. Refer to for more information on the TAP controller:
- The M27218 outputs the preloaded data to the pins at the falling edge of TCK in the *Update\_IR* TAP controller state. The JTAG instruction register is updated with the EXTEST instruction.
- The EXTEST instruction selects the cells to be tested in the *Shift\_DR* TAP controller state.
- Once the EXTEST instruction has been executed, the output pins can change state on the falling edge of TCK in the *Update\_DR* TAP controller state.

After execution of the EXTEST instruction, the M27218 must be reset.

### A.2.2 SAMPLE

The SAMPLE instruction is used to sample the state of the device pins. Execution of the SAMPLE instruction causes the output boundary scan cells to sample the value driven by the M27218. Input boundary scan cells sample their corresponding input pins on the rising edge of TCK. I/O pins can be driven by either the M27218 or external logic. The values shifted to the input latches are not used by internal logic.

The SAMPLE instruction uses the following TAP controller states:

- The SAMPLE instruction selects the cells to be tested in the *Shift\_DR* TAP controller state.
- The state of the pins to be tested are sampled on the rising edge of TCK in the *Capture\_DR* TAP controller state.
- The boundary scan cells are latched into the output latches on the falling edge of TCK in the *Update\_DR* TAP controller state.

This instruction can also be used to preload the boundary scan output cells with specific values. These preloaded values are then enabled to the output pins using the EXTEST instruction.

### A.2.3 BYPASS

The BYPASS instruction is used to bypass a component that is connected in series with other components. This allows for rapid movement of data through the various components on the board by bypassing those that do not need to be tested. The BYPASS instruction is forced onto the instruction register output latches during the *Test\_Logic\_Reset* state. When the BYPASS instruction is executed, test data is passed from TDI to TDO via the single-bit *Bypass* register, effectively bypassing the M27218.

This instruction can be entered by holding TDI at a HIGH logic level while completing an instruction scan cycle. This allows for easier access to a specific device on a multi-device board.

## A.3 Optional Boundary Scan Instructions

The M27218 supports three mandatory instructions; CLAMP, IDCODE, and HIGHZ. These instructions are encoded in the instruction register as shown in [Table A-1](#). The following subsections describe these instructions in more detail.

### A.3.1 CLAMP

The CLAMP instruction allows the state of the signals driven on the component pins to be determined from the boundary-scan register while the Bypass register is selected as the serial path between TDI and TDO.

The CLAMP instruction selects the Bypass register to be connected for serial access between TDI and TDO in the Shift\_DR TAP controller state. When the CLAMP instruction is selected, the state of all signals driven from the system output pins are defined by the data stored in the boundary-scan register.

### A.3.2 IDCODE

The IDCODE contains the Conexant vendor ID and part number. When this 32-bit register is read, it returns a value of 0x0000\_0013 to indicate the Mindspeed M27218 device.

### A.3.3 HIGHZ

The HIGHZ instruction place the M27218 device into a state in which all of the system logic outputs are placed into an inactive drive state. During the HIGHZ state, the test system may drive signals onto the connections normally driven by the M27218 output pins without risking damage to the device.

## A.4 TAP Controller

The Test Access Port (TAP) controller is a synchronous state machine that controls the test logic sequence of operations. The TAP controller changes state on the rising edge of TCK, and during power-up.

The value of the Test Mode Select (TMS) signal on the rising edge of TCK controls the state transitions of the TAP controller state machine. [Figure A-2](#) shows a diagram of the TAP controller state machine.

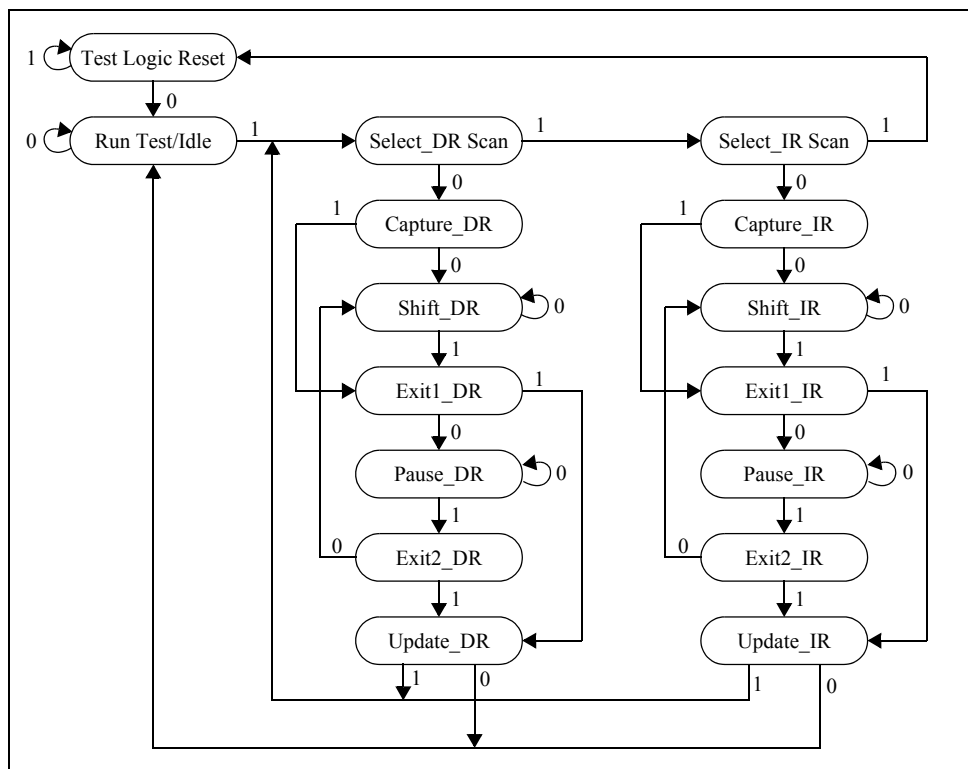


Figure A-2 TAP Controller State Diagram

#### A.4.1 Test-Logic-Reset State

In the *Test-Logic-Reset* state the boundary scan test logic is disabled, allowing normal operation of the M27218 to continue. The test logic enters the *Test-Logic-Reset* state when the TMS input is held HIGH for at least five rising edges of TCK. The BYPASS instruction is forced into the instruction register output latches during this state. The controller remains in the *Test-Logic-Reset* state as long as TMS is HIGH.

If the controller transitions from the *Test-Logic-Reset* state as a result of an erroneous low signal on TMS (for one rising edge of TCK), the controller returns to the *Test-Logic-Reset* state if TMS becomes HIGH for three rising edges of TCK. The operation of the test logic is such that, should the above condition occur, no disturbance is caused to the on-chip system logic. When the state machine transitions from the *Test-Logic-Reset* state to the *Run-Test/Idle* state, no action is taken because the current instruction has been set to select operation of the *Bypass* register. The test logic is also inactive in the *Select\_DR* and *Select\_IR* controller states.

#### A.4.2 Run-Test/Idle State

The controller enters the *Run-Test/Idle* state between scan operations. The controller remains in this state as long as TMS is held LOW. The instruction register and all test data registers retain their previous state. The instruction cannot change when the TAP controller is in this state.

When TMS is sampled HIGH at the rising edge of TCK, the controller transitions to the *Select\_DR* state.

#### A.4.3 Select\_DR\_Scan State

This is a temporary controller state in which all test data registers selected by the current instruction retain their previous state. If TMS is sampled LOW at the rising edge of TCK, the controller transitions to the *Capture\_DR* state. A HIGH on TMS causes the controller to transition to the *Select\_IR* state. The instruction cannot change while the TAP controller is in this state.

#### A.4.4 Select\_IR\_Scan State

This is a temporary controller state in which all test data registers selected by the current instruction retain their previous state. If TMS is sampled LOW at the rising edge of TCK, the controller transitions to the *Capture\_IR* state. A HIGH on TMS causes the controller to transition to the *Test-Reset-Logic* state. The instruction cannot change while the TAP controller is in this state.

#### A.4.5 Capture\_DR State

In this state the boundary scan register captures input pin data as the current instruction is either EXTEST or SAMPLE/PRELOAD. If TMS is sampled LOW at the rising edge of TCK, the controller transitions to the *Shift\_DR* state. A HIGH on TMS causes the controller to transition to the *Exit1\_DR* state. The instruction cannot change while the TAP controller is in this state.

#### A.4.6 Shift\_DR State

In this state the test data register connected between TDI and TDO as a result of the current instruction shifts data one stage toward its serial output on the rising edge of TCK. If TMS is sampled LOW at the rising edge of TCK, the controller remains in the *Shift\_DR* state. A HIGH on TMS causes the controller to transition to the *Exit1\_DR* state. The instruction cannot change while the TAP controller is in this state.

#### A.4.7 Exit1\_DR State

This is a temporary controller state in which all test data registers selected by the current instruction retain their previous state. If TMS is sampled LOW at the rising edge of TCK, the controller transitions to the *Pause\_DR* state. A HIGH on TMS causes the controller to transition to the *Update\_DR* state which terminates the scanning process. The instruction cannot change while the TAP controller is in this state.

#### A.4.8 Pause\_DR State

The *Pause\_DR* state allows the controller to temporarily halt the shifting of data through the test data register in the serial path between TDI and TDO. All test data registers selected by the current instruction retain their previous state. If TMS is sampled LOW at the rising edge of TCK, the controller remains in the *Pause\_DR* state. A HIGH on TMS causes the controller to transition to the *Exit2\_DR* state. The instruction cannot change while the TAP controller is in this state.

#### A.4.9 Exit2\_DR State

This is a temporary controller state in which all test data registers selected by the current instruction retain their previous state. If TMS is sampled LOW at the rising edge of TCK, the controller transitions to the *Shift\_DR* state to allow another serial shift of data. A HIGH on TMS causes the controller to transition to the *Update\_DR* state which terminates the scanning process. The instruction cannot change while the TAP controller is in this state.

### A.4.10 Update\_DR State

The boundary scan register includes a latched parallel output to prevent changes at the parallel output while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the boundary scan register is selected, data is latched into the parallel output of this register from the shift-register path on the falling edge of TCK. Data held at this latched parallel output only changes during this state.

If TMS is sampled LOW at the rising edge of TCK, the controller transitions to the *Run-Test/Idle* state. A HIGH on TMS causes the controller to transition to the *Select\_DR\_Scan* state. The instruction cannot change while the TAP controller is in this state and all shift register stages in the test data registers selected by the current instruction retain their previous state.

### A.4.11 Capture\_IR State

In this state the shift register contained in the instruction register loads a fixed pattern on the rising edge of TCK. The test data registers selected by the current instruction retain their previous state.

If TMS is sampled LOW at the rising edge of TCK, the controller transitions to the *Shift\_IR* state. A HIGH on TMS causes the controller to transition to the *Exit1\_IR* state. The instruction cannot change while the TAP controller is in this state.

### A.4.12 Shift\_IR State

In this state the test data register connected between TDI and TDO as a result of the current instruction shifts data one stage toward its serial output on the rising edge of TCK. If TMS is sampled LOW at the rising edge of TCK, the controller remains in the *Shift\_IR* state. A HIGH on TMS causes the controller to transition to the *Exit1\_IR* state. The instruction cannot change while the TAP controller is in this state.

### A.4.13 Exit1\_IR State

This is a temporary controller state in which all test data registers selected by the current instruction retain their previous state. If TMS is sampled LOW at the rising edge of TCK, the controller transitions to the *Pause\_IR* state. A HIGH on TMS causes the controller to transition to the *Update\_IR* state which terminates the scanning process. The instruction cannot change while the TAP controller is in this state and the instruction register retains its previous state.

### A.4.14 Pause\_IR State

The *Pause\_DR* state allows the controller to temporarily halt the shifting of data through the test data register in the serial path between TDI and TDO. All test data registers selected by the current instruction retain their previous state. If TMS is sampled LOW at the rising edge of TCK, the controller remains in the *Pause\_IR* state. A HIGH on TMS causes the controller to transition to the *Exit2\_IR* state. The instruction cannot change while the TAP controller is in this state.

### A.4.15 Exit2\_IR State

This is a temporary controller state in which all test data registers selected by the current instruction retain their previous state. If TMS is sampled LOW at the rising edge of TCK, the controller transitions to the *Shift\_IR* state to allow another serial shift of data. A HIGH on TMS causes the controller to transition to the *Update\_IR* state which terminates the scanning process. The instruction cannot change while the TAP controller is in this state.

#### A.4.16 Update\_IR State

The instruction shifted into the instruction register is latched onto the parallel output from the shift register path on the falling edge of TCK. Once the instruction has been latched it becomes the new instruction.

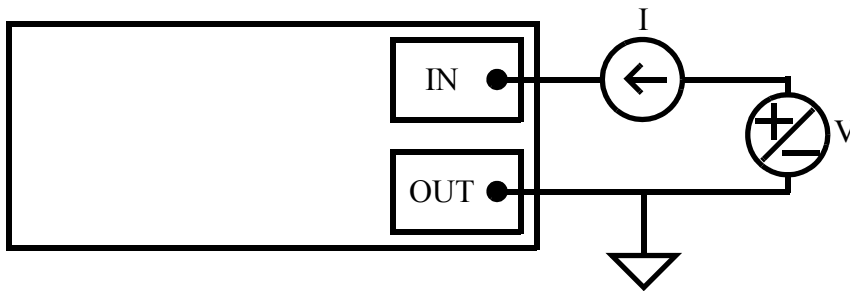
If TMS is sampled LOW at the rising edge of TCK, the controller transitions to the *Run-Test/Idle* state. A HIGH on TMS causes the controller to transition to the *Select\_IR\_Scan* state.

## Appendix B Thermal Diode (V, I, T) Curve Description

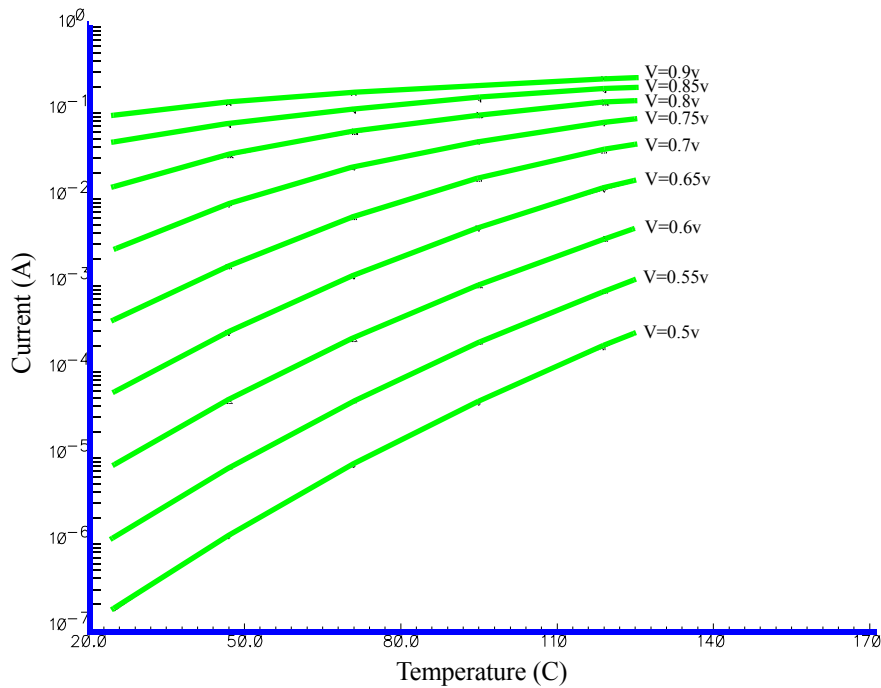
The M27218 provides two pins (THERMAL\_IN and THERMAL\_OUT) that allows the user to measure the device's internal temperature.

Refer to the diagram of electrical connections. Apply a voltage (V) from 0.5 V to 0.9 V with the positive terminal on pin THERMAL\_IN and the negative terminal on pin THERMAL\_OUT. Measure the current (I). Locate the measured current on the Y-axis (logarithmic scale) of the diode curves and find the intersection with the curve of the voltage applied. Read the temperature (T) from the X-axis.

### Electrical Connections



### Diode Curves



## Appendix C Miscellaneous Reserved Pins Description

### DELAY\_IN

Delay line test input pin. This pin is used together with pin DELAY\_OUT to test the delay in different process (fast, slow, typical). A pulse sent in from this pin should travel through a pure combinational logic come out from DELAY\_OUT pin with a delay of 24.43 ns (best case) and 54.68 (worst case) in fast and slow processes respectively.

### DELAY\_OUT

Delay line test output pin. See DELAY\_IN for more details.

### FRAME\_SYNC

Input Frame Synchronization signal from external device. When this signal has a value of “1” and when the “Frame\_Sync\_Reset\_EN” bit is set for its corresponding Bit Counter (18 bit wide, running at 622 MHz), the Bit Counter(s) will be reset to 0; when this signal has a value of “0” the Bit Counters will be free running and wrapping around back to 0 after they reach the value defined in Frame Counter reset control registers.