Signetics

FAST 74F455, 74F456
Buffers/Drivers

74F455 Octal Buffer/Driver With Parity, Inverting (3-State)
74F456 Octal Buffer/Driver With Parity, Non-Inverting (3-State)

Product Specification

FAST Products

FEATURES

- **High impedance NPN base inputs for reduced loading (40μA in High and Low states)**
- **'F455 combines 'F240 and 'F280A functions in one package**
- **'F456 combines 'F244 and 'F280A functions in one package**
- **'F455 and 'F456 are center pin versions of the 'F655A and 'F656A respectively**
- **'F455 Inverting**
  'F456 Non-Inverting
- **3-state outputs sink 64mA and source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Broadside pinout simplifies PC board layout**

DESCRIPTION

The 'F455 and 74F456 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F455	6.5ns	64mA
74F456	7.5ns	64mA

ORDERING INFORMATION

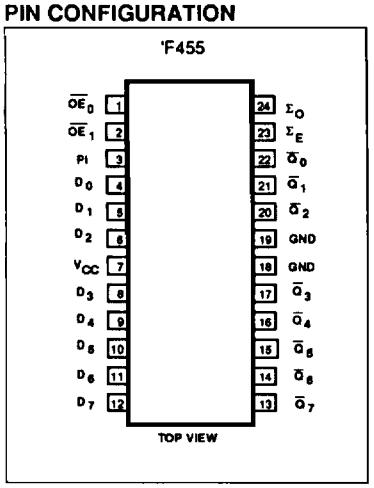
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F455N, N74F456N
24-Pin Plastic SOL	N74F455D, N74F456D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

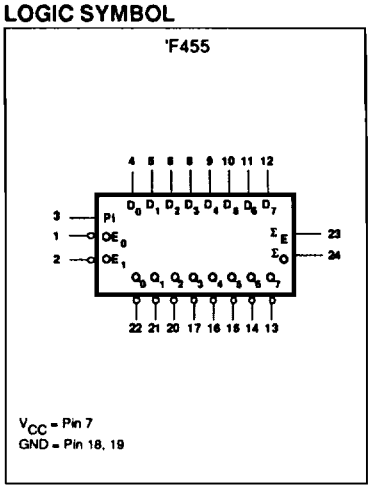
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_7	Data inputs	2.0/0.066	40μA/40μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA
$\overline{O}_0$- $\overline{O}_7$	Data outputs ('F455)	750/106.7	15mA/64mA
O_0- O_7	Data outputs ('F456)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

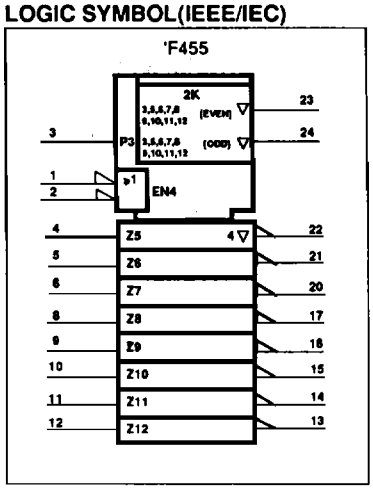
PIN CONFIGURATION



LOGIC SYMBOL

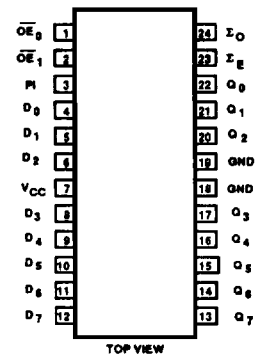


LOGIC SYMBOL(IEEE/IEC)



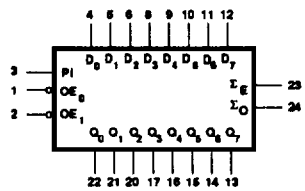
PIN CONFIGURATION

'F456



LOGIC SYMBOL

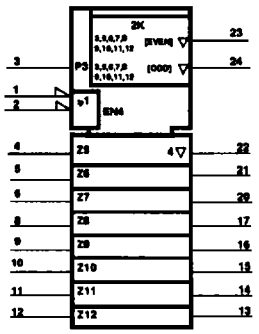
'F456



V_{CC} = Pin 7
GND = Pin 18, 19

LOGIC SYMBOL(IEEE/IEC)

'F456



FUNCTION TABLE

INPUTS			OUTPUTS	
			'F455	'F456
$\overline{OE}_0$	$\overline{OE}_1$	D_n	$\overline{O}_n$	Q_n
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

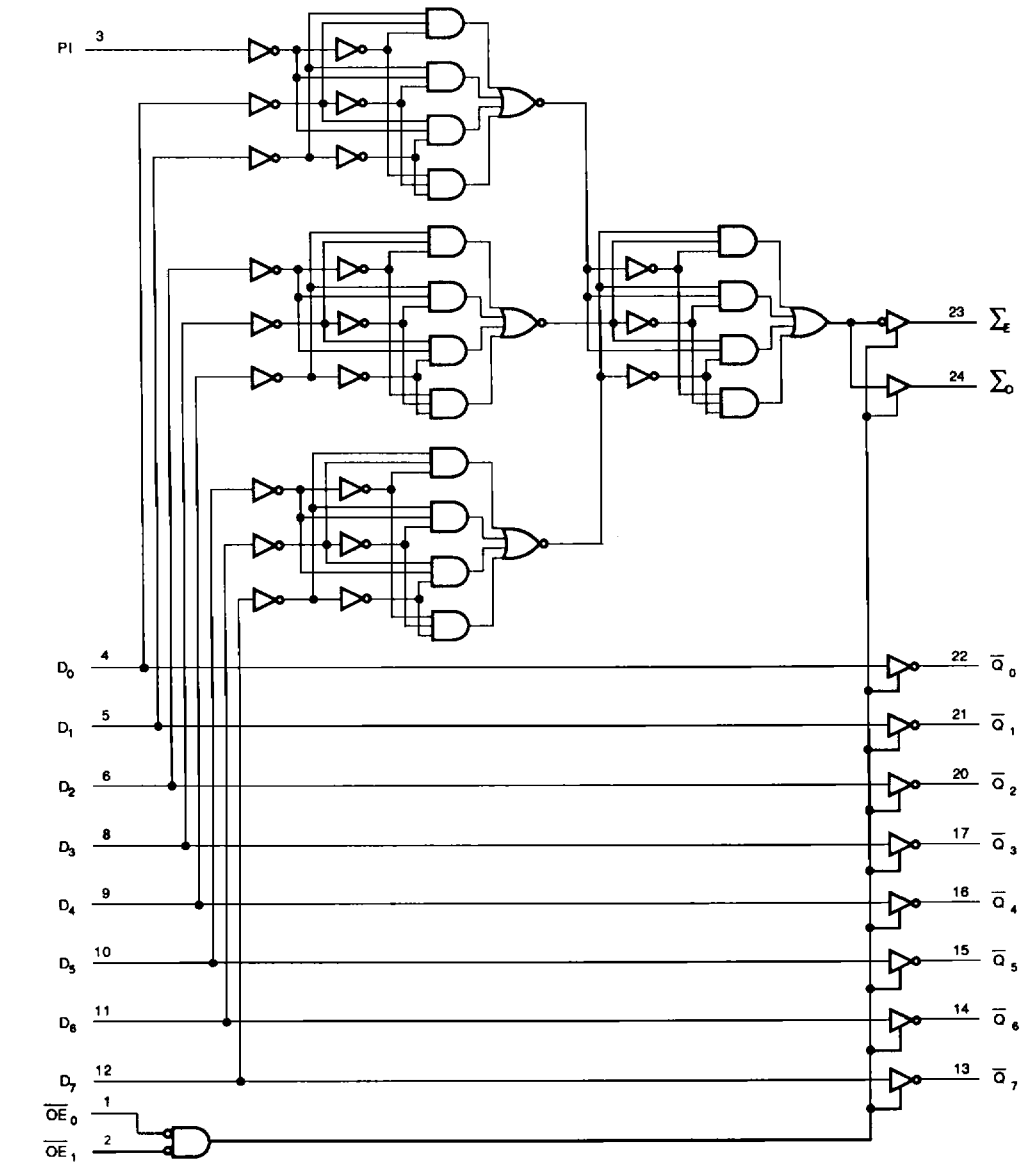
H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state

FUNCTION TABLE for PARITY OUTPUTS

INPUTS	OUTPUTS	
Number of inputs High (PI, D_0-D_7)	Σ_E	Σ_O
Even ------ 0, 2, 4, 6, 8	H	L
Odd ------1, 3, 5, 7, 9	L	H
Any $\overline{OE}_n$=High	Z	Z

H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state

LOGIC DIAGRAM for 'F455



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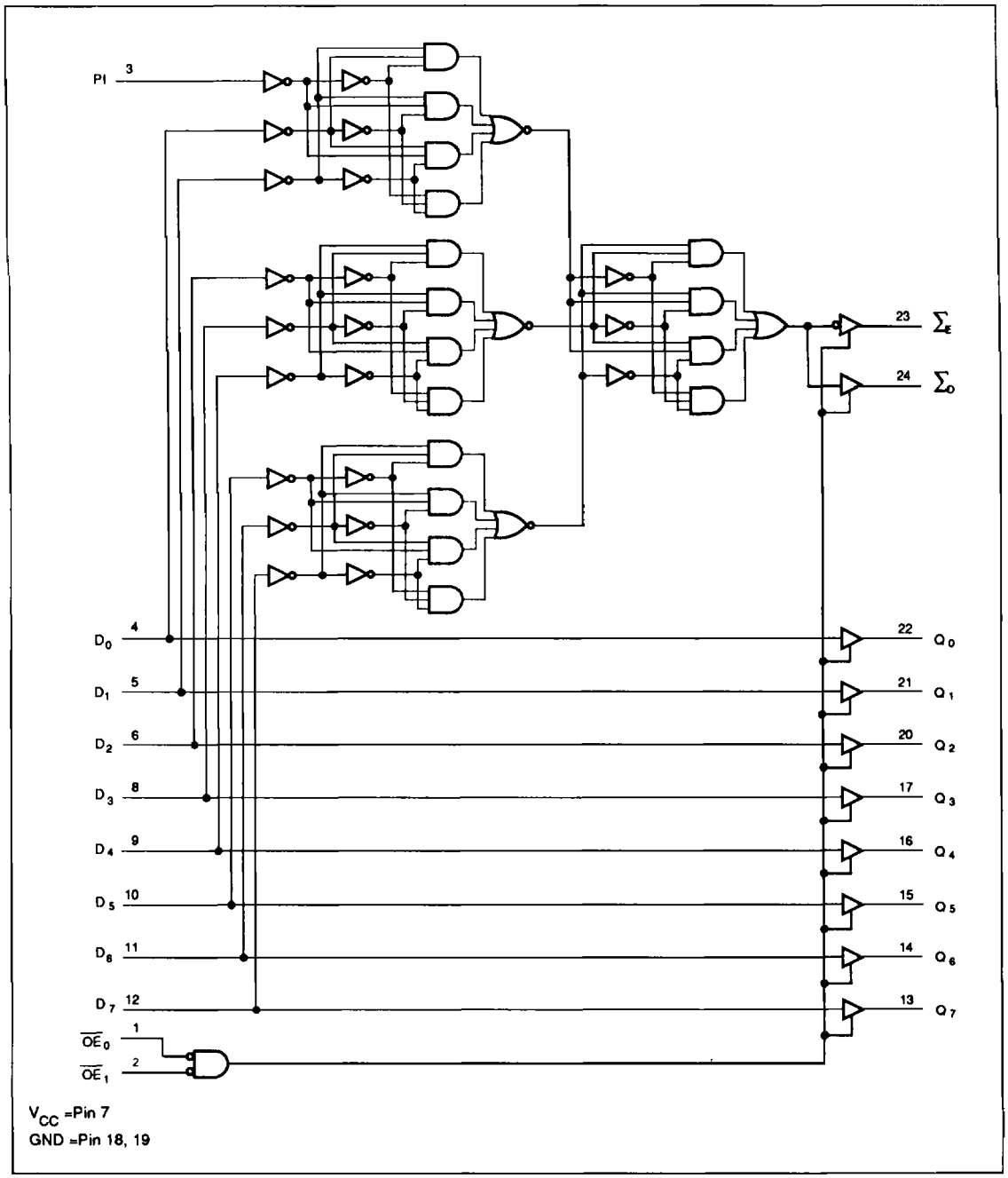
LOGIC DIAGRAM for 'F456



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	D_n	V_{CC} = MAX, V_I = 2.7V					40	µA
		PI, $\overline{OE}_n$						20	µA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V					-40	µA
		PI, $\overline{OE}_n$						-20	µA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	80	mA
		I_{CCL}					78	110	mA
		I_{CCZ}					63	90	mA

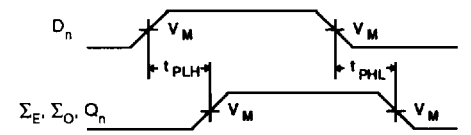
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

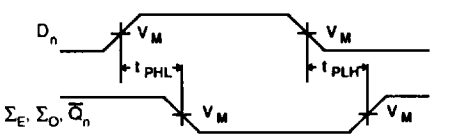
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F455	Waveform 2	2.0 1.0	4.5 2.0	6.5 4.0	2.0 1.0	7.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F456	Waveform 1	2.0 2.5	4.5 5.0	6.5 7.0	2.0 2.5	7.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Σ_E, Σ_O		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	4.0 4.0	7.0 8.0	9.5 10.5	4.0 4.0	10.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	ns

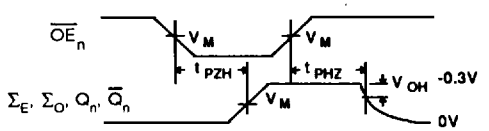
AC WAVEFORMS



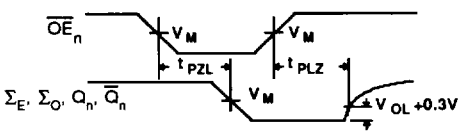
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs



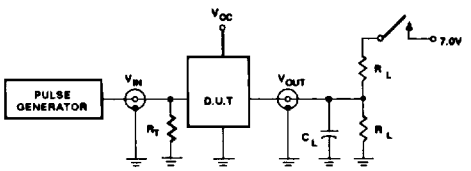
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

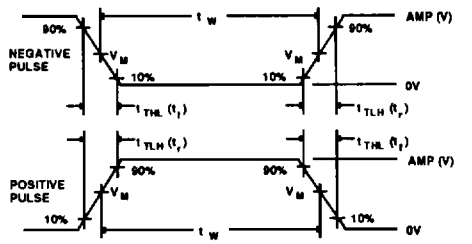
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns