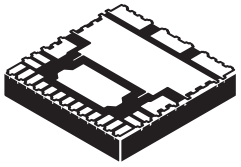
Document Number: MC33894
Rev 3.0, 10/2006

Quad High-Side Switch (Quad 35 mΩ)

33894

QUAD HIGH-SIDE SWITCH 35 mΩ



Bottom View

PNA SUFFIX
98ARL10596D
24-PIN PQFN

The 33894 is one in a family of devices designed for low-voltage automotive and industrial lighting and motor control applications. Its four low $R_{DS(ON)}$ MOSFETs (four 35 mΩ) can control the high sides of four separate resistive or inductive loads.

Programming, control, and diagnostics are accomplished using a 16-bit SPI interface. Additionally, each output has its own parallel input for pulse-width modulation (PWM) control if desired. The 33894 allows the user to program the fault current trip levels and duration of acceptable lamp inrush or motor stall intervals via the SPI. Such programmability allows tight control of fault currents and can protect wiring harnesses and circuit boards as well as loads.

The 33894 is packaged in a power-enhanced 12 x 12 nonleaded Power QFN package with exposed tabs.

Features

- Quad 35 mΩ High-Side Switches (at 25°C)
- Operating Voltage Range of 6.0 V to 27 V with Standby Current < 5.0 μA
- SPI Control of Overcurrent Limit, Overcurrent Fault Blanking Time, Output OFF Open Load Detection, Output ON/OFF Control, Watchdog Timeout, Slew Rates, and Fault Status Reporting
- SPI Status Reporting of Overcurrent, Open and Shorted Loads, Overtemperature, Undervoltage and Overvoltage Shutdown, Fail-Safe Pin Status, and Program Status
- Analog Current Feedback with Selectable Ratio
- Enhanced -16 V Reverse Polarity V_{PWR} Protection
-

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33894PNA/R2	-40°C to 125°C	24 PQFN

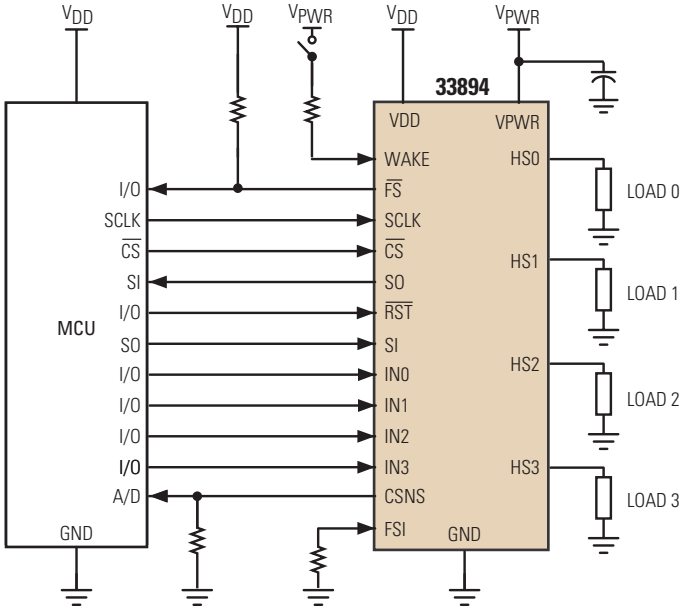


Figure 1. 33894 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

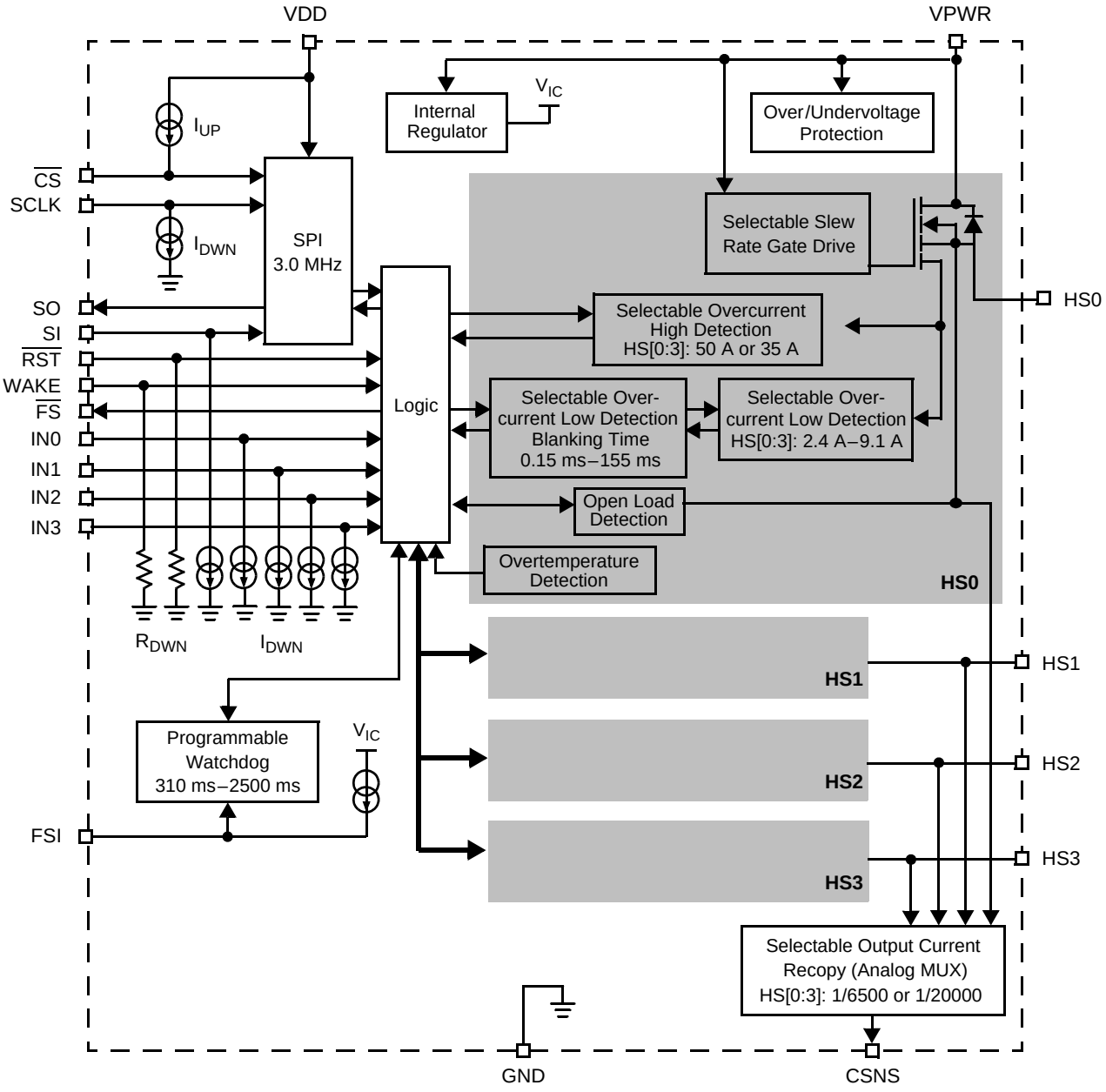


Figure 2. 33894 Simplified Internal Block Diagram

PIN CONNECTIONS

Transparent Top View of Package

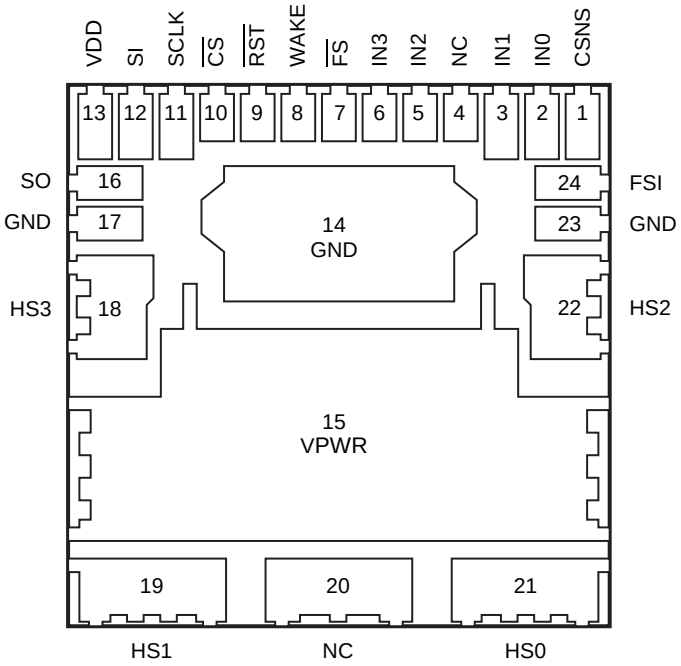


Figure 3. 33894 Pin Connections

Table 1. 33894 Pin Definitions

Functional descriptions of many of these pins can be found in Functional Description on page 16.

Pin Number	Pin Name	Formal Name	Definition
1	CSNS	Output Current Monitoring	The Current Sense pin sources a current proportional to the designated HS0:HS3 output. That current is fed into a ground-referenced resistor and its voltage is monitored by an MCU's A/D. The output to be monitored is selected via the SPI. This pin can be tri-stated through SPI.
2 3 5 6	IN0 IN1 IN2 IN3	Serial Inputs	The IN0:IN3 high-side input pins are used to directly control HS0:HS3 high-side output pins, respectively. An SPI register determines if each input is activated or if the input logic state is ORed or ANDed with the SPI instruction. These pins are to be driven with 5.0 V CMOS levels, and they have an active internal pulldown current source.
4, 20	NC	No Connect	These pins may not be connected.
7	$\overline{FS}$	Fault Status (Active Low)	This pin is an open drain configured output requiring an external pullup resistor to VDD for fault reporting. If a device fault condition is detected, this pin is active LOW. Specific device diagnostic faults are reported via the SPI SO pin.
8	WAKE	Wake	This input pin controls the device mode and watchdog timeout feature if enabled. An internal clamp protects this pin from high damaging voltages when the output is current limited with an external resistor. This input has a passive internal pulldown.
9	$\overline{RST}$	Reset	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low-current sleep mode. The pin also starts the watchdog timer when transitioning from logic [0] to logic [1]. This pin should not be allowed to be logic [1] until V_{DD} is in regulation. This pin has a passive internal pulldown.

Table 1. 33894 Pin Definitions (continued)

Functional descriptions of many of these pins can be found in Functional Description on page 16.

Pin Number	Pin Name	Formal Name	Definition
10	$\overline{CS}$	Chip Select (Active Low)	This input pin is connected to a chip select output of a master MCU. The MCU determines which device is addressed (selected) to receive data by pulling the $\overline{CS}$ pin of the selected device logic LOW, thereby enabling SPI communication with the device. Other *unselected* devices on the serial link having their $\overline{CS}$ pins pulled up logic HIGH disregard the SPI communication data sent. This pin has an active internal pullup current source and requires CMOS logic levels.
11	SCLK	Serial Clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication. It transitions one time per bit transferred at an operating frequency, f_{SPI}, defined by the communication interface. The 50 percent duty cycle CMOS level serial clock signal is idle between command transfers. The signal is used to shift data into and out of the device. This pin has an active internal pulldown current source.
12	SI	Serial Input	This pin is a command data input pin connected to the SPI Serial Data Output of the microcontroller (MCU) or to the SO pin of the previous device of a daisy-chain of devices. The input requires CMOS logic level signals and incorporates an internal active pulldown. Device control is facilitated by the input's receiving the MSB first of a serial 8-bit control command. The MCU ensures data is available upon the falling edge of SCLK. The logic state of SI present upon the rising edge of SCLK loads that bit command into the internal command shift register. This pin has an active internal pulldown current source.
13	VDD	Digital Drain Voltage (Power)	This pin is an external voltage input pin used to supply power to the SPI circuit. In the event V_{DD} is lost, an internal supply provides power to a portion of the logic, ensuring limited functionality of the device.
14, 17, 23	GND	Ground	These pins are the ground for the logic and analog circuitry of the device.
15	VPWR	Positive Power Supply	This pin connects to the positive power supply and is the source of operational power for the device. The V_{PWR} contact is the backside surface mount tab of the package.
16	SO	Serial Output	This output pin is connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device of a daisy-chain of devices. This output will remain tri-stated (high-impedance OFF condition) so long as the $\overline{CS}$ pin of the device is logic HIGH. SO is only active when the $\overline{CS}$ pin of the device is asserted logic LOW. The generated SO output signals are CMOS logic levels. SO output data is available on the falling edge of SCLK and transitions immediately on the rising edge of SCLK.
18 19 21 22	HS3 HS1 HS0 HS2	High-Side Outputs	Protected 35 mΩ high-side power output pins to the load.
24	FSI	Fail-Safe Input	The value of the resistance connected between this pin and ground determines the state of the outputs after a Watchdog timeout occurs. Depending on the resistance value, either all outputs are OFF or the output HSO only is ON. If the FSI pin is left to float up to a logic [1] level, then the outputs HS0 and HS2 will turn ON when in the Fail-Safe state. When the FSI pin is connected to GND, the Watchdog circuit and Fail-Safe operation are disabled. This pin incorporates an active internal pullup current source.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Operating Voltage Range Steady-State	$V_{PWR(SS)}$	 -16 to 41	V
V_{DD} Supply Voltage	V_{DD}	0 to 5.5	V
Input/Output Voltage (1)	$V_{IN[0:3]}$, $\overline{RST}$, FSI, CSNS, SI, SCLK, $\overline{CS}$, $\overline{FS}$	-0.3 to 7.0	V
SO Output Voltage (1)	V_{SO}	-0.3 to V_{DD}+0.3	V
WAKE Input Clamp Current	$I_{CL(WAKE)}$	2.5	mA
CSNS Input Clamp Current	$I_{CL(CSNS)}$	10	mA
Output Current (2)	$I_{HS[0:3]}$	11	A
Output Clamp Energy (3)	$E_{CL[0:3]}$	TBD	J
ESD Voltage (4) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Thermal Resistance (5) Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 <1.0 TBD	°C/W
Peak Pin Reflow Temperature During Solder Mounting (6)	T_{SOLDER}	240	°C

Notes

1. Exceeding voltage limits on IN[0:3], $\overline{RST}$, FSI, CSNS, SI, SO, SCLK, $\overline{CS}$, or $\overline{FS}$ pins may cause a malfunction or permanent damage to the device.
2. Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
3. Active clamp energy using single-pulse method (L = 16 mH, R_L = 0 Ω, V_{PWR} = 12 V, T_J = 150°C).
4. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω) and in accordance with the system module specification with a capacitor > 0.01 μF connected from high-side outputs to GND.
5. Device mounted on a 2s2p test board per JEDEC JESD51-2.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Battery Supply Voltage Range Fully Operational	V_{PWR}	 6.0	 –	 27	V
VPWR Operating Supply Current Outputs ON, HS[0:3] Open	$I_{PWR(ON)}$	 –	 –	 20	mA
VPWR Supply Current Outputs OFF, Open Load Detection Disabled, WAKE > 0.7 V_{DD}, $\overline{RST}$ = $V_{LOGIC\ HIGH}$	$I_{PWR(SBY)}$	 –	 –	 5.0	mA
Sleep State Supply Current (V_{PWR} < 14 V, $\overline{RST}$ < 0.5 V, WAKE < 0.5 V) T_J = 25°C T_J = 85°C	$I_{PWR(SLEEP)}$	 – –	 – –	 10 50	µA
VDD Supply Voltage	$V_{DD(ON)}$	4.5	5.0	5.5	V
VDD Supply Current No SPI Communication 3.0 MHz SPI Communication	$I_{DD(ON)}$	 – –	 – –	 1.0 5.0	mA
VDD Sleep State Current	$I_{DD(SLEEP)}$	–	–	5.0	µA
Overvoltage Shutdown Threshold	$V_{PWR(OV)}$	28	32	36	V
Overvoltage Shutdown Hysteresis	$V_{PWR(OVHYS)}$	0.2	0.8	1.5	V
Undervoltage Shutdown Threshold (7)	$V_{PWR(UV)}$	4.75	5.25	5.75	V
Undervoltage Hysteresis (8)	$V_{PWR(UVHYS)}$	–	0.25	–	V
Undervoltage Power-ON Reset	$V_{PWR(UVPOR)}$	–	–	5.0	V

Notes

7. Output will automatically recover to instructed state when V_{PWR} voltage is restored to normal so long as the V_{PWR} degradation level did not go below the undervoltage power-ON reset threshold. This applies to all internal device logic that is supplied by V_{PWR} and assumes that the external V_{DD} supply is within specification.
8. This applies when the undervoltage fault is not latched (IN[0:3] = 0).

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0:HS3					
Output Drain-to-Source ON Resistance ($I_{HS[0:3]}$ = 5.0 A, T_J = 25°C)	$R_{DS(ON)}$				mΩ
V_{PWR} = 6.0 V		–	–	55	
V_{PWR} = 10 V		–	–	35	
V_{PWR} = 13 V		–	–	35	
Output Drain-to-Source ON Resistance ($I_{HS[0:3]}$ = 5.0 A, T_J = 150°C)	$R_{DS(ON)}$				mΩ
V_{PWR} = 6.0 V		–	–	94	
V_{PWR} = 10 V		–	–	60	
V_{PWR} = 13 V		–	–	60	
Output Source-to-Drain ON Resistance (9)	$R_{DS(ON)}$				mΩ
$I_{HS[0:3]}$ = 5.0 A, T_J = 25°C, V_{PWR} = -12 V		–	–	70	
Output Overcurrent High Detection Levels (9.0 V ≤ V_{PWR} ≤ 16 V)					A
SOCH = 0	I_{OCH0}	40	50	62	
SOCH = 1	I_{OCH1}	28	35	43	
Overcurrent Low Detection Levels (SOCL[2:0], 9.0 V ≤ V_{PWR} ≤ 16 V)					A
000	I_{OCL0}	7.2	9.1	11	
001	I_{OCL1}	6.5	8.15	9.8	
010	I_{OCL2}	5.7	7.2	8.7	
011	I_{OCL3}	5.0	6.25	7.5	
100	I_{OCL4}	4.2	5.25	6.3	
101	I_{OCL5}	3.4	4.3	5.2	
110	I_{OCL6}	2.6	3.35	4.1	
111	I_{OCL7}	1.9	2.4	2.9	
Current Sense Ratio (9.0 V ≤ V_{PWR} ≤ 16 V, CSNS ≤ 4.5 V)					–
DICR D2 = 0	C_{SR0}	–	1/6500	–	
DICR D2 = 1	C_{SR1}	–	1/20000	–	
Current Sense Ratio (C_{SR0}) Accuracy	C_{SR0_ACC}				%
Output Current					
2.0 A		-20	–	20	
5.0 A		-14	–	14	
10 A		-13	–	13	
12.5 A		-12	–	12	
15 A		-13	–	13	
20 A		-13	–	13	

Notes

9. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{PWR}.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0:HS3 (continued)					
Current Sense Ratio (C_{SR1}) Accuracy	C_{SR1_ACC}				%
Output Current					
5.0 A		-25	–	25	
10 A		-19	–	19	
12.5 A		-18	–	18	
15 A		-17	–	17	
20 A		-18	–	18	
25 A		-18	–	18	
Current Sense Clamp Voltage	$V_{CL(CSNS)}$				V
CSNS Open; $I_{HS[0:3]}$ = 11 A		4.5	6.0	7.0	
Open Load Detection Current (10)	I_{OLDC}	30	–	100	µA
Output Fault Detection Threshold	$V_{OFD(THRES)}$				V
Output Programmed OFF		2.0	3.0	4.0	
Output Negative Clamp Voltage	V_{CL}				V
0.5 A ≤ $I_{HS[0:3]}$ ≤ 2.0 A, Output OFF		-20	–	–	
Overtemperature Shutdown (11)	T_{SD}	155	175	190	°C
Overtemperature Shutdown Hysteresis (11)	$T_{SD(HYS)}$	5.0	–	20	°C

Notes

10. Output OFF Open Load Detection Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF.
11. Guaranteed by process monitoring. Not production tested.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE					
Input Logic High Voltage (12)	V_{IH}	0.7 V_{DD}	–	–	V
Input Logic Low Voltage (12)	V_{IL}	–	–	0.2 V_{DD}	V
Input Logic Voltage Hysteresis (12)	$V_{IN(HYS)}$	100	350	750	mV
Input Logic Pulldown Current (SCLK, SI, IN[0:3])	I_{DWN}	5.0	–	20	µA
$\overline{RST}$ Input Voltage Range	$V_{\overline{RST}}$	4.5	5.0	5.5	V
SO, $\overline{FS}$ Tri-State Capacitance (13)	C_{SO}	–	–	20	pF
Input Logic Pulldown Resistor ($\overline{RST}$) and WAKE	R_{DWN}	100	200	400	kΩ
Input Capacitance (14)	C_{IN}	–	4.0	12	pF
Wake Input Clamp Voltage (15) $I_{CL(WAKE)}$ < 2.5 mA	$V_{CL(WAKE)}$	7.0	–	14	V
Wake Input Forward Voltage $I_{CL(WAKE)}$ = -2.5 mA	$V_{F(WAKE)}$	-2.0	–	-0.3	V
SO High-State Output Voltage I_{OH} = 1.0 mA	V_{SOH}	0.8 V_{DD}	–	–	V
$\overline{FS}$, SO Low-State Output Voltage I_{OL} = -1.6 mA	V_{SOL}	–	0.2	0.4	V
SO Tri-State Leakage Current $\overline{CS}$ ≥ 0.7 V_{DD}	$I_{SO(LEAK)}$	-5.0	0	5.0	µA
Input Logic Pullup Current (16) $\overline{CS}$, V_{IN} > 0.7 V_{DD}	I_{UP}	5.0	–	20	µA
FSI Input pin External Pulldown Resistance (17)	RFS				kΩ
FSI Disabled, HS[0:3] Indeterminate	RFS_{DIS}	–	0	1.0	
FSI Enabled, HS[0:3] OFF	RFS_{OFFOFF}	6.0	6.5	7.0	
FSI Enabled, HS0 ON, HS[1:3] OFF	RFS_{ONOFF}	15	17	19	
FSI Enabled, HS0 and HS2 ON, HS1 and HS3 OFF	RFS_{ONON}	40	Infinite	–	

Notes

12. Upper and lower logic threshold voltage range applies to SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN[0:3], and WAKE input signals. The WAKE and $\overline{RST}$ signals may be supplied by a derived voltage referenced to V_{PWR}.
13. Parameter is guaranteed by process monitoring but is not production tested.
14. Input capacitance of SI, $\overline{CS}$, SCLK, $\overline{RST}$, and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
15. The current must be limited by a series resistance when using voltages > 7.0 V.
16. Pullup current is with $\overline{CS}$ OPEN. $\overline{CS}$ has an active internal pullup to V_{DD}.
17. The selection of the RFS must take into consideration the tolerance, temperature coefficient and lifetime duration to assure that the resistance value will always be within the desired (specified) range.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0:HC3					
Output Rising Slow Slew Rate A (DICR D3 = 0) (18) 9.0 V < V_{PWR} < 16 V	SR_{RA_SLOW}	0.1	0.3	0.5	V/µs
Output Rising Slow Slew Rate B (DICR D3 = 0) (19) 9.0 V < V_{PWR} < 16 V	SR_{RB_SLOW}	0.015	0.05	0.15	V/µs
Output Rising Fast Slew Rate A (DICR D3 = 1) (18) 9.0 V < V_{PWR} < 16 V	SR_{RA_FAST}	0.2	0.5	1.5	V/µs
Output Rising Fast Slew Rate B (DICR D3 = 1) (19) 9.0 V < V_{PWR} < 16 V	SR_{RB_FAST}	0.015	0.05	0.5	V/µs
Output Falling Slow Slew Rate A (DICR D3 = 0) (18) 9.0 V < V_{PWR} < 16 V	SR_{FA_SLOW}	0.1	0.3	0.5	V/µs
Output Falling Slow Slew Rate B (DICR D3 = 0) (19) 9.0 V < V_{PWR} < 16 V	SR_{FB_SLOW}	0.015	0.05	0.15	V/µs
Output Falling Fast Slew Rate A (DICR D3 = 1) (18) 9.0 V < V_{PWR} < 16 V	SR_{FA_FAST}	0.4	1.0	2.0	V/µs
Output Falling Fast Slew Rate B (DICR D3 = 1) (19) 9.0 V < V_{PWR} < 16 V	SR_{FB_FAST}	0.05	0.175	0.6	V/µs
Output Turn-ON Delay Time in Fast/Slow Slew Rate (20) DICR = 0, DICR = 1	$t_{DLY(ON)}$	2.0	30	200	µs
Output Turn-OFF Delay Time in Slow Slew Rate Mode (21) DICR = 0	$t_{DLY\_SLOW(OFF)}$	40	460	1000	µs
Output Turn-OFF Delay Time in Fast Slew Rate Mode (21) DICR = 1	$t_{DLY\_FAST(OFF)}$	20	120	400	µs
Overcurrent Low Detection Blanking Time (OCLT[1:0]) 00 01 (22) 10 11	 t_{OCL0} t_{OCL1} t_{OCL2} t_{OCL3}	 108 – 55 0.08	 155 – 75 0.15	 202 – 95 0.25	ms

Notes

18. Rise and Fall Slew Rates A measured across a 5.0 Ω resistive load at high-side output = 0.5 V to V_{PWR}-3.5 V (see Figure 4, page 13). These parameters are guaranteed by process monitoring.
19. Rise and Fall Slew Rates B measured across a 5.0 Ω resistive load at high-side output = 0.5 V to V_{PWR}-3.5 V (see Figure 4). These parameters are guaranteed by process monitoring.
20. Turn-ON delay time measured from rising edge of any signal (IN[0:3], SCLK, $\overline{CS}$) that would turn the output ON to $V_{HS[0:3]}$ = 0.5 V with R_L = 5.0 Ω resistive load.
21. Turn-OFF delay time measured from falling edge of any signal (IN[0:3], SCLK, $\overline{CS}$) that would turn the output OFF to $V_{HS[0:3]}$ = V_{PWR}-0.5 V with R_L = 5.0 Ω resistive load.
22. This logical bit is not defined. Do not use.

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0:HC3 (CONTINUED)					
Overcurrent High Detection Blanking Time	t_{OCH}	1.0	10	20	µs
$\overline{CS}$ to CSNS Valid Time (23)	t_{CNSVAL}	–	–	10	µs
Watchdog Timeout (WD[1:0]) (24)					ms
00	t_{WDTO0}	496	620	806	
01	t_{WDTO1}	248	310	403	
10	t_{WDTO2}	2000	2500	3250	
11	t_{WDTO3}	1000	1250	1625	

Notes

23. Time necessary for the CSNS to be with ±5% of the targeted value.
24. Watchdog timeout delay measured from the rising edge of WAKE or $\overline{RST}$ from a sleep state condition, to output turn-ON with the output driven OFF and FSI floating. The values shown are for WDR setting of [00]. The accuracy of t_{WDTO} is consistent for all configured watchdog timeouts.

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE CHARACTERISTICS					
Maximum Frequency of SPI Operation	f_{SPI}	–	–	3.0	MHz
Required Low State Duration for $\overline{RST}$ (25)	$t_{W\overline{RST}}$	–	50	350	ns
Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (26)	$t_{\overline{CS}}$	–	–	300	ns
Rising Edge of $\overline{RST}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (26)	t_{ENBL}	–	–	5.0	µs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time) (26)	t_{LEAD}	–	50	167	ns
Required High State Duration of SCLK (Required Setup Time) (26)	t_{WSCLKH}	–	–	167	ns
Required Low State Duration of SCLK (Required Setup Time) (26)	t_{WSCLKL}	–	–	167	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time) (26)	t_{LAG}	–	50	167	ns
SI to Falling Edge of SCLK (Required Setup Time) (27)	$t_{SI(SU)}$	–	25	83	ns
Falling Edge of SCLK to SI (Required Setup Time) (27)	$t_{SI(HOLD)}$	–	25	83	ns
SO Rise Time C_L = 200 pF	t_{RSO}	–	25	50	ns
SO Fall Time C_L = 200 pF	t_{FSO}	–	25	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time (27)	t_{RSI}	–	–	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time (27)	t_{FSI}	–	–	50	ns
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (28)	$t_{SO(EN)}$	–	–	145	ns
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (29)	$t_{SO(DIS)}$	–	65	145	ns
Time from Rising Edge of SCLK to SO Data Valid (30) 0.2 V_{DD} ≤ SO ≥ 0.8 V_{DD}, C_L = 200 pF	t_{VALID}	–	65	105	ns

Notes
25. $\overline{RST}$ low duration measured with outputs enabled and going to OFF or disabled condition.
26. Maximum setup time required for the 33894 is the minimum guaranteed time needed from the microcontroller.
27. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
28. Time required for output status data to be available for use at SO. 1.0 kΩ on pullup on $\overline{CS}$.
29. Time required for output status data to be terminated at SO. 1.0 kΩ on pullup on $\overline{CS}$.
30. Time required to obtain valid data out from SO following the rise of SCLK.

TIMING DIAGRAMS

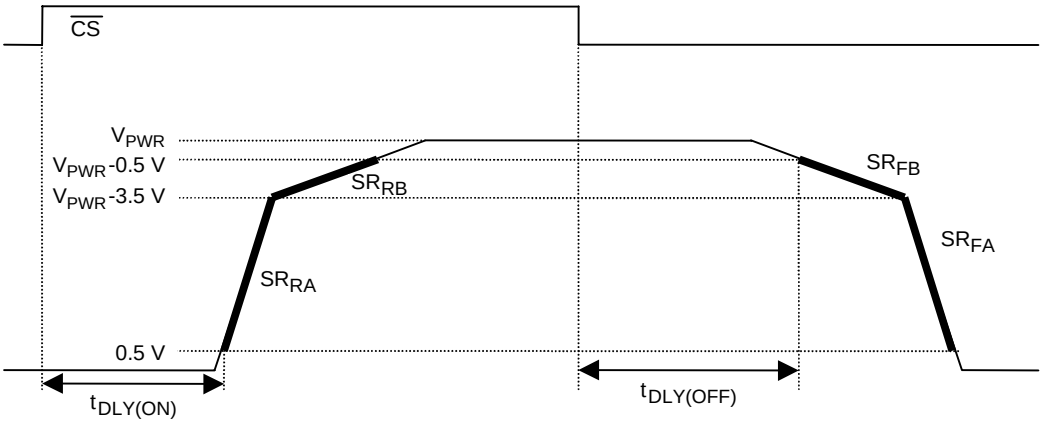


Figure 4. Output Slew Rate and Time Delays

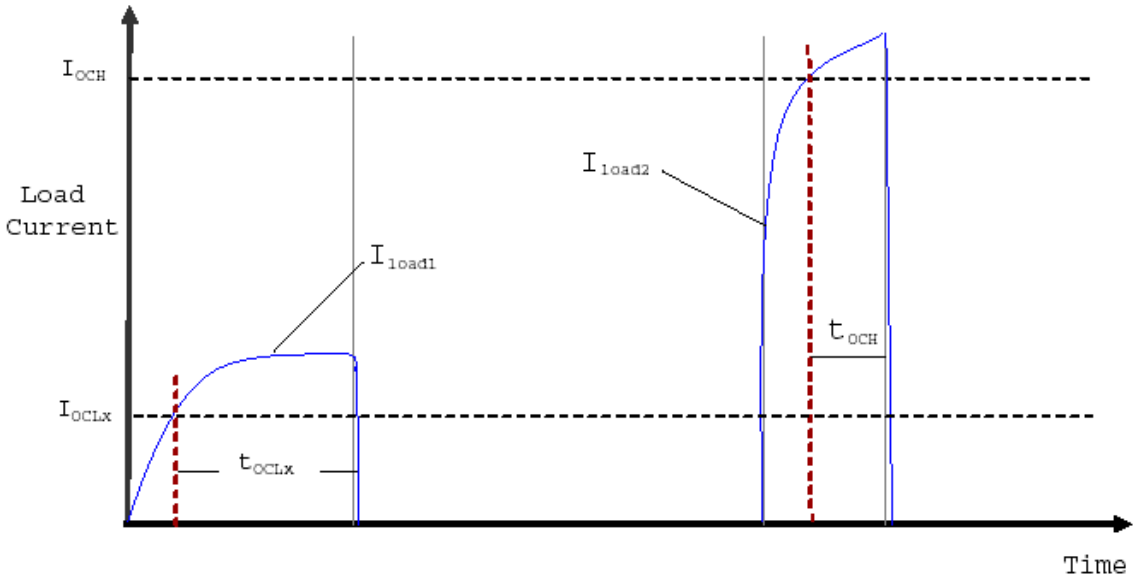


Figure 5. Overcurrent Shutdown

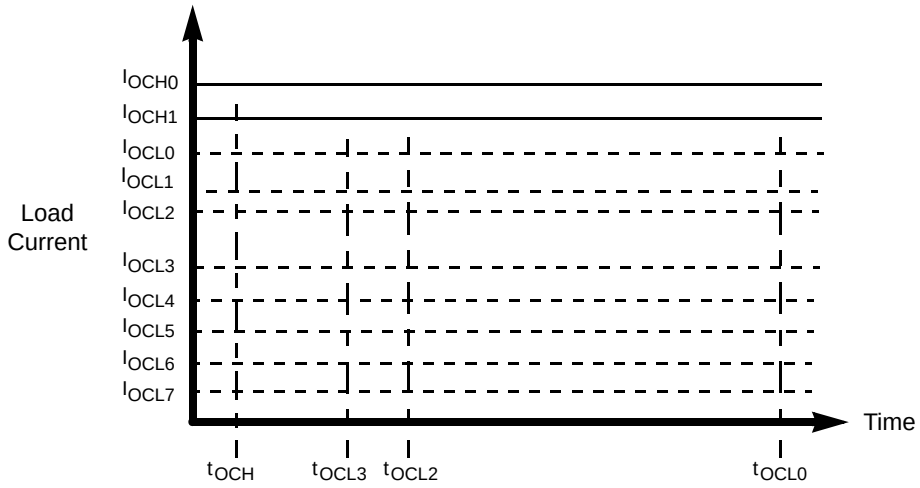


Figure 6. Overcurrent Low and High Detection

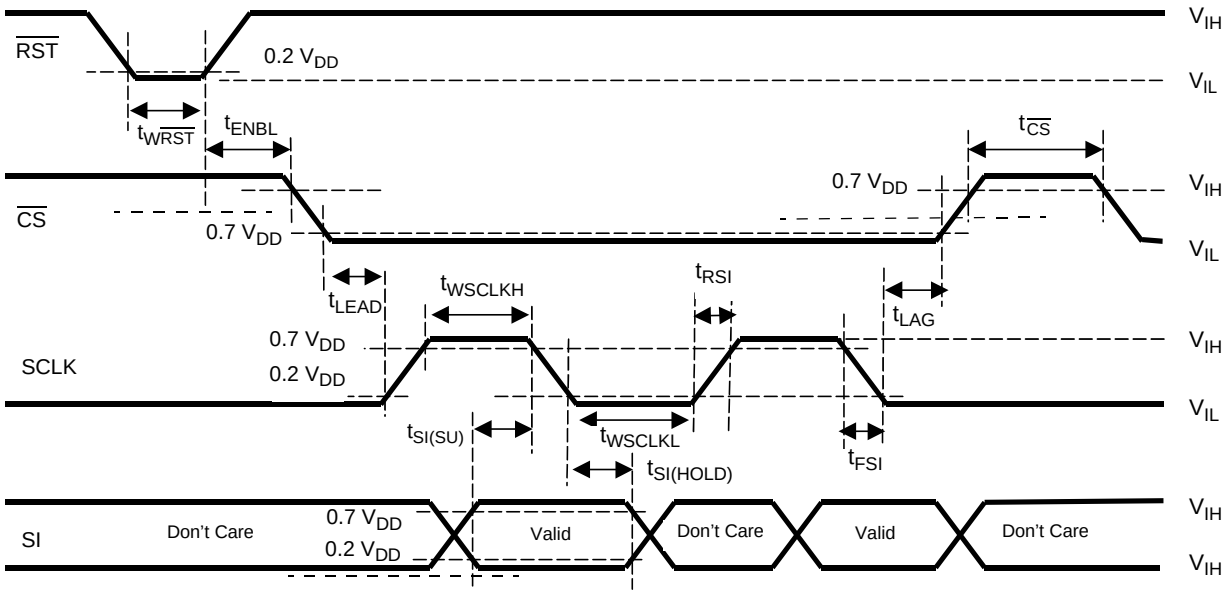


Figure 7. Input timing Switching Characteristics

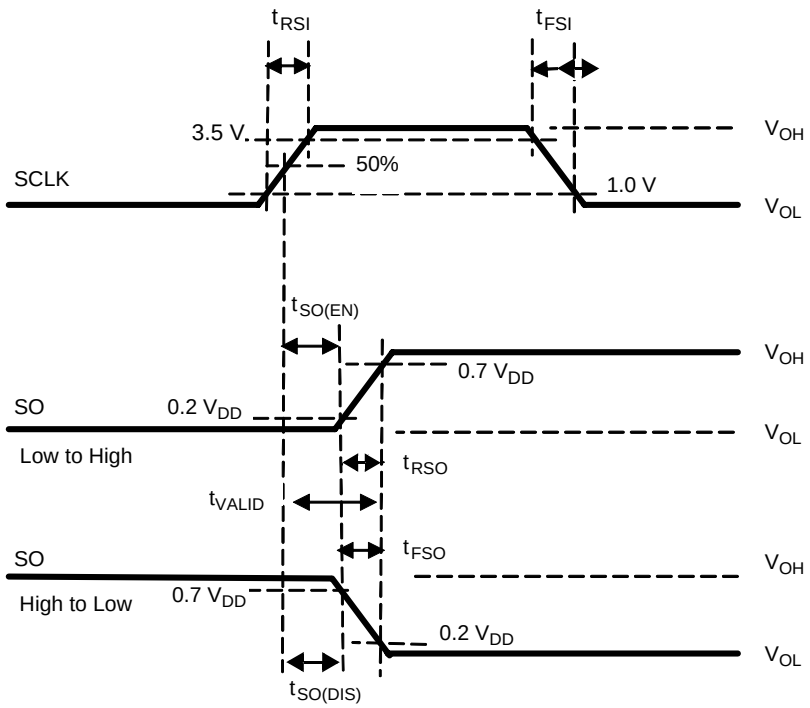


Figure 8. SCLK Waveform and Valid SO Data Delay Time

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33894 is one in a family of devices designed for low-voltage automotive and industrial lighting and motor control applications. Its four low $R_{DS(ON)}$ MOSFETs (four 35 mΩ) can control the high sides of four separate resistive or inductive loads.

Programming, control, and diagnostics are accomplished using a 16-bit SPI interface. Additionally, each output has its own parallel input for PWM control if desired. The 33894 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush or motor stall intervals. Such programmability allows tight control of fault currents and can protect wiring harnesses and circuit boards as well as loads.

The 33894 is packaged in a power-enhanced 12 x 12 nonleaded PQFN package with exposed tabs.

FUNCTIONAL PIN DESCRIPTION

SPI PROTOCOL DESCRIPTION

The SPI interface has a full duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Input (SI), Serial Output (SO), Serial Clock (SCLK), and Chip Select ($\overline{CS}$).

The SI/SO pins of the 33894 follow a first-in first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V CMOS logic levels.

The SPI lines perform the following functions:

SERIAL INPUT (SI)

This is a serial interface (SI) command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 to D0. The internal registers of the 33894 are configured and controlled using a 5-bit addressing scheme described in Table 7, page 19. Register addressing and configuration are described in Table 8, page 20. The SI input has an active internal pulldown, I_{DWN}.

SERIAL OUTPUT (SO)

The SO data pin is a tri-stateable output from the shift register. The SO pin remains in a high-impedance state until the $\overline{CS}$ pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, and the state of the key inputs. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. Fault and input status descriptions are provided in Table 15, page 23.

SERIAL CLOCK (SCLK)

The SCLK pin clocks the internal shift registers of the 33894 device. The serial input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal while the serial output (SO) pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important the SCLK pin be in a logic low state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended the SCLK pin be in logic [0] whenever the device is not accessed ($\overline{CS}$ logic [1] state). SCLK has an active internal pulldown. When $\overline{CS}$ is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high impedance) (see Figure 9, page 19).

CHIP SELECT ($\overline{CS}$)

The $\overline{CS}$ pin enables communication with the master microcontroller (MCU). When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the MCU. The 33894 latches in data from the input shift registers to the addressed registers on the rising edge of $\overline{CS}$. The device transfers status information from the power output to the Shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is logic [0]. $\overline{CS}$ should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. $\overline{CS}$ has an active internal pullup, I_{UP}.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

The 33894 has four operating modes: Sleep, Normal, Fault, and Fail-Safe. Table 5 summarizes details contained in succeeding paragraphs.

Table 5. Fail-Safe Operation and Transitions to Other 33894 Modes

Mode	$\overline{FS}$	WAKE	$\overline{RST}$	WDTO	Comments
Sleep	x	0	0	x	Device is in Sleep mode. All outputs are OFF
Normal	1	x	1	No	Normal mode. Watchdog is active if enabled.
Fault	0	1	1	No	Device is currently in Fault mode. The faulted output(s) is (are) OFF.
	0	1	0		
	0	x	1		
Fail-Safe	1	0	1	Yes	Watchdog has timed out and the device is in Fail-Safe mode. The outputs are as configured with the RFS resistor connected to FSI. $\overline{RST}$ and WAKE must be transitioned to logic [0] simultaneously to bring the device out of the Fail-safe mode or momentarily tied the FSI pin to ground.
	1	1	1		
	1	1	0		

x=Don't care.

SLEEP MODE

The default mode of the 33894 is the Sleep mode. This is the state of the device after first applying battery voltage (V_{PWR}) prior to any I/O transitions. This is also the state of the device when the WAKE and $\overline{RST}$ are both logic [0]. In the Sleep mode, the output and all unused internal circuitry, such as the internal 5.0 V regulator, are OFF to minimize current draw. In addition, all SPI-configurable features of the device are as if set to logic [0]. The 33894 will transition to the Normal or Fail-Safe operating modes based on the WAKE and $\overline{RST}$ inputs as defined in Table 5.

NORMAL MODE

The 33894 is in Normal mode when:

- V_{PWR} is within the normal voltage range.
- $\overline{RST}$ pin is logic [1].
- No fault has occurred.

FAIL-SAFE MODE

Fail-Safe Mode and Watchdog

If the FSI input is not grounded, the watchdog timeout detection is active when either the WAKE or the $\overline{RST}$ input pin transitions from logic [0] to logic [1]. The WAKE input is capable of being pulled up to V_{PWR} with a series of limiting resistance limiting the internal clamp current according to the specification.

The Watchdog timeout is a multiple of an internal oscillator and is specified in the Table 14, page 22. As long as the WD bit (D15) of an incoming SPI message is toggled within the minimum watchdog timeout period (WDTO), based on the programmed value of the WDR, the device will operate normally. If an internal watchdog timeout occurs before the WD bit, the device will revert to a Fail-Safe mode until the device is reinitialized.

During the Fail-Safe mode, the outputs will be ON or OFF depending upon the resistor RFS connected to the FSI pin, regardless of the state of the various direct inputs and modes (Table 6).

Table 6. Output State During Fail-Safe Mode

RFS (kΩ)	High-Side State
0	Fail-Safe Mode Disabled
6.0	All HS OFF
15	HS0 ON HS1:HS3 OFF
30	HS0 and HS2 ON HS1 and HS3 OFF

In the Fail-Safe mode, the SPI register content is retained except for overcurrent high and low detection levels and timing, which are reset to their default value (SOCL, SOCH, and OCTL). Then the watchdog, overvoltage, overtemperature, and overcurrent circuitry (with default value) are fully operational.

The Fail-Safe mode can be detected by monitoring the WDTO bit D2 of the WD register. This bit is logic [1] when the device is in Fail-Safe mode. The device can be brought out of the Fail-Safe mode by transitioning the WAKE and $\overline{RST}$ pins from logic [1] to logic [0] or forcing the FSI pin to logic [0]. Table 5 summarizes the various methods for resetting the device from the latched Fail-Safe mode.

If the FSI pin is tied to GND, the Watchdog fail-safe operation is disabled.

Loss of V_{DD}

If the external 5.0 V supply is not within specification, or even disconnected, all register content is reset. The outputs can still be driven by the direct inputs IN0:IN3. The 33894 uses the battery input to power the output MOSFET-related current sense circuitry and any other internal logic, providing fail-safe device operation with no V_{DD} supplied. In this state, the watchdog, overvoltage, overtemperature, and overcurrent circuitry are fully operational with default values.

FAULT MODE

This 33894 indicates the faults below as they occur by driving the $\overline{FS}$ pin to logic [0]:

- Overtemperature fault
- Overvoltage and undervoltage fault
- Open load fault
- Overcurrent fault (high and low)

The $\overline{FS}$ pin automatically returns to logic [1] when the fault condition is removed, except for overcurrent and in some cases undervoltage faults.

Fault information is retained in the Fault register and is available (and reset) via the SO pin during the first valid SPI communication (refer to Table 16, page 23).

Overtemperature Fault (Non-Latching)

The 33894 incorporates overtemperature detection and shutdown circuitry in the output structure. Overtemperature detection is enabled when the output is in the ON state.

For the output, an overtemperature fault (OTF) condition results in the faulted output turning OFF until the temperature falls below the $T_{SD(HYS)}$. This cycle will continue indefinitely until action is taken by the MCU to shut OFF the output, or until the offending load is removed.

When experiencing this fault, the OTF fault bit will be set in the Status register and cleared after either a valid SPI read or a power reset of the device.

Overvoltage Fault (Non-Latching)

The 33894 shuts down the output during an overvoltage fault (OVF) condition on the V_{PWR} pin. The output remains in the OFF state until the overvoltage condition is removed. When experiencing this fault, the OVF fault bit is set in the bit D1 and cleared after either a valid SPI read or a power reset of the device.

The overvoltage protection can be disabled through SPI (bit OV_DIS). When disabled, the returned SO bit OD13 still reflects any overvoltage condition (overvoltage warning).

Undervoltage Shutdown (Latching or Non-Latching)

The output latches OFF at some battery voltage between 4.75 V and 5.75 V. As long as the V_{DD} level stays within the normal specified range, the internal logic states within the device will be sustained. This ensures that when the battery level then returns above 5.75 V, the 33894 can be returned to the state that it was in prior to the low V_{PWR} excursion. Once the output latches OFF, the outputs must be turned OFF and ON again to re-enable them. In the case IN1:IN0=0, this fault is non-latched.

The undervoltage protection can be disabled through SPI (bit UV_DIS). When disabled, the returned SO bit OD14 still reflects any undervoltage condition (undervoltage warning).

Open Load Fault (Non-Latching)

The 33894 incorporates open load detection circuitry on the output. Output open load fault (OLF) is detected and reported as a fault condition when the output is disabled (OFF). The open load fault is detected and latched into the Status register after the internal gate voltage is pulled low enough to turn OFF the output. The OLF fault bit is set in the Status register. If the open load fault is removed, the Status register will be cleared after reading the register.

The open load protection can be disabled trough SPI (bit OL_DIS).

Overcurrent Fault (Latching)

The 33894 has eight programmable overcurrent low detection levels (I_{OCL}) and two programmable overcurrent high detection levels (I_{OCH}) for maximum device protection. The two selectable, simultaneously active overcurrent detection levels, defined by I_{OCH} and I_{OCL}, are illustrated in Figure 6, page 14. The eight different overcurrent low detect levels (I_{OCL0}:I_{OCL7}) are illustrated in Figure 6.

If the load current level ever reaches the selected overcurrent low detection level and the overcurrent condition exceeds the programmed overcurrent time period (t_{OCx}), the device will latch the output OFF.

If at any time the current reaches the selected I_{OCH} level, then the device will immediately latch the fault and turn OFF the output, regardless of the selected t_{OCLx} driver.

For both cases, the device output will stay off indefinitely until the device is commanded OFF and then ON again.

REVERSE BATTERY

The output survives the application of reverse voltage as low as -16 V. Under these conditions, the output's gate is enhanced to keep the junction temperature less than 150°C. The ON resistance of the output is fairly similar to that in the Normal mode. No additional passive components are required.

GROUND DISCONNECT PROTECTION

In the event the 33894 ground is disconnected from load ground, the device protects itself and safely turns OFF the output regardless of the state of the output at the time of disconnection.

SOLDERING INFORMATION

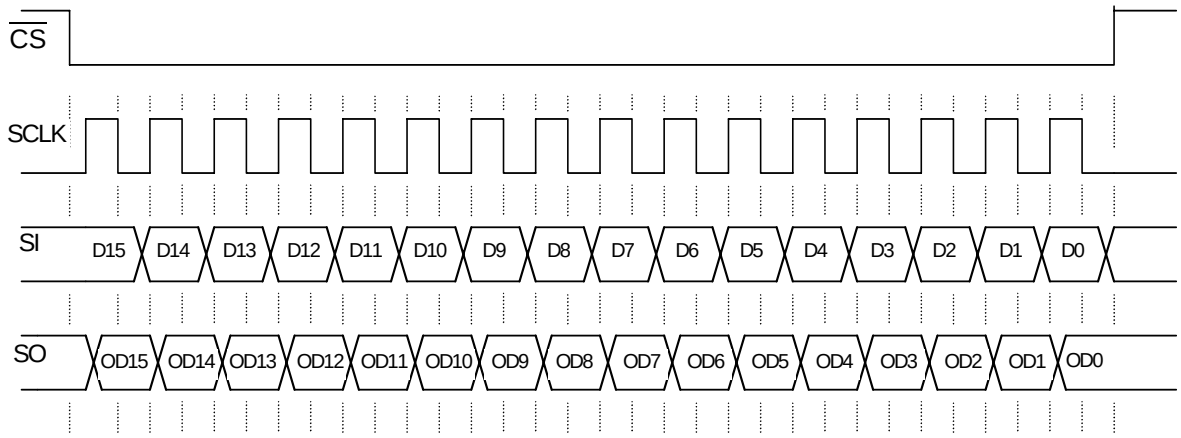
The 33894 is packaged in a surface mount power package intended to be soldered directly on the printed circuit board.

The 33894 was qualified in accordance with JEDEC standards JESD22-A113-B and J-STD-020A. The recommended reflow conditions are as follows:

- Convection: 235°C +5.0/-0°C
- Vapor Phase Reflow (VPR): 235°C +5.0/-0°C
- Infrared (IR)/Convection: 235°C +5.0/-0°C

The maximum peak temperature during the soldering process should not exceed 240°C. The time at maximum temperature should range from 10 s to 40 s maximum.

LOGIC COMMANDS AND REGISTERS



Notes 1. $\overline{RST}$ is a logic [1] state during the above operation.
2. D15:D0 relate to the most recent ordered entry of data into the device.
3. OD15:OD0 relate to the first 16 bits of ordered fault and status data out of the device.

Figure 9. Single 16-Bit Word SPI Communication

SERIAL INPUT COMMUNICATION

SPI communication is accomplished using 16-bit messages. A message is transmitted by the MCU starting with the MSB D15 and ending with the LSB, D0 (Table 7). Each incoming command message on the SI pin can be interpreted using the following bit assignments: the MSB, D15, is the watchdog bit. In some cases, output selection is done with bits D12:D11. The next three bits, D10:D8, are used to select the command register. The remaining five bits, D4:D0, are used to configure and control the outputs and their protection features.

Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable, or to confirm transmitted data, as long as the messages are all multiples of 16 bits. Any attempt made to latch in a message that is not 16 bits will be ignored.

The 33894 has defined registers, which are used to configure the device and to control the state of the outputs. Table 8, page 20, summarizes the SI registers.

Table 7. SI Message Bit Assignment

Bit Sig	SI Msg Bit	Message Bit Description
MSB	D15	Watchdog in: toggled to satisfy watchdog requirements.
	D14:D15	Not used.
	D12:D11	Register address bits used in some cases for output selection.
	D10:D8	Register address bits.
	D7:D5	Not used.
	D4:D1	Used to configure the inputs, outputs, and the device protection features and SO status content.
LSB	D0	Used to configure the inputs, outputs, and the device protection features and SO status content.

Table 8. Serial Input Address and Configuration Bit Map

SI Register	SI Data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STATR	WDIN	x	x	x	x	0	0	0	x	x	x	SOA4	SOA3	SOA2	SOA1	SOA0
OCR0	WDIN	x	x	x	0	0	0	1	x	x	x	x	IN3_SPI	IN2_SPI	IN1_SPI	IN0_SPI
OCR1	WDIN	x	x	x	1	0	0	1	x	x	x	x	CSNS3 $\overline{EN}$	CSNS2 $\overline{EN}$	CSNS1 $\overline{EN}$	CSNS0 $\overline{EN}$
SOCHLR_s	WDIN	x	x	A_1	A_0	0	1	0	x	x	x	x	SOCH_s	SOCL2_s	SOCL1_s	SOCL0_s
CDTOLR_s	WDIN	x	x	A_1	A_0	0	1	1	x	x	x	x	OL_DIS_s	OCL_DIS_s	OCLT1_s	OCLT0_s
DICR_s	WDIN	x	x	A_1	A_0	1	0	0	x	x	x	x	FAST_SR_s	CSNS_high_s	DIR_DIS_s	A/O_s
UOVR	WDIN	x	x	x	0	1	0	1	x	x	x	x	x	x	UV_DIS	OV_DIS
WDR	WDIN	x	x	x	1	1	0	1	x	x	x	x	x	x	WD1	WD0
NAR	WDIN	x	x	x	x	1	1	0	x	x	x	x	No Action (Allow Toggling of D15–WDIN)			
TEST	WDIN	x	x	x	x	1	1	1	x	x	x	x	Freescale Internal Use (Test)			

x=Don't care.
s=Output selection with the bits A_1A_0 as defined in Table 9.

DEVICE REGISTER ADDRESSING

The following section describes the possible register addresses and their impact on device operation.

ADDRESS XX000—STATUS REGISTER (STATR)

The STATR register is used to read the device status and the various configuration register contents without disrupting the device operation or the register contents. The register bits D4:D0 determine the content of the first sixteen bits of SO data. In addition to the device status, this feature provides the ability to read the content of the OCR0, OCR1, SOCHLR, CDTOLR, DICR, UOVR, WDR, and NAR registers. (Refer to the section entitled Serial Output Communication (Device Status Return Data) beginning on page 22.)

ADDRESS X0001—OUTPUT CONTROL REGISTER (OCR0)

The OCR0 register allows the MCU to control the ON/OFF state of four outputs through the SPI. Incoming message bit D3:D0 reflects the desired states of the four high-side outputs (INx_SPI), respectively. A logic [1] enables the corresponding output switch and a logic [0] turns it OFF.

ADDRESS X1001—OUTPUT CONTROL REGISTER (OCR1)

Incoming message bits D3:D0 reflect the desired output that will be mirrored on the Current Sense (CSNS) pin. A logic [1] on message bits D3:D0 enables the CSNS pin for outputs HS3:HS0, respectively. In the event the current sense is enabled for multiple outputs, the current will be summed. In the event that bits D3:D0 are all logic [0], the output CSNS will be tri-stated. This is useful when several CSNS pins of several devices share the same A/D converter.

ADDRESS $A_1A_0$010—SELECT OVERCURRENT HIGH AND LOW REGISTER (SOCHLR_S)

The SOCHLR_s register allows the MCU to configure the output overcurrent low and high detection levels, respectively. Each output "s" is independently selected for configuration based on the state of the D12:D11 bits (Table 9).

Table 9. Output Selection

A_1 (D12)	A_0 (D11)	HS_s
0	0	HS0
0	1	HS1
1	0	HS2
1	1	HS3

Each output can be configured to different levels. In addition to protecting the device, this slow blow fuse emulation feature can be used to optimize the load requirements matching system characteristics. Bits D2:D0 set the overcurrent low detection level to one of eight possible levels, as shown in Table 10, page 21. Bit D3 sets the overcurrent high detection level to one of two levels, as outlined in Table 11, page 21.

Table 10. Overcurrent Low Detection Levels

SOCL2_s* (D2)	SOCL1_s* (D1)	SOCL0_s* (D0)	Overcurrent Low Detection (Amperes)
			HS0:HS3
0	0	0	9.1
0	0	1	8.15
0	1	0	7.2
0	1	1	6.25
1	0	0	5.25
1	0	1	4.3
1	1	0	3.35
1	1	1	2.4

* "_s" refers to the output, which is selected through bits D12:D11; refer to Table 9, page 20.

Table 11. Overcurrent High Detection Levels

SOCH_s* (D3)	Overcurrent High Detection (Amperes)
	HS0:HS3
0	50
1	35

* "_s" refers to the output, which is selected through bits D12:D11; refer to Table 9, page 20.

ADDRESS $A_1A_0$011—CURRENT DETECTION TIME AND OPEN LOAD REGISTER (CDTOLR)

The CDTOLR register is used by the MCU to determine the amount of time the device will allow an overcurrent low condition before an output latches OFF. Each output is independently selected for configuration based on A_1A_0, which are the state of the D12:D11 bits (refer to Table 9, page 20).

Bits D1:D0 (OCLT1_s:OCLT0_s) allow the MCU to select one of three overcurrent fault blanking times defined in Table 12. Note that these timeouts apply only to the overcurrent low detection levels. If the selected overcurrent high level is reached, the device will latch off within 20 µs.

Table 12. Overcurrent Low Detection Blanking Time

OCLT[1:0]_s*	Timing
00	155 ms
01	Do not use
10	75 ms
11	150 µs

* "_s" refers to the output, which is selected through bits D12:D11; refer to Table 9, page 20.

A logic [1] on bit D2 (OCL_DIS_s) disables the overcurrent low detection feature. When disabled, there is no timeout for the selected output and the overcurrent low detection feature is disabled.

A logic [1] on bit D3 (OL_DIS_s) disables the open load (OL) detection feature for the output corresponding to the state of bits D12:D11.

ADDRESS $A_1A_0$100—DIRECT INPUT CONTROL REGISTER (DICR)

The DICR register is used by the MCU to enable, disable, or configure the direct IN pin control of each output. Each output is independently selected for configuration based on the state bits D12:D11 (refer to Table 9, page 20).

For the selected output, a logic [0] on bit D1 (DIR_DIS_s) will enable the output for direct control. A logic [1] on bit D1 will disable the output from direct control.

While addressing this register, if the Input was enabled for direct control, a logic [1] for the D0 (A/O_s) bit will result in a Boolean AND of the IN pin with its corresponding IN_SPI D4:D0 message bit when addressing OCR0. Similarly, a logic [0] on the D0 pin results in a Boolean OR of the IN pin to the corresponding message bits when addressing the OCR0. This register is especially useful if several loads are required to be independently PWM controlled. For example, the IN pins of several devices can be configured to operate all of the outputs with one PWM output from the MCU. If each output is then configured to be Boolean ANDed to its respective IN pin, each output can be individually turned OFF by SPI while controlling all of the outputs, commanded on with the single PWM output.

A logic [1] on bit D2 (CSNS_high_s) is used to select the high ratio on the CSNS pin for the selected output. The default value [0] is used to select the low ratio (Table 13).

Table 13. Current Sense Ratio

CSNS_high_s* (D2)	Current Sense Ratio
	HS0:HS3
0	1/6500
1	1/20000

* "_s" refers to the output, which is selected through bits D12:D11; refer to Table 9, page 20.

A logic [1] on bit D3 (FAST_SR_s) is used to select the high speed slew rate for the selected output, the default value [0] corresponds to the low speed slew rate.

ADDRESS X0101—UNDERVOLTAGE/ OVERVOLTAGE REGISTER (UOVR)

The UOVR register disables the undervoltage (D1) and/or overvoltage (D0) protection. When these two bits are logic [0], the undervoltage and overvoltage are active (default value).

ADDRESS X1101— WATCHDOG REGISTER (WDR)

The WDR register is used by the MCU to configure the Watchdog timeout. The Watchdog timeout is configured using bits D1 and D0. When D1 and D0 bits are programmed for the desired watchdog timeout period (Table 14), the WDSPI bit should be toggled as well, ensuring the new timeout period is programmed at the beginning of a new count sequence.

Table 14. Watchdog Timeout

WD[1:0] (D1:D0)	Timing (ms)
00	620
01	310
10	2500
11	1250

ADDRESS XX110—NO ACTION REGISTER (NAR)

The NAR register can be used to no-operation fill SPI data packets in a daisy-chain SPI configuration. This would allow devices to be unaffected by commands being clocked over a daisy-chained SPI configuration. By toggling the WD bit (D15) the watchdog circuitry would continue to be reset while no programming or data read back functions are being requested from the device.

ADDRESS XX111—TEST

The TEST register is reserved for test and is not accessible with SPI during normal operation.

SERIAL OUTPUT COMMUNICATION (DEVICE STATUS RETURN DATA)

When the $\overline{CS}$ pin is pulled low, the output register is loaded. Meanwhile, the data is clocked out MSB- (OD15-) first as the new message data is clocked into the SI pin. The first 16 bits of data clocking out of the SO, and following a $\overline{CS}$ transition, is dependent upon the previously written SPI word.

Any bits clocked out of the SO pin after the first 16 bits will be representative of the initial message bits clocked into the SI pin since the $\overline{CS}$ pin first transitioned to logic [0]. This feature is useful for daisy chaining devices as well as message verification.

A valid message length is determined following a $\overline{CS}$ transition of logic [0] to logic [1]. If there is a valid message length, the data is latched into the appropriate registers. A valid message length is a multiple of 16 bits. At this time, the SO pin is tri-stated and the fault status register is now able to accept new fault status information.

SO data will represent information ranging from fault status to register contents, user selected by writing to the STATR bits OD4, OD3, OD2, OD1, and OD0. The value of the previous bits SOA4 and SOA3 will determine which output the SO information applies to for the registers which are output specific; viz., Fault, SOCHLR, CDTOLR, and DICR registers.

Note that the SO data will continue to reflect the information for each output (depending on the previous OD4, OD3 state) that was selected during the most recent STATR write until changed with an updated STATR write.

The output status register correctly reflects the status of the STATR-selected register data at the time that the $\overline{CS}$ is pulled to a logic [0] during SPI communication, and/or for the period of time since the last valid SPI communication, with the following exceptions:

- The previous SPI communication was determined to be invalid. In this case, the status will be reported as though the invalid SPI communication never occurred.
- Battery transients below 6.0 V resulting in an under-voltage shutdown of the outputs may result in incorrect data loaded into the Status register. The SO data transmitted to the MCU during the first SPI communication following an undervoltage V_{PWR} condition should be ignored.
- The $\overline{RST}$ pin transition from a logic [0] to logic [1] while the WAKE pin is at logic [0] may result in incorrect data loaded into the Status register. The SO data transmitted to the MCU during the first SPI communication following this condition should be ignored.

SERIAL OUTPUT BIT ASSIGNMENT

The 16 bits of serial output data depend on the previous serial input message, as explained in the following paragraphs. Table 15, page 23, summarizes SO returned data for bits OD15:OD0.

- Bit OD15 is the MSB; it reflects the state of the Watchdog bit from the previously clocked-in message.
- Bit OD14 remains logic [0] except when an undervoltage condition occurred.
- Bit OD13 remains logic [0] except when an overvoltage condition occurred.
- Bits OD12:OD8 reflect the state of the bits SOA4:SOA0 from the previously clocked in message.
- Bits OD7:OD4 give the fault status flag of the outputs HS3:HS0, respectively.
- The contents of bits OD3:OD0 depend on bits D4:D0 from the most recent STATR command SOA4:SOA0 as explained in the paragraphs following Table 15.

Table 15. Serial Output Bit Map Description

Previous STATR					SO Returned Data														
SO A4	SO A3	SO A2	SO A1	SO A0	OD 15	OD 14	OD 13	OD 12	OD 11	OD 10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
A_1	A_0	0	0	0	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	OTF_s	OCHF_s	OCLF_s	OLF_s
x	0	0	0	1	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	IN3_SPI	IN2_SPI	IN1_SPI	IN0_SPI
x	1	0	0	1	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	CSNS3 $\overline{EN}$	CSNS2 $\overline{EN}$	CSNS1 $\overline{EN}$	CSNS0 $\overline{EN}$
A_1	A_0	0	1	0	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	SOCH_s	SOCL2_s	SOCL1_s	SOCL0_s
A_1	A_0	0	1	1	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	OL_DIS_s	OCL_DIS_s	OCLT1_s	OCLT0_s
A_1	A_0	1	0	0	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	Fast_SR_s	CSNS_high_s	DIR_DIS_s	A/O_s
x	0	1	0	1	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	–	–	UV_DIS	OV_DIS
x	1	1	0	1	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	–	WDTO	WD1	WD0
x	0	1	1	0	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	HS2_failsaf	HS0_failsaf	WD_en	WAKE
x	1	1	1	0	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	IN3	IN2	IN1	IN0

x=Don't care.
s=Output selection with the bits A_1A_0 as defined in Table 9, page 20.

PREVIOUS ADDRESS SOA4:SOA0=$A_1A_0$000

Bits OD3:OD0 reflect the current state of the Fault register (FLTR) corresponding to the output previously selected with the bits A_1A_0 (Table 16).

Table 16. Output-Specific Fault Register

OD3	OD2	OD1	OD0
OTF_s	OCHF_s	OCLF_s	OLF_s

s=Selection of the output.

Note The $\overline{FS}$ pin reports all faults. For latched faults, this pin is reset by a new Switch ON command (via SPI or direct input IN).

PREVIOUS ADDRESS SOA4:SOA0=X0001

Data in bits OD3:OD0 contains IN3_SPI:IN0_SPI programmed bits for outputs HS3:HS0, respectively.

PREVIOUS ADDRESS SOA4:SOA0=X1001

Data in bits OD3:OD0 contains the programmed CSNS3 $\overline{EN}$:CSNS0 $\overline{EN}$ bits for outputs HS3:HS0, respectively.

PREVIOUS ADDRESS SOA4:SOA0=$A_1A_0$010

Data returned in bits OD3:OD0 are programmed current values for the overcurrent high detection level (refer to Table 11, page 21) and the overcurrent low detection level (refer to Table 10, page 21), corresponding to the output previously selected with A_1A_0.

PREVIOUS ADDRESS SOA4:SOA0=$A_1A_0$011

The returned data contains the programmed values in the CDTOLR register for the output selected with A_1A_0.

PREVIOUS ADDRESS SOA4:SOA0=$A_1A_0$100

The returned data contains the programmed values in the DICR register for the output selected with A_1A_0.

PREVIOUS ADDRESS SOA4:SOA0=X0101

The returned data contains the programmed values in the UOVR register.

PREVIOUS ADDRESS SOA4:SOA0=X1101

The returned data contains the programmed values in the WDR register. Bit OD2 (WDTO) reflects the status of the watchdog circuitry. If WDTO bit is logic [1], the watchdog has timed out and the device is in Fail-Safe mode. IF WDTO is logic [0], the device is in Normal mode (assuming the device is powered and not in the Sleep mode), with the watchdog either enabled or disabled.

PREVIOUS ADDRESS SOA4:SOA0=X0110

The returned data OD3 and OD2 contain the state of the outputs HS2 and HS0, respectively, in case of Fail-Safe state. This information is stated with the external resistance placed at the FSI pin. OD1 indicates if the watchdog is enabled or not. OD0 returns the state of the WAKE pin.

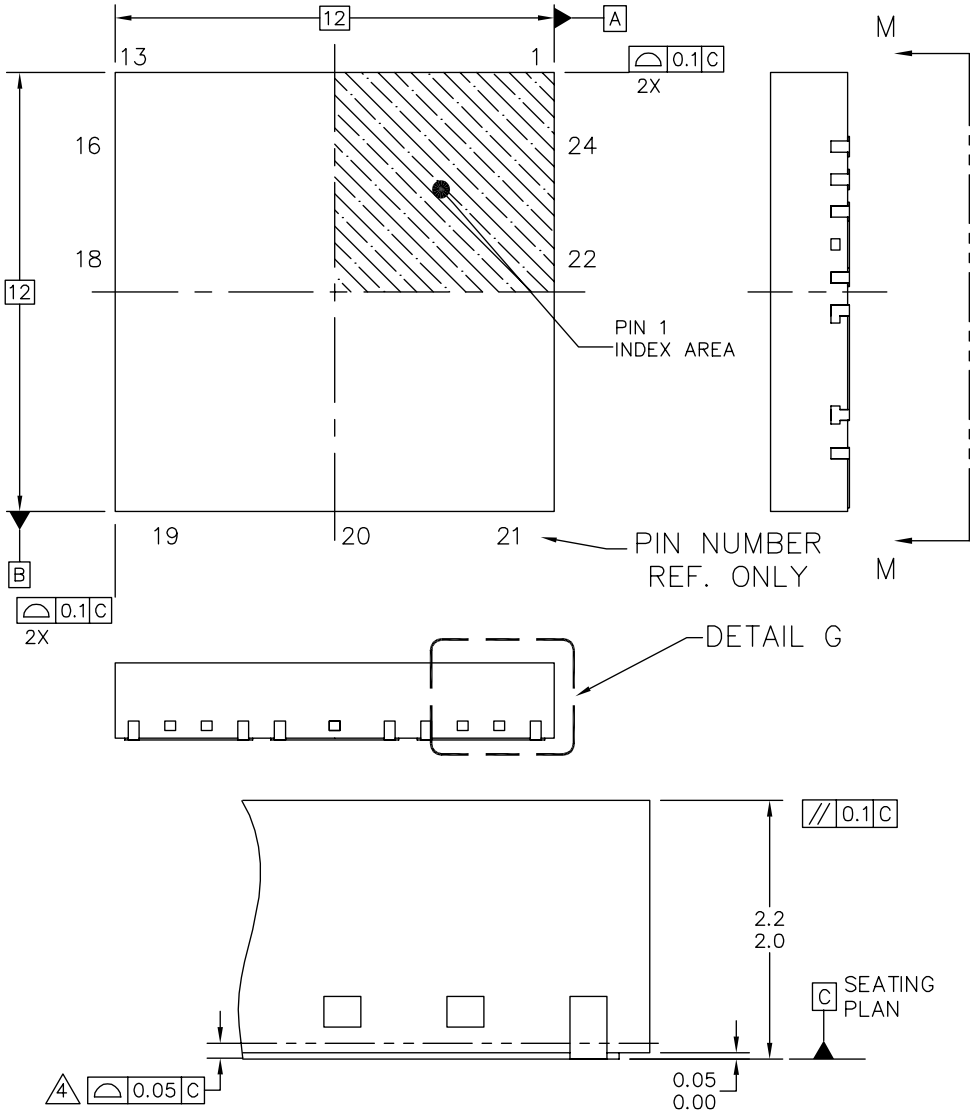
PREVIOUS ADDRESS SOA4:SOA0=X1110

The returned data OD3:OD0 reflects the state of the direct pins IN3:IN0, respectively.

PACKAGING

PACKAGE DIMENSIONS

For the most current revision of the package, visit **www.freescale.com** and perform a keyword search using the ”98A” drawing number listed below.

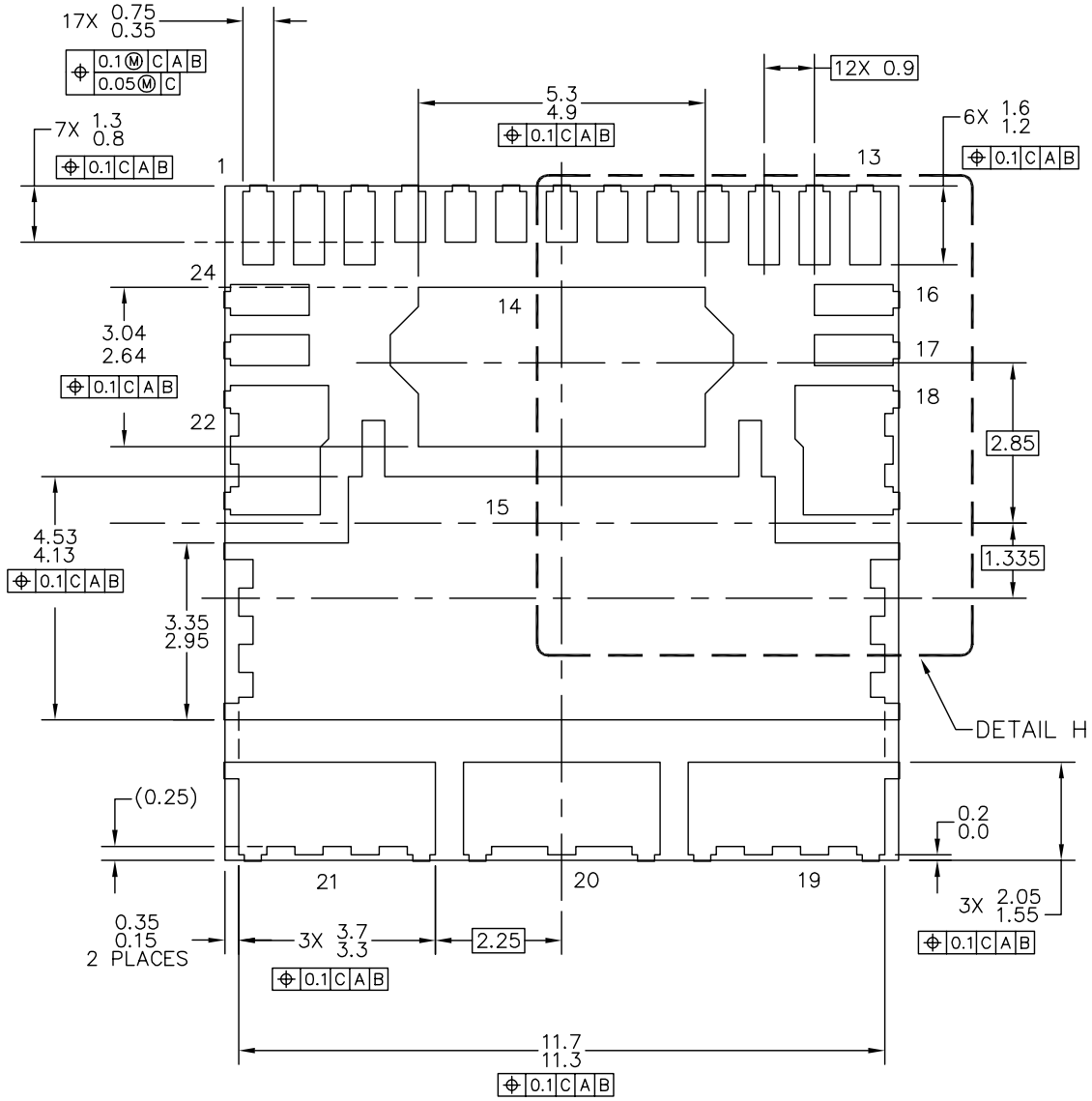


DETAIL G

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN) 24 TERMINAL, 0.9 PITCH(12X12X2.1)	DOCUMENT NO: 98ARL10596D	REV: C
	CASE NUMBER: 1593–03	13 OCT 2005
	STANDARD: NON–JEDEC	

PNA SUFFIX
24-PIN PQFN
NON-LEADED PACKAGE
98ARL10596D
ISSUE C

33894

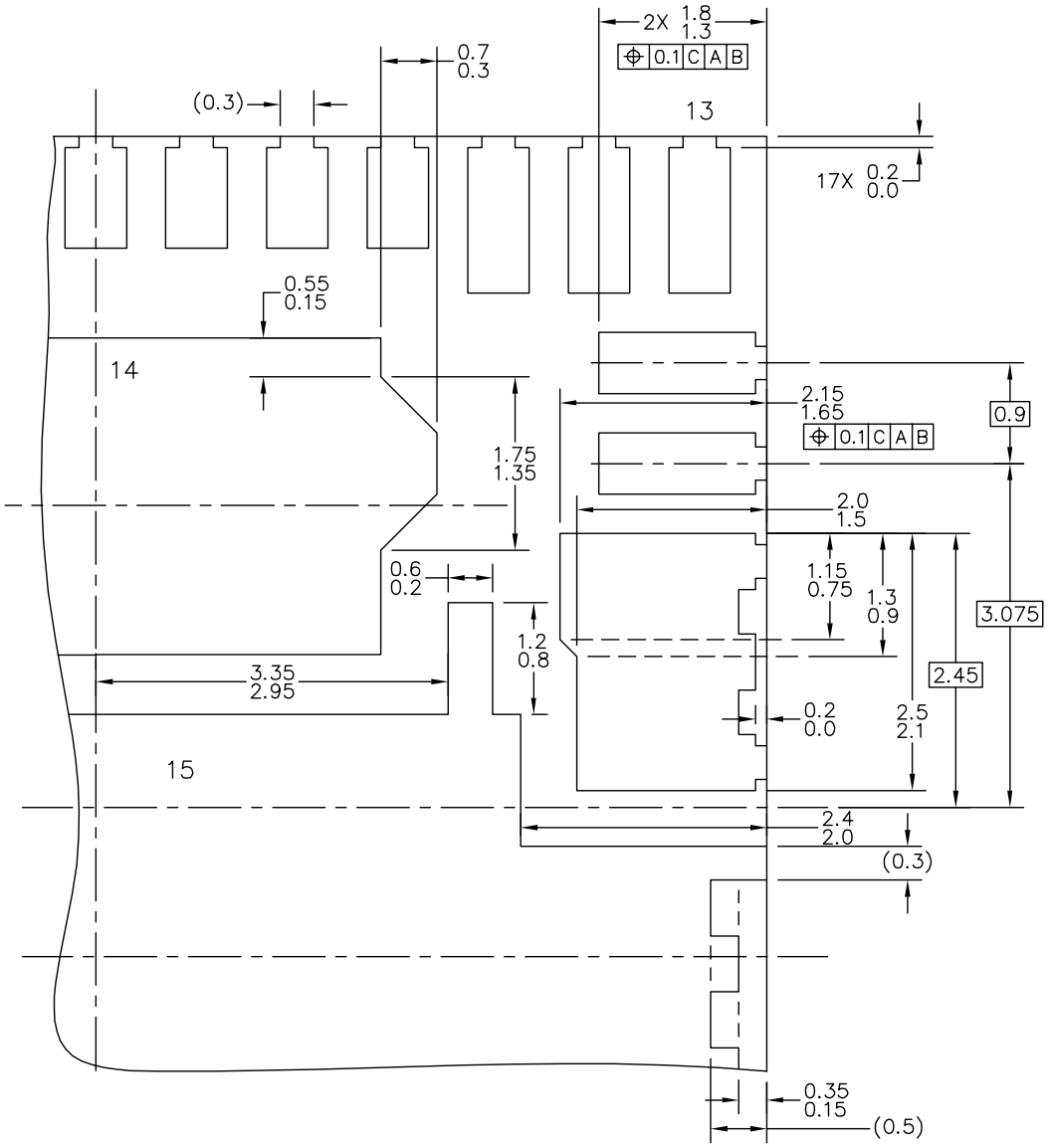


VIEW M–M

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN) 24 TERMINAL, 0.9 PITCH(12X12X2.1)	DOCUMENT NO: 98ARL10596D	REV: C
	CASE NUMBER: 1593–03	13 OCT 2005
	STANDARD: NON–JEDEC	

PNA SUFFIX
24-PIN PQFN
NON-LEADED PACKAGE
98ARL10596D
ISSUE C

33894



DETAIL H

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN) 24 TERMINAL, 0.9 PITCH(12X12X2.1)	DOCUMENT NO: 98ARL10596D	REV: C
	CASE NUMBER: 1593–03	13 OCT 2005
	STANDARD: NON–JEDEC	

PNA SUFFIX
24-PIN PQFN
NON-LEADED PACKAGE
98ARL10596D
ISSUE C

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	10/2006	• Implemented Revision History page • Converted to Freescale format and updated with the prevailing form and style • Updated to the current package drawing 98ARL10596D, REV C

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to http://www.freescale.com/epp.

MC33894
Rev 3.0
10/2006

freescale™ semiconductor