29C300/301

T1/E1 Integrated Short Haul Transceivers with Receive Jitter Attenuation

Description

The 29C300 and 29C301 are fully integrated transceivers for both North American 1.544 MHz (T1), and European 2.048 MHz (E1/CEPT) applications. Transmit pulse shapes (DSX-1 or E1/CEPT) are selectable for various line lengths and cable types.

The 29C300 provides receive jitter attenuation starting at 6 Hz, and is microprocessor controllable through a serial interface. The 29C301 is pin compatible, but does not provide jitter attenuation or a serial interface.

Both transceivers offer a variety of diagnotic features including transmit and receive monitoring. Clock inputs may be derived from an on-chip crystal oscillator or digital inputs. They use an advanced double-poly, double-metal CMOS process and each requires only a single 5-volt power supply.

The MHS 29C300 and 29C301 find applications in widely diverse areas of telecommunication, including :

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Ditigal Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

Features

- Compatible with most popular PCM framers including MHS 29C96
- Line driver, data recovery and clock recovery functions
- Receive jitter attenuation starting at 6 Hz meets or exceeds AT&T PUB 62411 (29C300 only)
- 29C300 and 29C301 are pin compatible, and offer pin and functional compatibility with crystal CS61574 (29C300) and crystal CS6158 (29C301)
- Minimum receive signal of 500 mV
- Selectable slicer levels (CEPT/DSX-1) improve SNR
- Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 FT
- Local and remote loopback functions
- Transmit driver performance monitor (DPM) output
- Receive monitor with loss of signal (LOS) output
- Receiver jitter tolerance 0.4 UI from 40 KHz to 100 KHz
- Microprocessor controllable (29C300 only)
- Available in 28 pin DIP or PLCC

Figure 1. 29C300 Block Diagram.

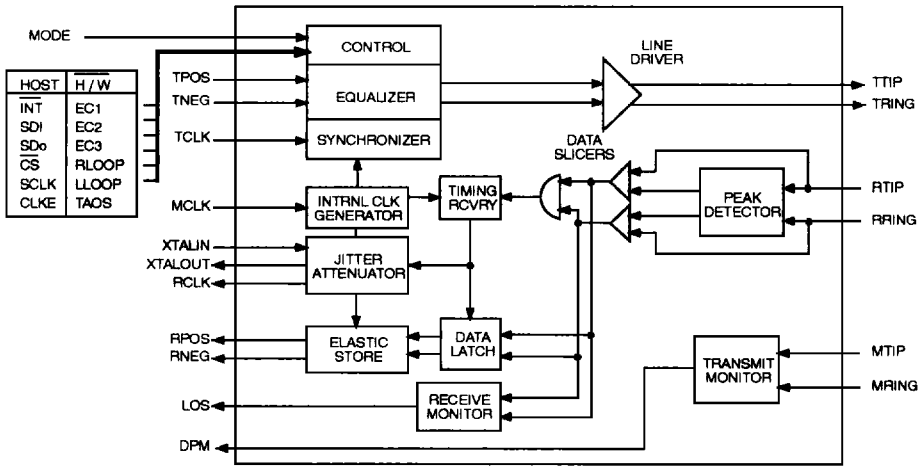
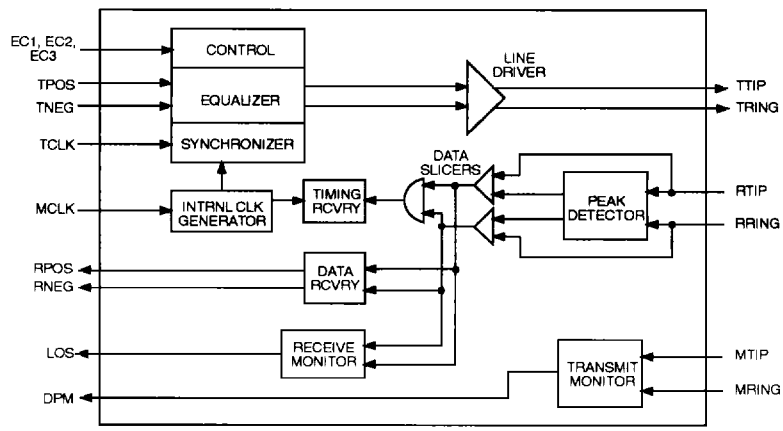
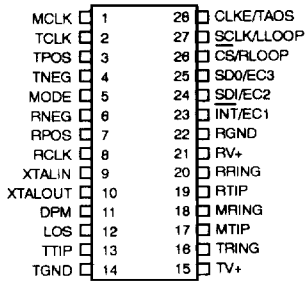


Figure 2. 29C301 Block Diagram.

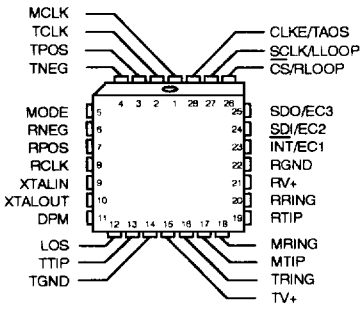


Interface

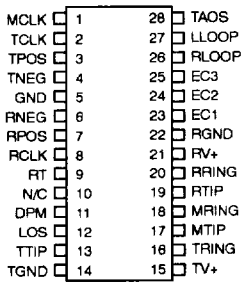
Pin Configuration



29C300 (DIP)



29C300 (PLCC)



29C301 (DIP)

Pin Description

Table 1.

Symbol	Pin #	I/O	Name	Description
MCLK	1	I	Master Clock	A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. *29C300 Only : If MCLK not applied, this pin should be grounded.*
TCLK	2	I	Transmit Clock	Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
TPOS	3	I	Transmit Positive Data	Input for positive pulse to be transmitted on the twisted-pair line.
TNEG	4	I	Transmit Negative Data	Input for negative pulse to be transmitted on the twisted-pair line.
MODE	5	I	Mode Select (29C300)	Setting MODE to logic 1 puts the 29C300 in the Host mode. In the Host mode, the serial interface is used to control the 29C300 and determine its status. Setting MODE to logic 0 puts the 29C300 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
GND		–	(29C301)	Tie to Ground.
RNEG	6	O	Receive Negative Data	Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valide on the rising edge of RCLK. *29C300 only : In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge of RCLK.*
RPOS	7	O	Receive Positive Data	
RCLK	8	O	Recovered Clock	This is the clock recovered from the signal received at RTIP and RRING.

Table 1. (continued)

Symbol	Pin #	I/O	Name	Description
RT	9	–	Resistor Termination (29C301)	Connect to RV through a 1 kΩ resistor.
XTALIN	9	I	Crystal Input (29C300)	An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7 pF load) is required to enable the jitter attenuation function of the 29C300. These pins may also used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
XTALOUT	10	O	Crystal Output (29C300)	
N/C	10	–	(29C301)	No connection
DPM	11	O	Driver Performance Monitor	DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ± 2 clock periods. DPM remains at logic 1 until a signal is detected.
LOS	12	O	Loss Of Signal	LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when a mark is detected.
TTIP	13	O	Transmit Tip	Differential Driver Outputs. These outputs are designed to drive a 25 Ω load. The transmitter will drive 100 Ω shielded twisted-pair cable through a 2:1 step−up transformer without additional components. To drive 75 Ω coaxial cable, two 2.2 Ω resistors are required in series with the transformer.
TRING	16	O	Transmit Ring	
TGND	14	–	Transmit Ground	Ground return for the transmit drivers power supply TV+.
TV+	15	I	Transmit Power Supply	+5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ± 0.3 V.
MTIP	17	I	Monitor Tip	These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another 29C300 or 301 on the board. *29C300 only : To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid−level voltage. The monitor clock can range from 100 kHz to the TCLK frequency.*
MRING	18	I	Monitor Ring	
RTIP	19	I	Receive Tip	The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
RRING	20	I	Receive Ring	
RV+	21	I	Receive Power Supply	+5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
RGND	22	–	Receive Ground	Ground return for power supply RV+.
$\overline{INT}$	23	O	Interrupt *(Host Mode)*	This 29C300 Host mode output goes low to flag the host processor when LOS or DPM go active. $\overline{INT}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{INT}$ is reset by clearing the respective register bit (LOS and/or DPM.)
EC1		I	Equalizer Control 1 *(H/W Mode)*	The signal applied at this pin in the 29C300. Hardware mode and 29C301 is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
SDI	24	I	Serial Data In *(Host Mode)*	The serial data input stream is applied to this pin when the operates in the *Host mode*. SDI is sampled on the rising edge of SCLK.
EC2		I	Equalizer Control 2 *(H/W Mode)*	The signal applied at this pin in the 29C300 *Hardware mode and* 29C301 is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.

Table 1. (continued)

Symbol	Pin #	I/O	Name	Description
SDO	25	O	Serial Data Out *(Host Mode)*	The serial data from the on-chip register is output on this pin in the 29C300 *Host mode*. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the failing edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
EC3		I	Equalizer Control 3 *(H/W Mode)*	The signal applied at this pin in the 29C300 *Hardware mode and* 29C301 is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
$\overline{CS}$	26	I	Chip Select *(Host Mode)*	This input is used to access the serial interface in 29C300 *Host mode*. For each read or write operation, $\overline{CS}$ must transition from high to low, and remain low.
RLOOP		I	Remote Loopback *(H/W Mode)*	This input controls loopback functions in the 29C300 *Hardware mode and* 29C301. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset.
SCLK	27	I	Serial Clock *(Host Mode)*	This clock is used in the 29C300 *Host mode* to write data to or read data from the serial interface registers.
LLOOP		I	Local Loopback *(H/W Mode)*	This input controls loopback functions in the 29C300 *Hardware mode and* 29C301. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
CLKE	28	I	Clock Edge *(Host Mode)*	Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
TAOS		I	Transmit All Ones *(H/W Mode)*	When set to a logic 1, TAOS causes the 29C300 *(Hardware mode) and* 29C301 to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

2

Functional Description

The 29C300 and 301 are fully integrated PCM transceivers for both 1.544 MHz (DSX-1) and 2.048 MHz (CEPT) applications. Both transceivers allow full-duplex transmission of digital data over existing twisted-pair installations. Figure 1 is a simplified block diagram of the 29C300. The 29C301 is shown in Figure 2. The 29C301 is similar to the 29C300 but does not incorporate the Jitter Attenuator and associated Elastic Store, or the serial interface port.

The 29C300 and 301 transceivers each interface with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

Transmitter

The transmitter circuits in the 29C300 and 301 are identical. The following discussion applies to both models. Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 2. Refer to Table 3 and Figure 3 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals are hard-wired to the 29C301.

29C300 Only: Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The 29C300 and 301 also match FCC and ECSA specifications for CSU applications. 2.048 MHz pulses can drive coaxial or shielded twisted-pair lines using appropriate resistors in line with the output transformer.

Table 2 : Equalizer Control Inputs.

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Frequency
0	1	1	0 – 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 – 266 ft ABAM	1.2 dB		
1	0	1	266 – 399 ft ABAM	1.8 dB		
1	1	0	399 – 533 ft ABAM	2.4 dB		
1	1	1	533 – 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		CEPT	2.048 MHz
0	1	0	FCC Part 68, Option A		CSU	1.544 MHz
0	1	1	ECSA T1C1.2			

Notes : 1.Line length from transceiver to DSX-1 cross-connect point.
2.Maximum cable loss at 772 kHz.

Driver Performance Monitor

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with the TTIP and TRING at the output transformer. The DPM output level goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

Line Code

The 29C300 and 301 transmit data as a 50 % AMI line code as shown in Figure 4. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled transmission of a space.

Table 3 : 29C300 and 301 Master Clock and Transmit Timing Characteristics (see figure 3)

Symbol	Parameter		Min	Typ[1]	Max	Units
MCLK	Master clock frequency	DSX-1	–	1.544	–	MHz
MCLK		CEPT	–	2.048	–	MHz
MCLKt	Master clock tolerance		–	± 100	–	ppm
MCLKd	Master clock duty cycle		40	–	60	%
fc	Crystal frequency 29C300 only	DSX-1	–	6.176	–	MHz
fc		CEPT	–	8.192	–	MHz
TCLK	Transmit clock frequency	DSX-1	–	1.544	–	MHz
TCLK		CEPT	–	2.048	–	MHz
TCLKt	Transmit clock tolerance		–	–	± 50	ppm
TCLKd	Transmit clock duty cycle		10	–	90	%
t_{SUT}	TPOS/TNEG to TCLK setup time		25	–	–	ns
t_{HT}	TCLK to TPOS/TNEG Hold time		25	–	–	ns

Note : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.

Figure 3. 29C300 and 301 Transmit Clock Timing Diagram.

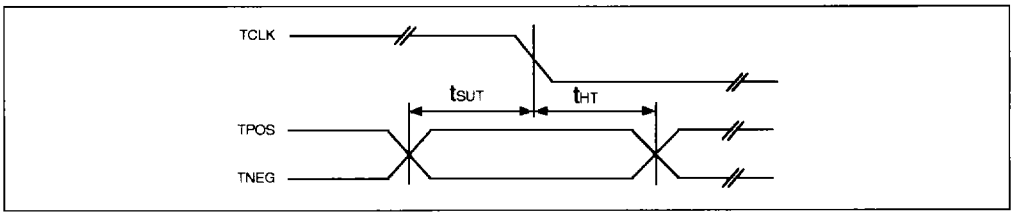
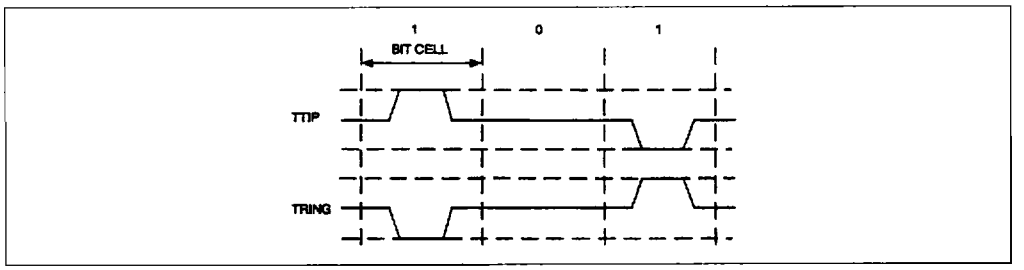


Figure 4. 50 % AMI Coding Diagram.



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Receiver

The 29C300 and 29C301 receivers are identical except for the jitter attenuator and elastic store. The following discussion applies to both transceivers except where noted.

The signal is received from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 4 and Figure 5 for 29C300 receiver timing. 29C301 receiver timing is shown in Table 5 and Figure 6.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000) the threshold is set to 70 % of the peak value. This threshold is maintained above 65 % for up to 15 successive zeros over the range of specified operating conditions. For CEPT applications (EC inputs = 000) the threshold is set to 50 %.

The receiver is capable of accurately recovering signals with up to - 13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB). Regardless of received signal level, the peak detectors are held above a mimimum level of .3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and the RCLK output is replaced with the MCLK.

(In the 29C300 only, if MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.)

The LOS pin will reset as soon as a one (mark) is received.

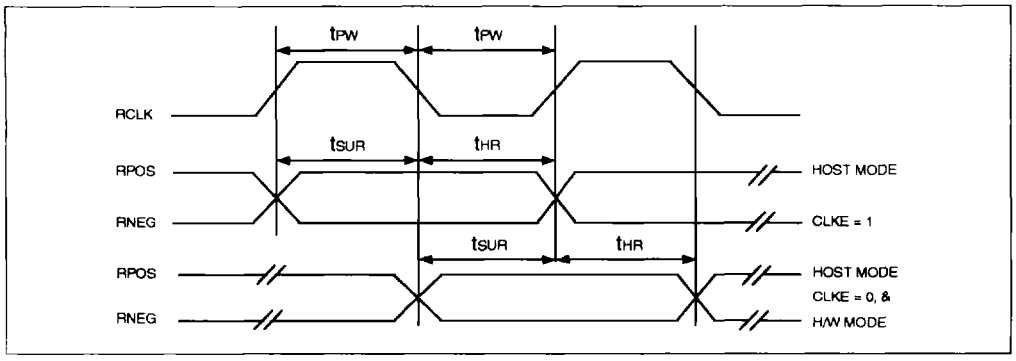
In the 29C300 only, recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK).

Table 4 : 29C300 Receive Timing Characteristics (See Figure 5).

Symbol	Parameter		Min	Typ[1]	Max	Units
RCLKd	Receive clock duty cycle		40	-	60	%
t_{PW}	Receive clock pulse width	DSX-1	-	344	-	ns
t_{PW}		CEPT	-	244	-	ns
t_{SUR}	RPOS / RNEG to RCLK	DSX-1	-	274	-	ns
t_{SUR}	rising setup time	CEPT	-	194	-	ns
t_{HR}	RCLK rising to RPOS /	DSX-1	-	274	-	ns
t_{HR}	RNEG hold time	CEPT	-	194	-	ns

Note : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.

Figure 5. 29C301 Receive Clock Timing Diagram.



Jitter Attenuation (29C300 only)

Jitter attenuation of the 29C300 clock and data outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clook stabilization. Refer to Table 6 for crystal specifications. The ES is a 32 x 2-bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 a bit period. The ES produces an average delay of 16 bits in the receive path.

Operating Modes

The 29C300 and 301 transceivers can be controlled through hard-wired pins (Hardware mode). Both transceivers can also be commanded to operate in one of several diagnostic modes.

29C300 Only: The 29C300 can be controlled by a micro-processor through a serial interface (Host mode). The mode of operation is set by the MODE pin logic level.

Host Mode Operation (29C300 only)

To allow a host microprocessor to access and control the 29C300 through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 7 shows the serial interface data structure and timing.

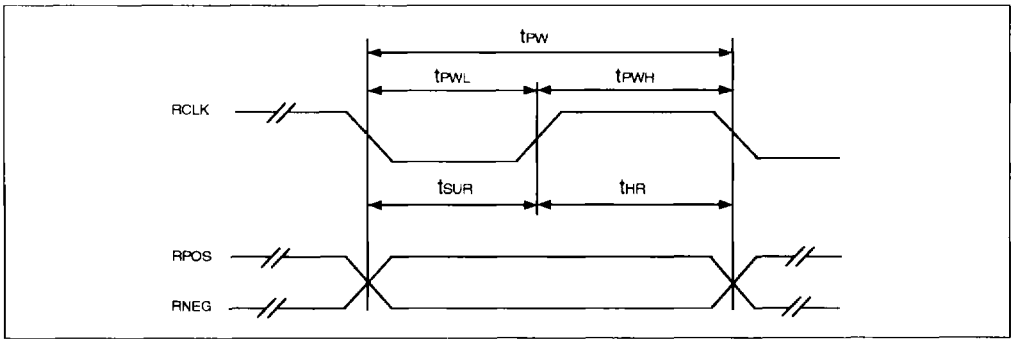
The Host mode provides a latched Interrupt output ($\overline{INT}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte.

Table 5 : 29C301 receive Timing Characteristics (See Figure 6).

Symbol	Parameter		Min	Typ[1]	Max	Units
RCLKd	Receive clock duty cycle[2]	DSX-1	40	50	60	%
RCLKd		CEPT	40	50	60	%
t_{PW}	Receive clock pulse width[2]	DSX-1	594	648	702	ns
t_{PW}		CEPT	447	488	529	ns
t_{PWH}	Receive clock pulse width high	DSX-1	–	324	–	ns
t_{PWH}		CEPT	–	244	–	ns
t_{PWL}	Receive clock pulse width low	DSX-1	270	324	378	ns
t_{PWL}		CEPT	203	244	285	ns
t_{SUR}	RPOS / RNEG to RCLK rising setup time	DSX-1	50	270	–	ns
t_{SUR}		CEPT	50	203	–	ns
t_{HR}	RCLK rising to RPOS / RNEG hold time	DSX-1	50	270	–	ns
t_{HR}		CEPT	50	203	–	ns

Notes : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.544 MHz, 0.2 UI clock displacement for 2.048 MHz.)

Figure 6. 29C301 receive Clock Timing Diagram.



Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows :

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The 29C300 serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The 29C300 contains only a single only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select ($\overline{CS}$) input to transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 7 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in Table 8, and Figures 8 and 9.

Hardware Mode Operation (29C300 and 301)

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{INT}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK. The 29C301 operates in Hardware mode at all times.

29C300 Only: To operate in Hardware mode, MODE must be set to 0. Equalizer Control Signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

Reset Operation (29C300 and 301)

Upon power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. MCLK provides the receiver reference for the 29C301. The crystal oscillator provides the receiver reference in the 29C300. If the 29C300 crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and centers the oscillator, then begins calibration.

Table 6 : 29C300 Crystal Specifications (External)

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	± 20 ppm @ 25 °C ± 25 ppm from – 40 ° C to + 85 °C (Ref 25 °C reading)	± 20 ppm @ 25 °C ± 25 ppm from – 40 °C to + 85 °C (Ref 25 °C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, – ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, – ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_o = 7 pF maximum C_M = 17 fF typical	HC49 (R3W), C_o = 7 pF maximum C_M = 17 fF typical

Table 7 : 29C300 Serial Data Output Bits (See Figure 7).

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

Figure 7. 29C300 Serial Interface Data Structure.

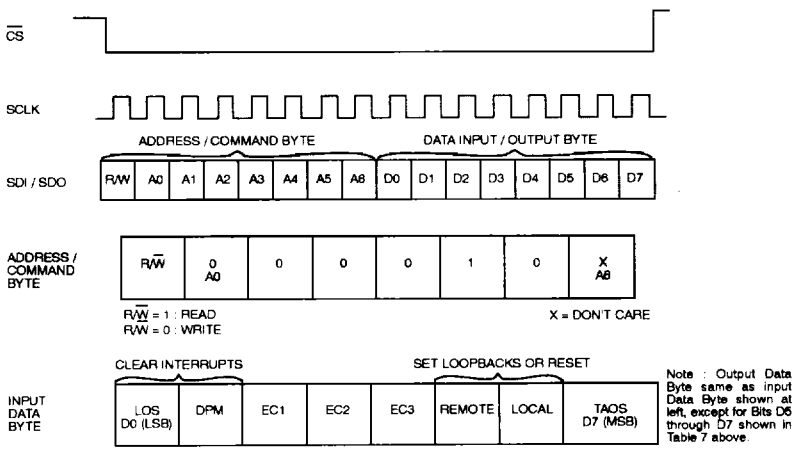


Table 8 : 29C300 Serial I/O Timing Characteristics (see Figures 8 and 9).

Sym	Parameter	Test Conditions	Min	Typ[1]	Max	Units
t_{RF}	Rise/Fall time – any digital output	Load 1.6 mA, 50 pF	–	–	100	ns
t_{DC}	SDI to SCLK setup time		50	–	–	ns
t_{CDH}	SCLK to SDI hold time		50	–	–	ns
t_{CL}	SCLK low time		240	–	–	ns
t_{CH}	SCLK high time		240	–	–	ns
t_R, t_F	SCLK rise and fall time		–	–	50	ns
t_{CC}	CS to SCLK setup time		50	–	–	ns
t_{CCH}	SCLK to CS hold time		50	–	–	ns
t_{CWH}	CS inactive time		250	–	–	ns
t_{CDV}	SCLK to SDO valid		–	–	200	ns
t_{CDZ}	SCLK falling edge or CS rising edge to SDO high Z		–	100	–	ns

Note : 1. Typical figures are at 25 °C and are for design aid only ; not guaranteed and not subject to production testing.

Figure 8. 29C300 Serial Data Input Timing Diagram.

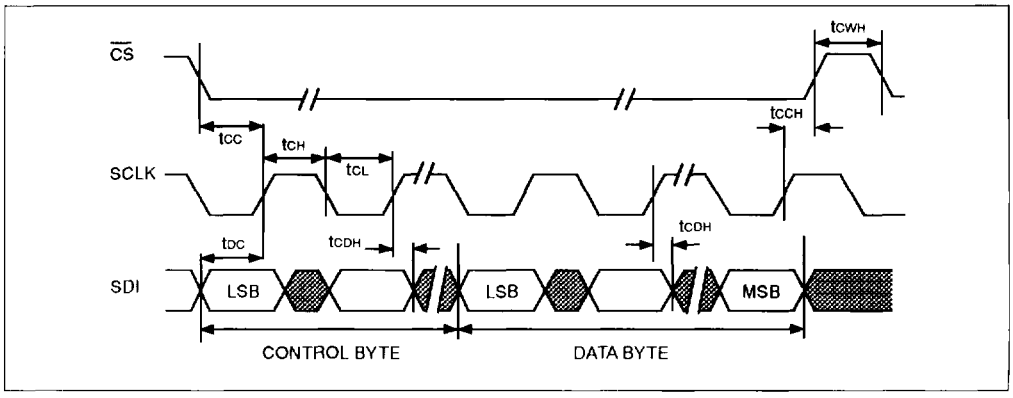
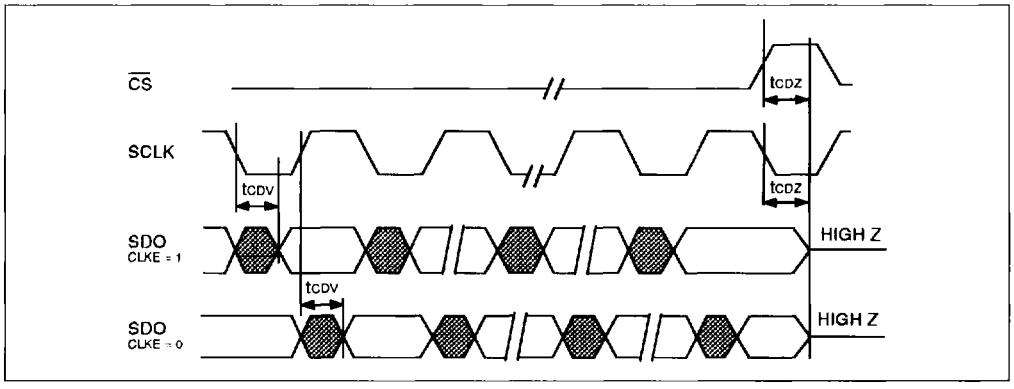


Figure 9. 29C300 Serial Data Output Timing Diagram.



Diagnostic Mode Operation

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair lines.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of 1's if the TAOS command is active) will be transmitted normally.

29C300 Only : When used in this mode with a crystal, the transceiver can be used as a stand-alone jitter attenuator.

Power Requirements

The 29C300 and 301 are low-power CMOS devices. Each operates from a single + 5 V power supply which

can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3 V of each other, and decoupled to their respective grounds separately, as shown in Figure 10. Isolation between the transmit and receive circuits is provided internally.

Applications

29C300 1.544 MHz T1 Interface Applications

Figure 10 is a typical 1.544 MHz T1 application. The 29C300 is shown in the Host mode with the 29C96 T1/ESF Framer providing the digital interface with the host controller. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68 µF and 0.1 µF on the receive side.)

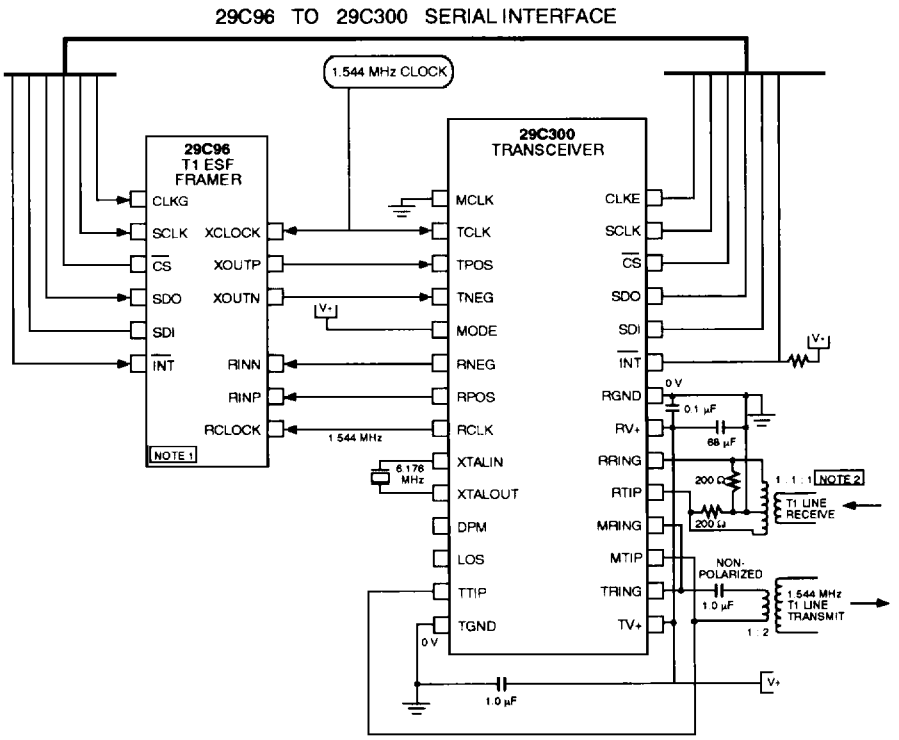
29C300 2.048 MHz E1/CEPT Interface Applications

Figure 11 is a typical 2.048 MHz E1/CEPT application. The 29C300 is shown in Hardware mode with the 29C96

E1/CRCA Framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 100 Ω shielded twisted-pair lines. As in the T1 application Figure 10, this configuration is illustrated with a crystal in place to enable the 29C300 Jitter Attenuation Loop, and a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.

2

Figure 10. Typical 29C300 1.544 MHz T1 Application (Host Mode).



Notes : 1. In addition to the 29C96 the 29C300 is compatible with a wide variety of digital framing and signaling devices.
2. When 29C300 is connected to the cross-connect frame through a low level monitor jack, receive transformer should be 1 : 2 : 2 to boost the input signal.

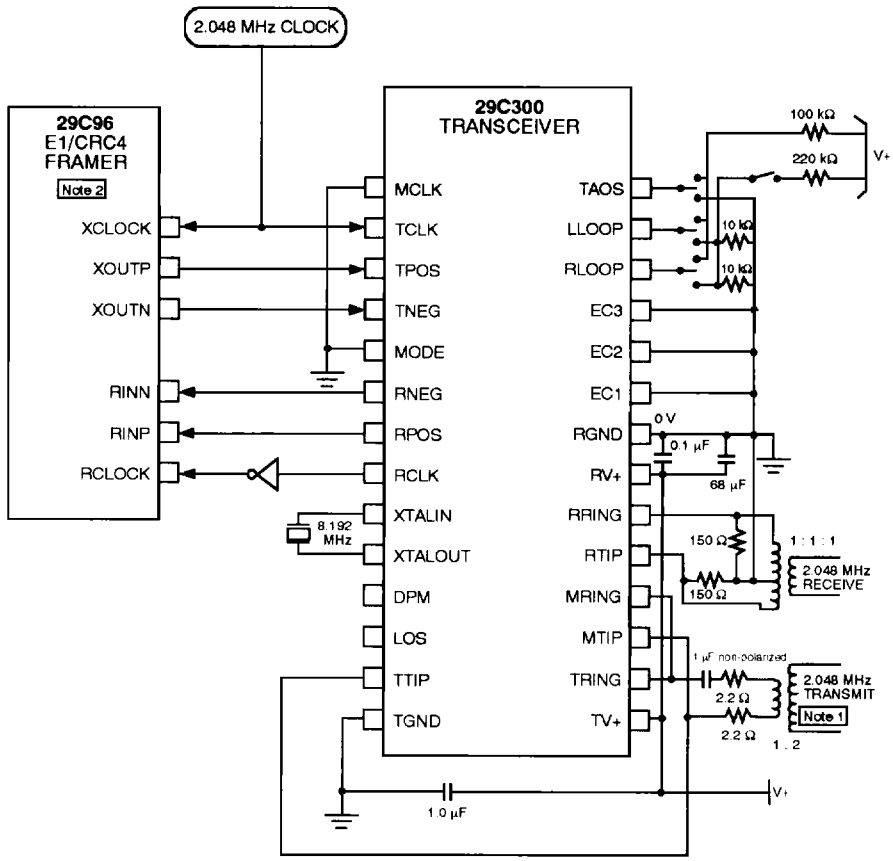
29C301 1.544 MHz T1 Interface

Figure 12 is a typical 1.544 MHz T1 application of the 29C301. The 29C301 is shown with the 29C96 T1/ESF Framer. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68 µF and 0.1 µF on the receive side.)

29C301 2.048 MHz CEPT Interface

Figure 13 is a typical 2.048 MHz CEPT application of the 29C301. The 29C301 is shown with the 29C96 E1/CRC4 Framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 100 Ω shielded twisted-pair lines. As in the T1 application Figure 12, this configuration is illustrated with a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.

Figure 11. Typical 29C300 2.048 MHz E1 Application (Hardware Mode).



Notes : 1. 2.2 Ω resistors required only for 75 Ω coaxial cable. Not required for transmission onto 100 Ω cable.
2. In addition to the 29C96 the 29C300 is compatible with a wide variety of digital framing and signaling devices.

Figure 12. Typical 29C301 1.544 MHz T1 Application.

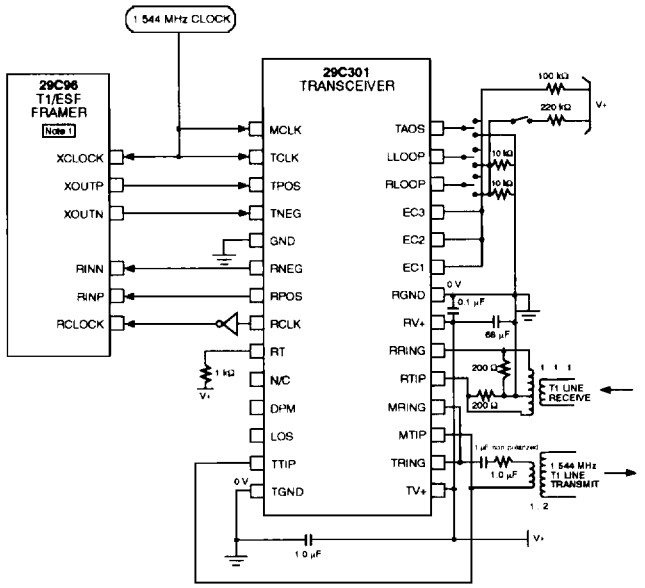
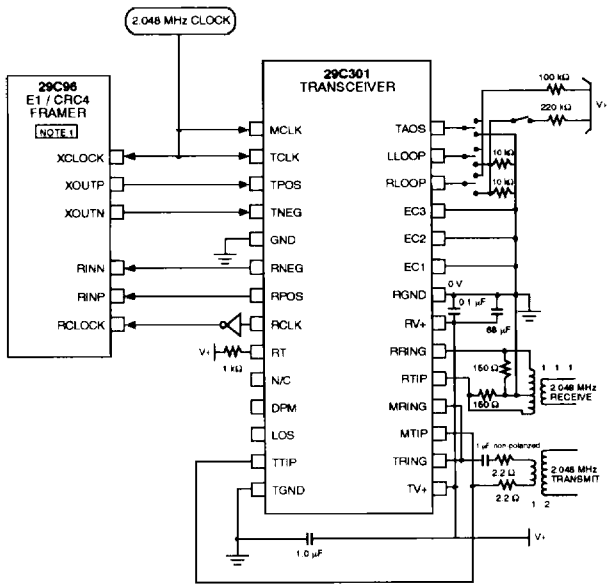


Figure 13. Typical 29C301 2.048 MHz T1 Application.



Note : 1. In addition to the 29C96, the 29C301 is compatible with a wide variety of digital framing and signaling devices.

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
RV+, TV+	DC supply (referenced to GND)	–	6.0	V
V_{IN}	Input voltage, any pin[1]	RGND – 0.3	RV+ + 0.3	V
I_{IN}	Input current, any pin[2]	– 10	10	mA
T_A	Ambient operating temperature	– 40	85	°C
T_{STG}	Storage temperature	– 65	150	°C

WARNING : Operations at or beyond these limits may result in permanent damage to the device. Normal operation not guaranteed at these extremes.

Notes : 1. Excluding RTIP and RRING which must stay within −6 V to RV + 0.3 V.
2. Transient current of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
RV+, TV+	DC supply[3]		4.75	5.0	5.25	V
T_A	Ambient operating temperature		– 40	25	85	°C
P_D	Total power dissipation	100 % ones density & maximum line lenght @ 5.25 V	–	620	–	mW

Notes : 3. TV+ must not exceed RV+ by more than 0.3 V.
4. Power dissipation while driving 25 Ω load over operating range. Includes device and load. Digital input levels are within 10 % of the supply rails and digital outputs are driving a 50 pF capacitive load.

Digital Characteristics (T_A = −40° to 85°C, V+ = 5.0 V ± 5 %, GND = 0 V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High level input voltage [5, 6] (pins 1-5, 10, 23-28)		2.0	–	–	V
V_{IL}	Low level input voltage [5, 6] (pins 1-5, 10, 23-28)		–	–	0.8	V
V_{OH}	High level output voltage [5, 6] (pins 6-8, 11, 12, 23, 25)	I_{OUT} = – 400 µA	2.4	–	–	V
V_{OL}	Low level output voltage [5, 6] (pins 6-8, 11, 12, 23, 25)	I_{OUT} = 1.6 mA	–	–	0.4	V
I_{LL}	Input leakage current		– 10	–	+ 10	µA
I_{3L}	Three-state leakage current[5] (pin 25)		– 10	–	+ 10	µA

Notes : 5. Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.
6. Output drivers will output CMOS logic levles into CMOS loads.

Analog Specifications (T_A = −40° to 85°C, V+ = 5.0 V ± 5 %, GND = 0 V)

Parameter		Test Conditions	Min	Typ	Max	Units
AMI Output Pulse Amplitudes	DSX−1	measured at the DSX	2.4	3.0	3.6	V
	CEPT	measured at line side	2.7	3.0	3.3	V
Recommended Output Load at TTIP and TRING			–	25	–	Ω
Jitter added by the transmitter[7]	10 Hz – 8 kHz		–	–	0.01	UI
	8 kHz – 40 kHz		–	–	0.025	UI
	10 Hz – 40 kHz		–	–	0.025	UI
	Broad Band		–	–	0.05	UI
Sensitivity below DSX	(0dB = 2.4 V)		13.6	–	–	dB
			500	–	–	mV
Loss of Signal threshold			–	0.3	–	V
Data decision threshold	DSX-1		–	65	–	% peak
	CEPT		–	50	–	% peak
Allowable consecutive zeros before LOS			160	175	190	–
Input jitter tolerance 10 kHz – 100 kHz			0.4	–	–	UI
Jitter attenuation curve corner frequency[8]			–	6	–	Hz

Notes : 7. Input signal to TCLK is jitter-free.
8. Circuit attenuates jitter at 20 dB/decade above the corner frequency.

2

Ordering Information