LM4981

LM4981 Ground-Referenced, 80mW Stereo Headphone Amplifier with Up/Down Volume Control

Literature Number: SNAS313G

National Semiconductor

LM4981

Boomer® Audio Power Amplifier Series

OBSOLETE
October 4, 2011

Ground-Referenced, 80mW Stereo Headphone Amplifier with Up/Down Volume Control

General Description

The LM4981 is a stereo, ground-referenced, output capacitor-less headphone amplifier capable of delivering 83mW of continuous average power into a 16Ω load with less than 1% THD+N while operating from a single 3V supply.

The LM4981 features a new circuit technology that utilizes a charge pump to generate a negative reference voltage. This allows the outputs to be biased about ground, thereby eliminating output-coupling capacitors typically used with normal single-ended loads.

The LM4981 provides high quality audio reproduction with minimal external components. A ground referenced output eliminates the output coupling capacitors typically required to drive single-ended loads such as headphones. The ground reference architecture reduces components count, cost and board space consumption, making the LM4981 ideal for handheld MP3 players, mobile phones and other portable equipment where board space is at a premium. Eliminating the output capacitors also improves low frequency response.

The LM4981 operates from a single 2.0V – 4.2V supply, and features a 2-wire, up/down volume control that sets the gain of the amplifier between -33dB to +12dB in 16 discrete steps. Selectable (active high/low) low power shutdown mode provides flexible shutdown control. Superior click and pop suppression eliminates audible transients during start-up and shutdown.

Key Specifications

■ Improved PSRR at 217Hz	67dB (typ)
■ THD+N at 1kHz, 50mW into 32Ω SE (3V)	1.0% (typ)
■ Single Supply Operation (V_{DD})	2.0 to 4.2V
■ Power Output at VDD = 3V, RL = 16Ω, THD ≤ 1%	83mW (typ)
■ Shutdown Current	0.01μA (typ)

Features

- Ground Referenced Outputs
- No Output Coupling Capacitors
- 16-Step Volume Control
- High PSRR
- Available in Space Saving LLP package
- Low Power Shutdown Mode
- Improved Click and Pop Suppression Eliminates Noises During Turn-on and Turn-off Transients
- 2.0V to 4.2V Operation
- 83mW Per Channel Into 16Ω
- Selectable Shutdown Controls (Active High/Low)

Applications

- Portable MP3 Players
- Mobile Phones
- PDAs

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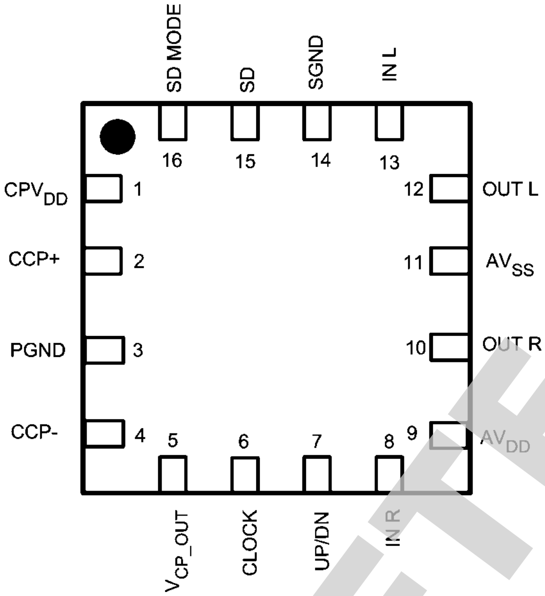
Connection Diagrams

LLP Package



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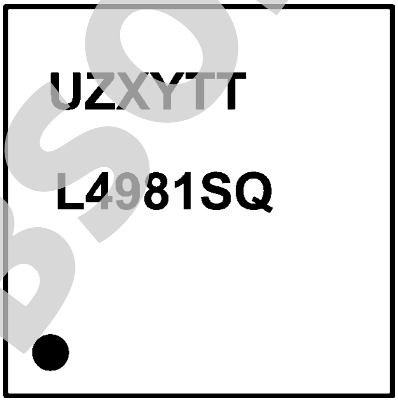
Top View
Order Number LM4981SQ
See NS Package Number SQA16A

LLP Marking



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Top View
U = Wafer Fab code
Z = Assembly plant
XY = 2 Digit date code
TT = Die Traceability
L4981SQ = LM4981SQ

Typical Application

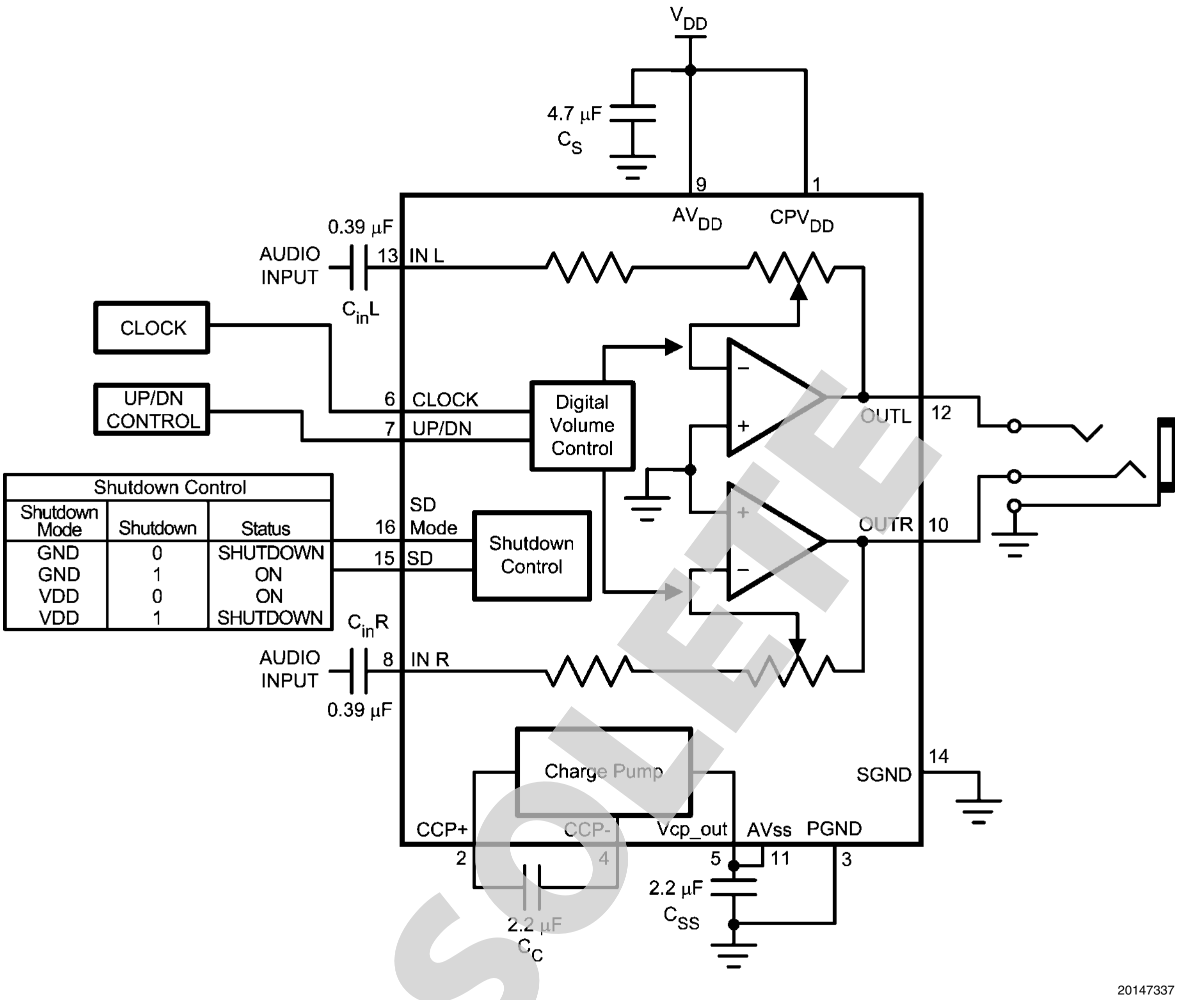


FIGURE 1. Typical Audio Amplifier Application Circuit

Pin	Name	Function
1	CP_{VDD}	Charge Pump Power Supply
2	CCP+	Positive Terminal- charge pump flying capacitor
3	PGND	Power Ground
4	CCP-	Negative Terminal- charge pump flying capacitor
5	VCP_OUT	Charge Pump Output
6	CLOCK	Clock
7	UP/DN	Up / Down
8	INR	Right Input
9	AV_{DD}	Positive Power Supply - Amplifier
10	OUT R	Right Output
11	AV_{SS}	Negative Power Supply - Amplifier
12	OUT L	Left Output
13	IN L	Left Input
14	SGND	Signal Ground
15	SD	Shutdown
16	SD MODE	Shutdown Mode Pin

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	4.5V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2500V
ESD Susceptibility (Note 5)	250V
Junction Temperature	150°C

Operating Ratings

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$-40°C \leq T_A \leq 85°C$
Supply Voltage (V_{DD})	$2.0V \leq V_{CC} \leq 4.2V$

Electrical Characteristics V_{DD} = 3V (Note 1, Note 2)

The following specifications apply for V_{DD} = 3V, AV = 1V/V R_L = 32Ω, f = 1kHz, unless otherwise specified. Limits apply to T_A = 25°C.

Symbol	Parameter	Conditions	LM4981		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, $R_L = \infty$	7	10	mA
I_{SD}	Shutdown Current	V_{SD} = GND	0.1	3.5	μA
V_{IH}	Logic Input Voltage High	SHDN, SDM, CLOCK, U/D		$0.7V_{DD}$	V
V_{IL}	Logic Input Voltage Low	SHDN, SDM, CLOCK, U/D		$0.3V_{DD}$	V
	Digital Volume	Input Referred Maximum Gain	12		dB
		Input Referred Minimum Gain	−33		dB
	Volume Step Size		3		dB
	Step Size Error		±0.3		dB
	Channel-to-Channel Volume Tracking Error	All gain settings	0.15		dB
T_{WU}	Wake Up Time		300		μs
V_{OS}	Output Offset Voltage	R_L = 32Ω	1	5	mV
P_O	Output Power	THD+N = 1% (max); f = 1kHz, R_L = 16Ω, one channel	83		mW
		THD+N = 1% (max); f = 1kHz, R_L = 32Ω, one channel	75		mW
		THD+N = 1% (max); f = 1kHz, R_L = 16Ω, (two channels in phase)	40	33	mW (min)
		THD+N = 1% (max); f = 1kHz, R_L = 32Ω, (two channels in phase)	47	43	mW (min)
THD+N	Total Harmonic Distortion	P_O = 60mW, f = 1kHz, R_L = 16Ω single channel	0.03		%
		P_O = 50mW, f = 1kHz, R_L = 32Ω single channel	0.02		
PSRR	Power Supply Rejection Ratio	$V_{RIPPLE} = 200mV_{P-P}$Sine, f_{RIPPLE} = 1kHz, Inputs AC GND, CI = 1μF	65		dB
		$V_{RIPPLE} = 200mV_{P-P}$Sine, f_{RIPPLE} = 10kHz, Inputs AC GND, CI = 1μF	50		dB
		$V_{RIPPLE} = 200mV_{P-P}$Sine, f_{RIPPLE} = 217Hz	67		dB
ϵ_{OS}	Output Noise	A-Weighted Filter	11		μV

Note 1: All voltages are measured with respect to the GND pin unless other wise specified

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4981, see power derating currents for more information.

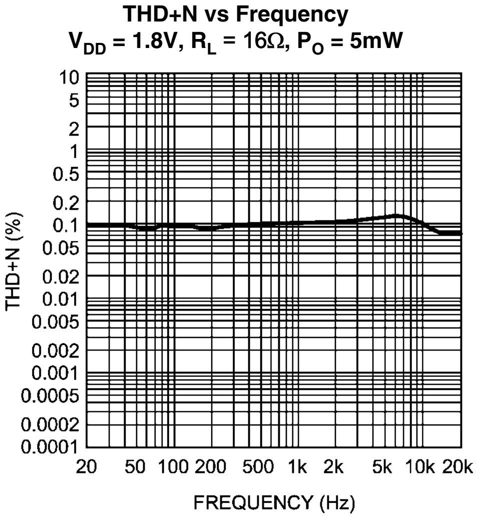
Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF - 240pF discharged through all pins.

Note 6: Typical specifications are specified at +25°C and represent parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Typical Performance Characteristics


THD+N vs Frequency
V_{DD} = 1.8V, R_L = 16Ω, P_O = 5mW

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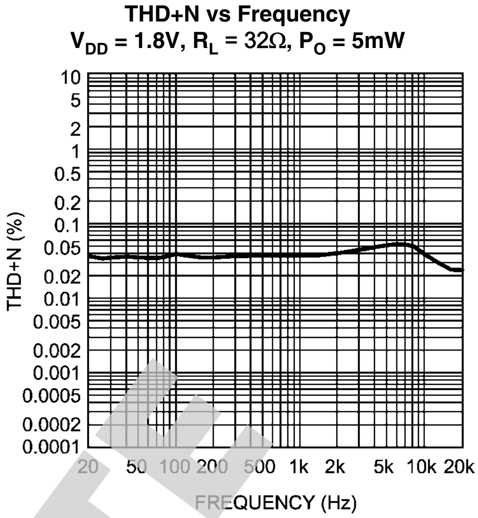
THD+N vs Frequency
V_{DD} = 1.8V, R_L = 32Ω, P_O = 5mW

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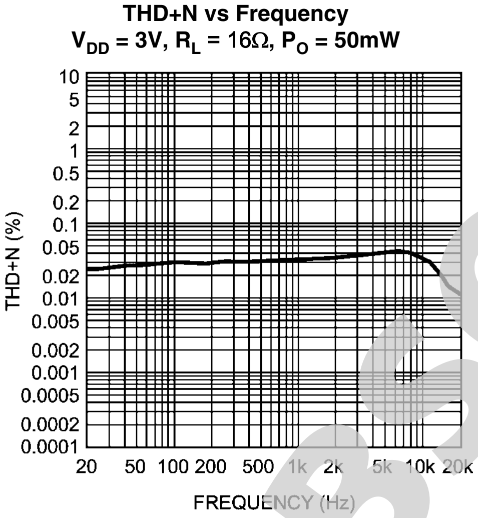
THD+N vs Frequency
V_{DD} = 3V, R_L = 16Ω, P_O = 50mW

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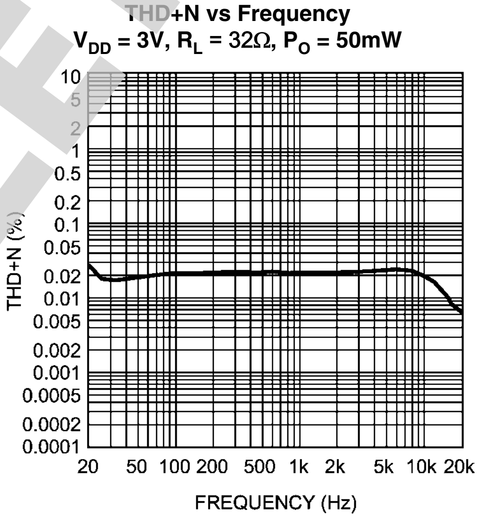
THD+N vs Frequency
V_{DD} = 3V, R_L = 32Ω, P_O = 50mW

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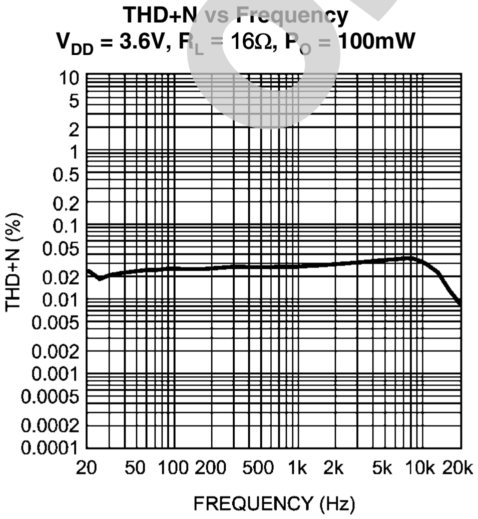
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 16Ω, P_O = 100mW

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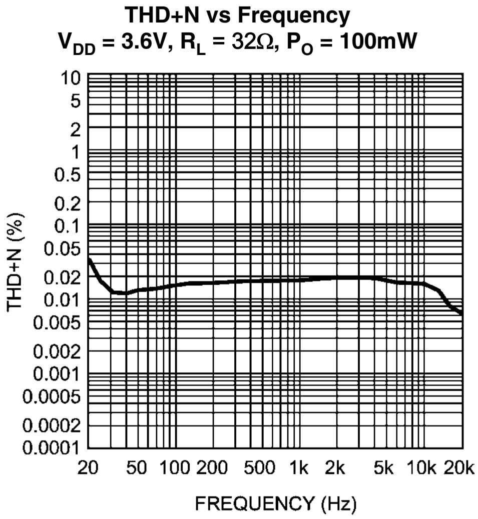
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 32Ω, P_O = 100mW

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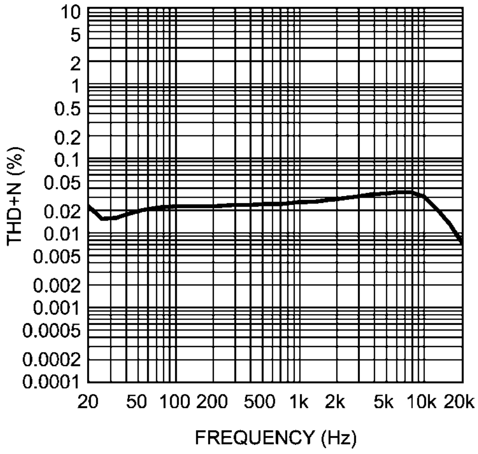
THD+N vs Frequency
V_{DD} = 4.2V, R_L = 16Ω, P_O = 150mW



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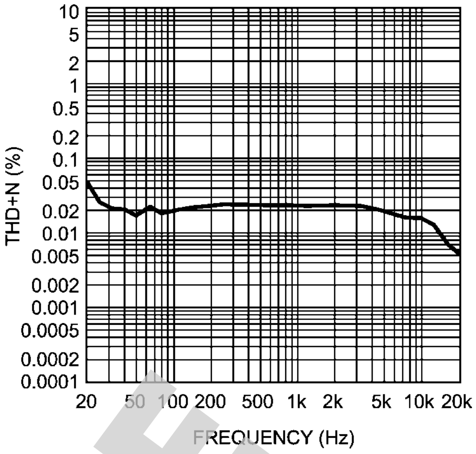
THD+N vs Frequency
V_{DD} = 4.2V, R_L = 32Ω, P_O = 150mW



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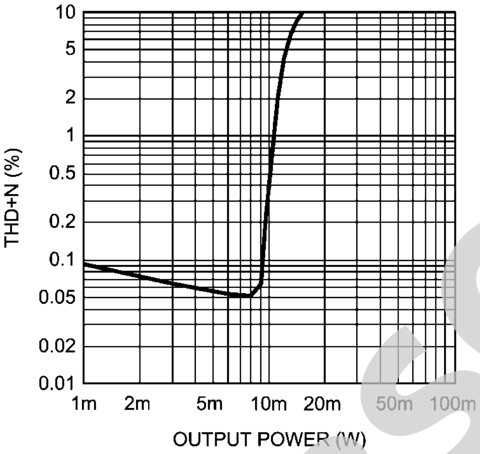
THD+N vs Output Power
V_{DD} = 1.8V, R_L = 16Ω, f = 1kHz, one channel



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THD+N vs Output Power
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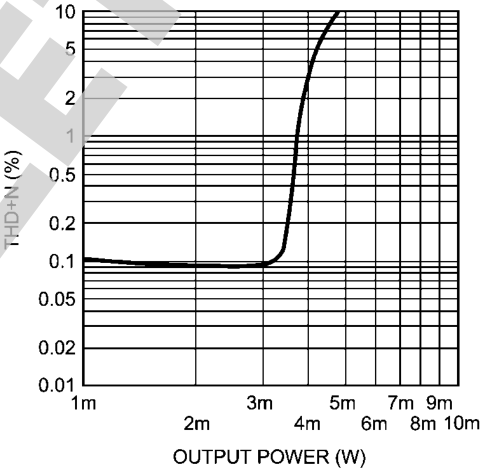

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THD+N vs Output Power
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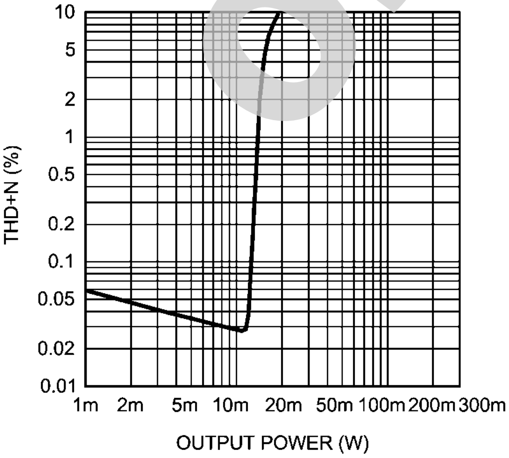

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THD+N vs Output Power
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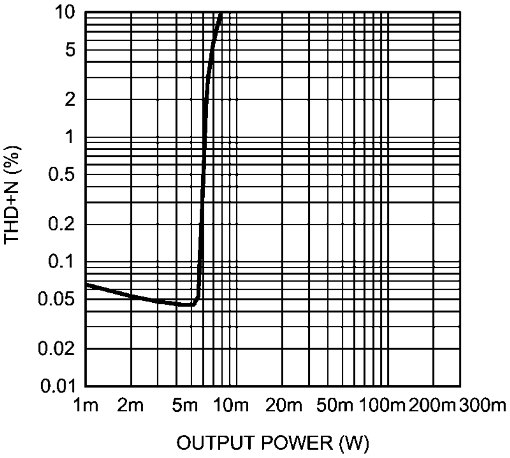

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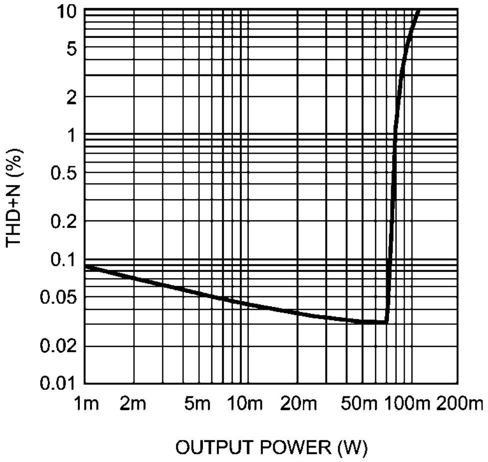
THD+N vs Output Power
V_{DD} = 3V, R_L = 16Ω, f = 1kHz, one channel



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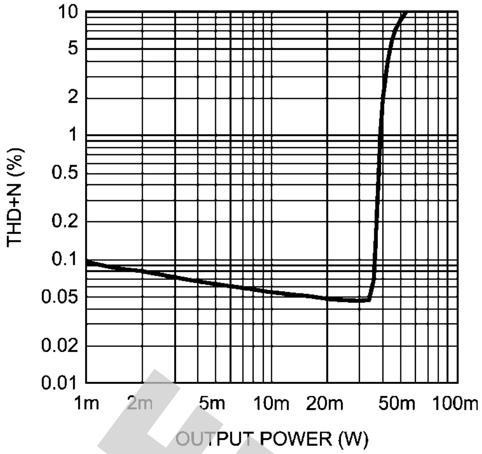
THD+N vs Output Power
V_{DD} = 3V, R_L = 16Ω, f = 1kHz, two channels



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THD+N vs Output Power
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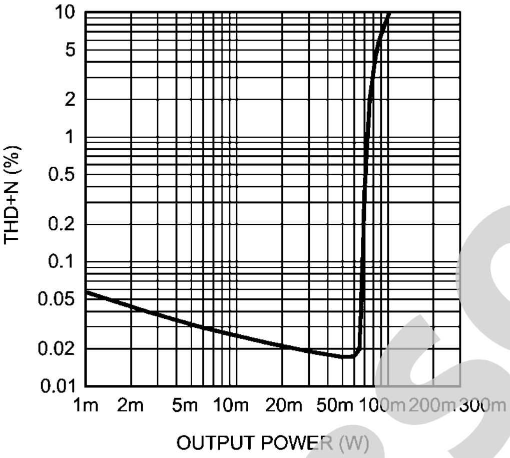

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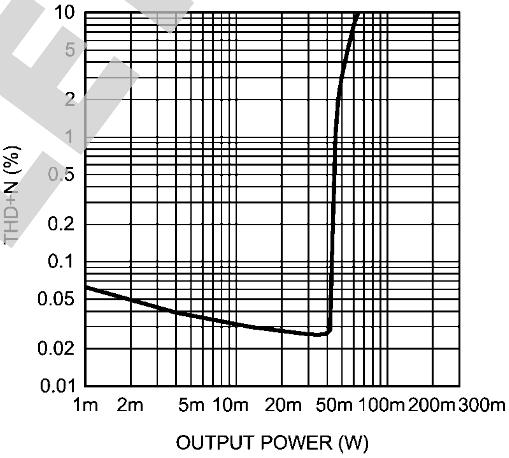
THD+N vs Output Power
V_{DD} = 3V, R_L = 32Ω, f = 1kHz, two channels



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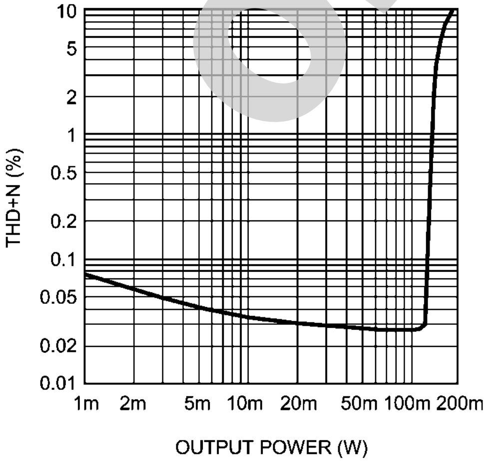
THD+N vs Output Power
V_{DD} = 3.6V, R_L = 16Ω, f = 1kHz, one channel



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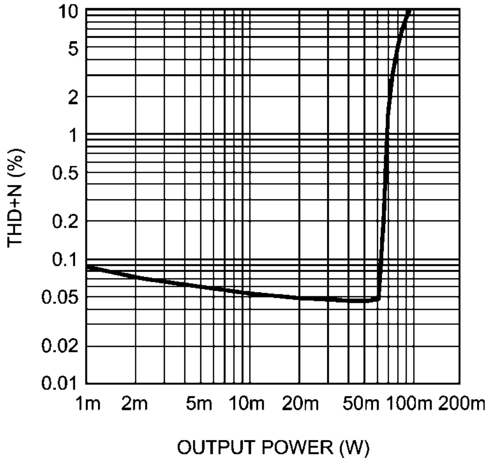
THD+N vs Output Power
V_{DD} = 3.6V, R_L = 16Ω, f = 1kHz, two channels



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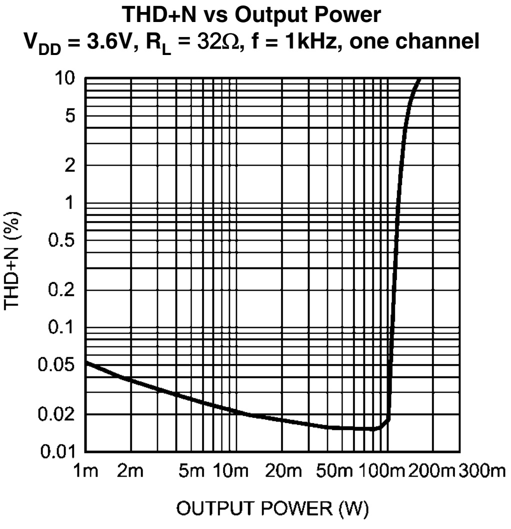
THD+N vs Output Power
V_{DD} = 3.6V, R_L = 32Ω, f = 1kHz, one channel

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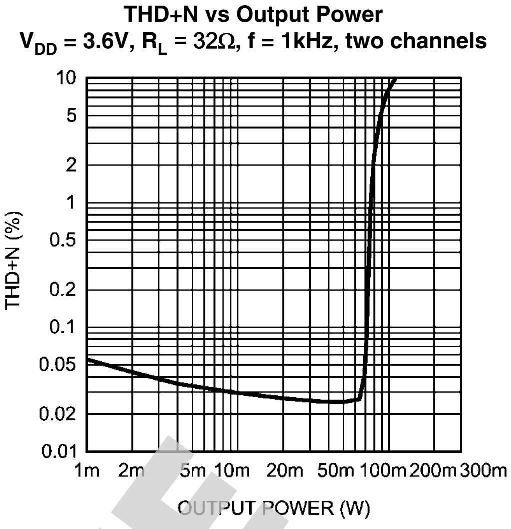
THD+N vs Output Power
V_{DD} = 3.6V, R_L = 32Ω, f = 1kHz, two channels

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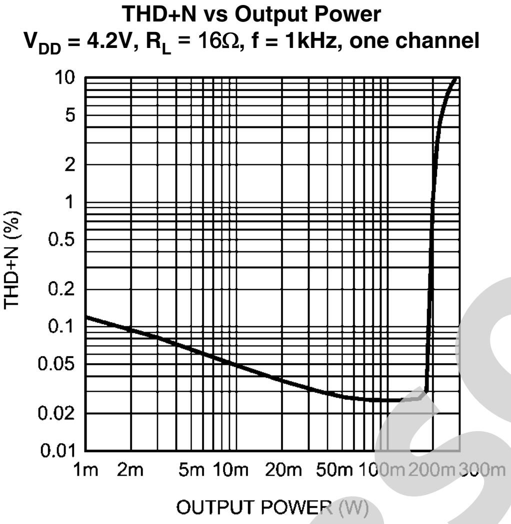
THD+N vs Output Power
V_{DD} = 4.2V, R_L = 16Ω, f = 1kHz, one channel

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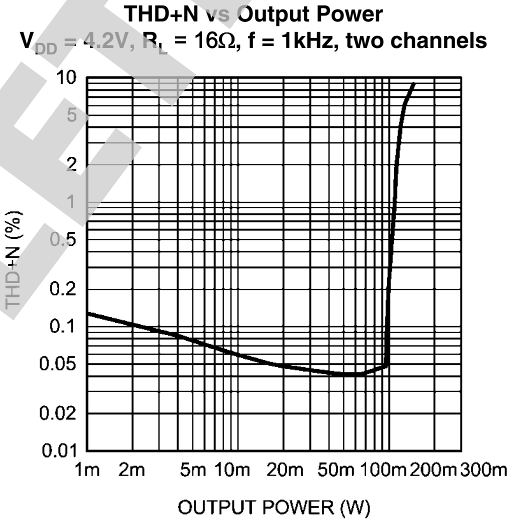
THD+N vs Output Power
V_{DD} = 4.2V, R_L = 16Ω, f = 1kHz, two channels

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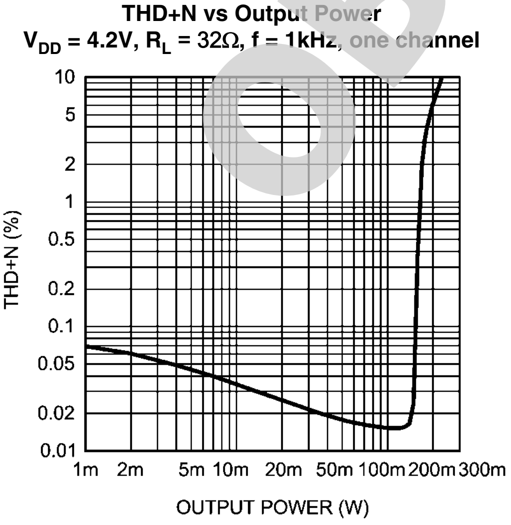
THD+N vs Output Power
V_{DD} = 4.2V, R_L = 32Ω, f = 1kHz, one channel

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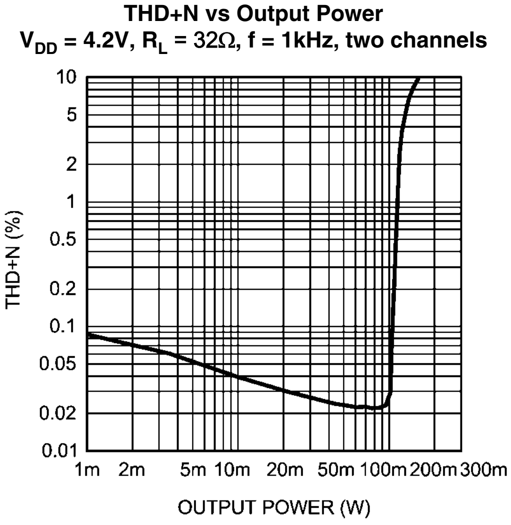
THD+N vs Output Power
V_{DD} = 4.2V, R_L = 32Ω, f = 1kHz, two channels

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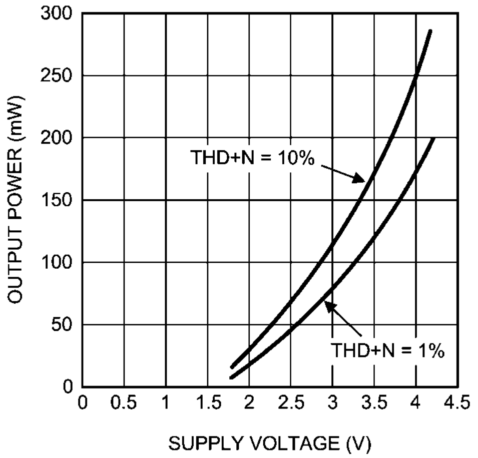
Output Power vs Supply Voltage
R_L = 16Ω, f = 1kHz, one channel



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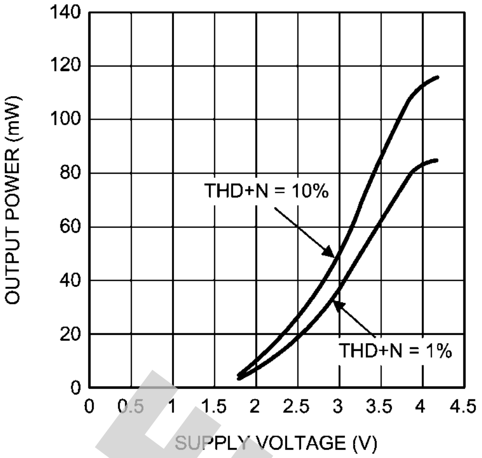
Output Power vs Supply Voltage
R_L = 16Ω, f = 1kHz, two channels



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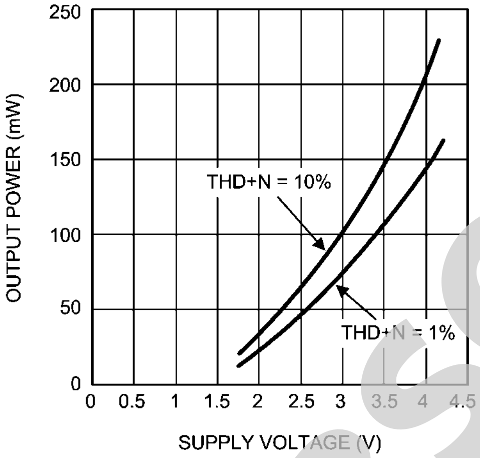
Output Power vs Supply Voltage
R_L = 32Ω, f = 1kHz, one channel



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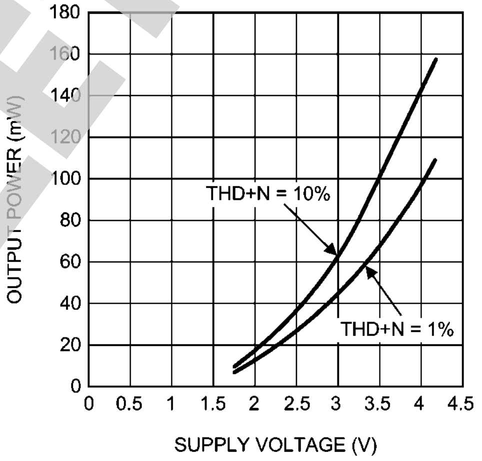
Output Power vs Supply Voltage
R_L = 32Ω, f = 1kHz, two channels



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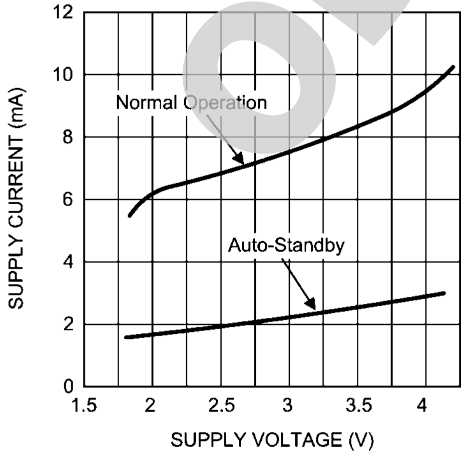
Supply Current vs Supply Voltage



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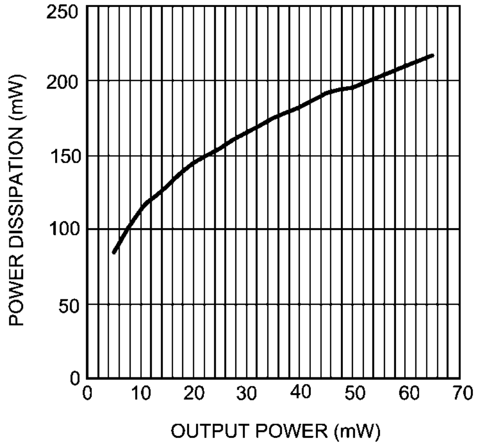
Power Dissipation vs Output Power
R_L = 16Ω, V_{DD} = 3V



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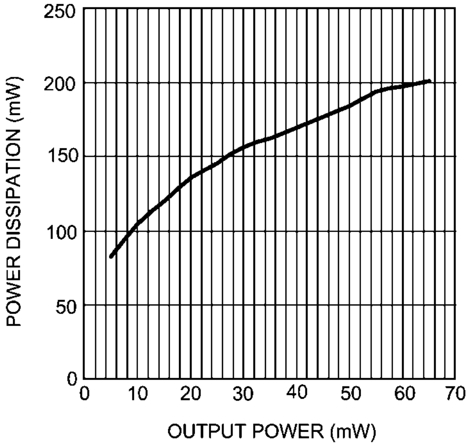
Power Dissipation vs Output Power
$R_L = 32\Omega$, $V_{DD} = 3V$



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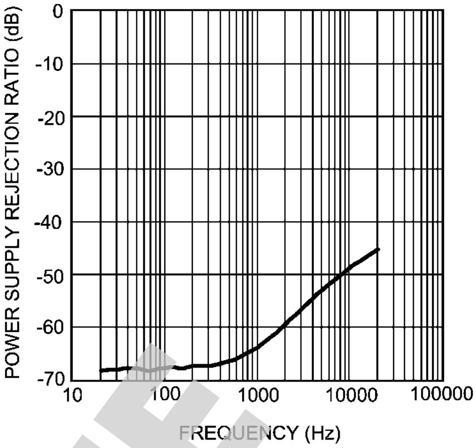
PSRR vs Frequency
$V_{DD} = 3V$, $R_L = 32\Omega$
$V_{ripple} = 200mVp\text{-}p$



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Application Information

DIGITAL VOLUME CONTROL

The LM4981's gain is controlled by the signals applied to the CLOCK and UP/DN inputs. An external clock is required to drive the CLOCK pin. At each rising edge of the clock signal, the gain will either increase or decrease by a 3dB step depending on the logic voltage level applied to the UP/DN pin. A logic high voltage level applied to the UP/DN pin causes the gain to increase by 3dB at each rising edge of the clock signal. Conversely, a logic low voltage level applied to the UP/DN pin causes the gain to decrease 3dB at each rising edge of the clock signal. For both the CLOCK and UP/DN inputs, the trigger point is 1.4V minimum for a logic high level, and 0.4V maximum for a logic low level.

There are 16 discrete gain settings ranging from +12dB maximum to −33dB minimum. Upon device power on, the amplifier's gain is set to a default value of 0dB. However, when coming out of shutdown mode, the LM4981 will revert back to its previous gain setting.

The LM4981's CLOCK and UP/DN pins should be debounced in order to avoid unwanted state changes during transitions between V_{IL} and V_{IH}. This will ensure correct operation of the digital volume control. A microcontroller or microprocessor output is recommended to drive the CLOCK and UP/DN pins.

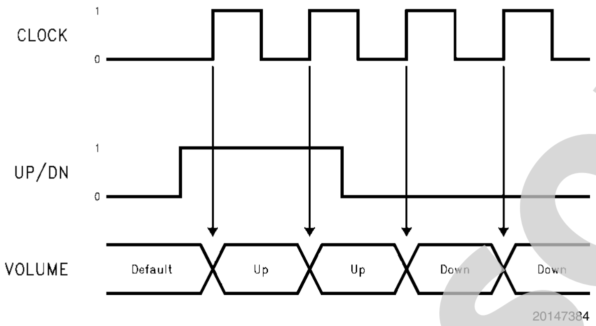


FIGURE 2. Timing Diagram

ELIMINATING THE OUTPUT COUPLING CAPACITOR

The LM4981 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the outputs of the LM4981 to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two, small ceramic charge pump capacitors, saving board space and cost.

Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor form a high pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM4981 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components.

In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM4981 when compared to a traditional headphone amplifier operating from the same supply voltage.

SUPPLY VOLTAGE SEQUENCING

It is a good general practice to first apply the supply voltage to a CMOS device before any other signal or supply on other pins. This is also true for the LM4891 audio amplifier which is a CMOS device.

Before applying any signal to the inputs or shutdown pins of the LM4891, it is important to apply a supply voltage to the V_{DD} pins. After the device has been powered, signals may be applied to the shutdown pins (see MICRO POWER SHUTDOWN) and input pins.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 3V power supply typically use a 4.7µF capacitor in parallel with a 0.1µF ceramic filter capacitor to stabilize the power supply's output, reduce noise on the supply line, and improve the supply's transient response. Keep the length of leads and traces that connect capacitors between the LM4981's power supply pin and ground as short as possible.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

Since the LM4981 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 1. Even with the large internal power dissipation, the LM4981 does not require heat sinking over a large range of ambient temperature. From Equation 1, assuming a 5V power supply and a 32Ω load, the maximum power dissipation point is 40mW per amplifier. Thus the maximum package dissipation point is 80mW. The maximum power dissipation point obtained must not be greater than the power dissipation predicted by Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (2)$$

For a given ambient temperature, T_A, of the system surroundings, Equation 2 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased, the load impedance increased, or T_A reduced.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4981 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. In addition, the LM4981 contains a Shutdown Mode pin, allowing the designer to designate whether the part will be driven into shutdown with a high level logic signal or a low level logic signal. This allows the designer maximum flexibility in device use, as the Shutdown Mode pin may simply be tied permanently to either V_{DD} or GND to set the LM4981 as either a "shutdown-high" device or a "shutdown-low" device, respectively. The device may then be placed into shutdown mode by toggling the Shutdown pin to the same state as the Shutdown Mode pin. For simplicity's sake, this is called "shutdown same", as the LM4981 enters shutdown mode whenever the two pins are in the same logic state. The trigger point for either shutdown high or shutdown low is shown as a typical value in the Supply Current vs Shutdown Voltage graphs in the **Typical Performance Characteristics** section. It is best to switch between ground and supply for maximum performance. While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.1μA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor (or pull-down, depending on shutdown high or low application). This scheme guarantees that the shutdown pin will not float, thus preventing unwanted state changes.

OUTPUT TRANSIENT ('CLICK AND POPS') ELIMINATED

The LM4981 contains advanced circuitry that virtually eliminates output transients ('clicks and pops'). This circuitry prevents all traces of transients when the supply voltage is first applied or when the part resumes operation after coming out of shutdown mode.

EXPOSED-DAP CONSIDERATIONS

It is essential that the exposed Die Attach Paddle (DAP), for the LM4981, is NOT connected to GND. For optimal operation it should be connected to AVss and VCP-OUT(Pins 5 and 11).

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4981's performance requires properly selecting external components. Though the LM4981 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values

Charge Pump Capacitor Selection

Use low ESR (equivalent series resistance) (<100mΩ) ceramic capacitors with an X7R dielectric for best performance. Low ESR capacitors keep the charge pump output impedance to a minimum, extending the headroom on the negative supply. Higher ESR capacitors result in reduced output power from the audio amplifiers.

Charge pump load regulation and output impedance are affected by the value of the flying capacitor (C_C). A larger valued C_C (up to 3.3uF) improves load regulation and minimizes charge pump output resistance. Beyond 3.3uF, the switch-on resistance dominates the output impedance for capacitor values above 2.2uF.

The output ripple is affected by the value and ESR of the output capacitor (C_{SS}). Larger capacitors reduce output ripple on the negative power supply. Lower ESR capacitors minimize the output ripple and reduce the output impedance of the charge pump.

The LM4981 charge pump design is optimized for 2.2uF, low ESR, ceramic, flying, and output capacitors.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitors ($C_{in}A$ and $C_{in}B$ in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using high value input and output capacitors.

Besides affecting system cost and size, the input capacitor has an effect on the LM4981's click and pop performance. The magnitude of the pop is directly proportional to the input capacitor's size. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired –3dB frequency.

As shown in Figure 1, the internal input resistor, R_i and the input capacitor, C_i, produce a -3dB high pass filter cutoff frequency that is found using Equation (3). Conventional headphone amplifiers require output capacitors; Equation (3) can be used, along with the value of R_L, to determine towards the value of output capacitor needed to produce a –3dB high pass filter cutoff frequency.

$$f_{i\text{-}3dB} = 1 / 2\pi R_i C_i \qquad (3)$$

Also, careful consideration must be taken in selecting a certain type of capacitor to be used in the system. Different types of capacitors (tantalum, electrolytic, ceramic) have unique performance characteristics and may affect overall system performance. (See the section entitled Charge Pump Capacitor Selection.)

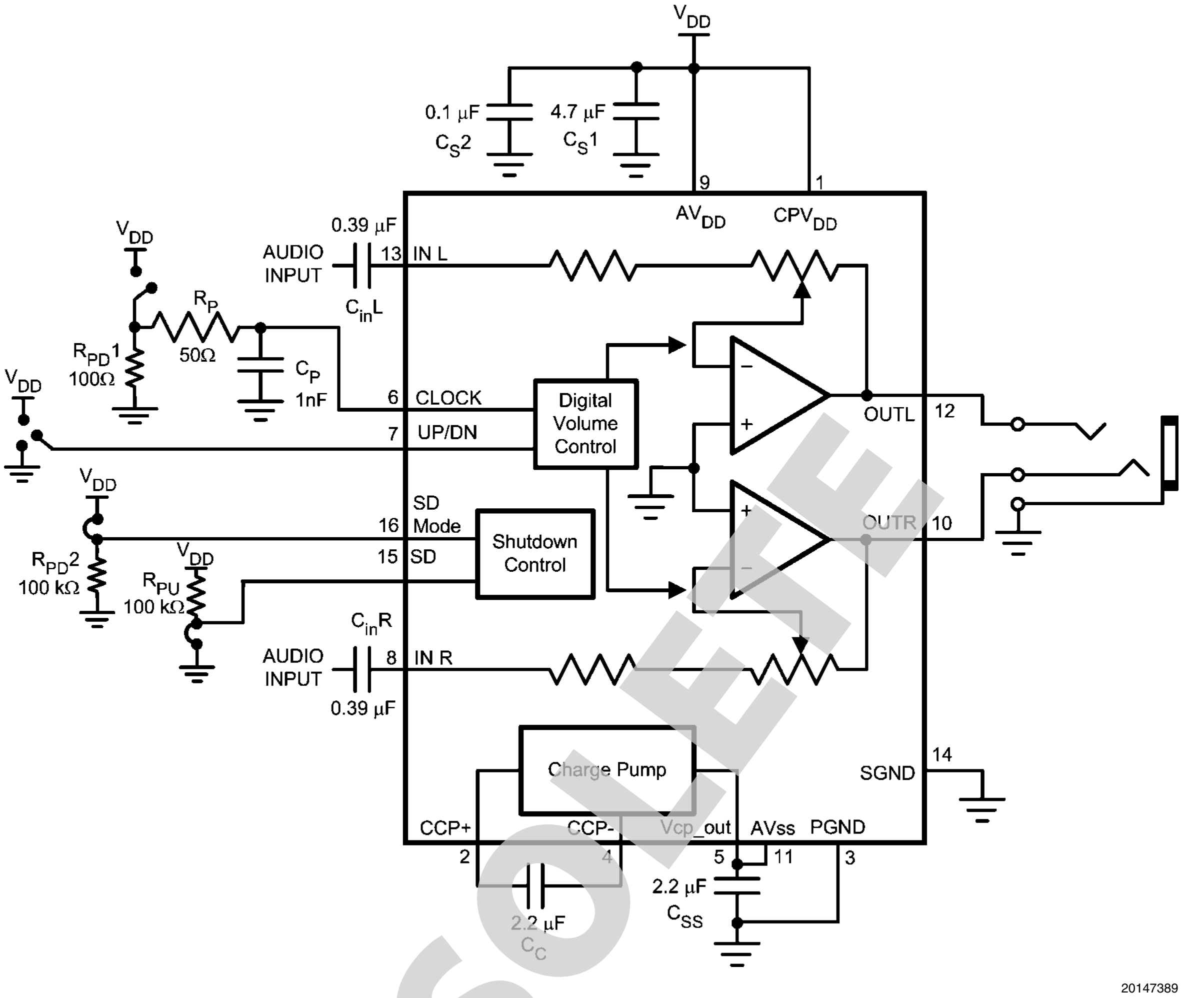
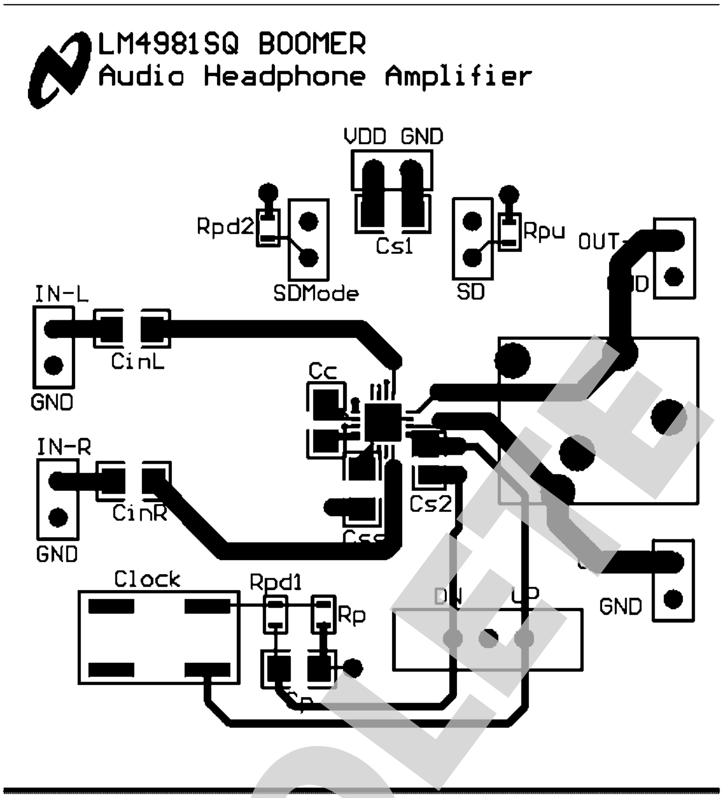


FIGURE 3. Demo Board Schematic

LM4981 DEMO BOARD ARTWORK

Top Layer



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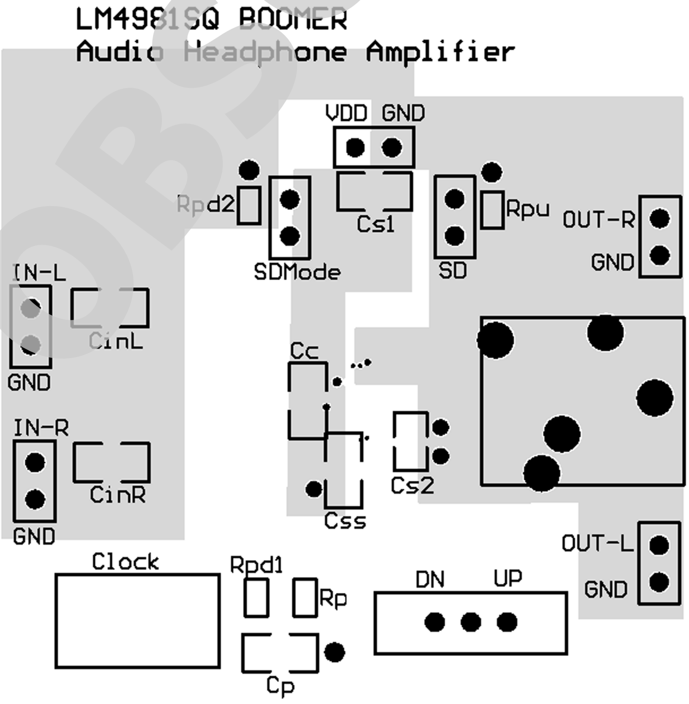
Mid Layer 1



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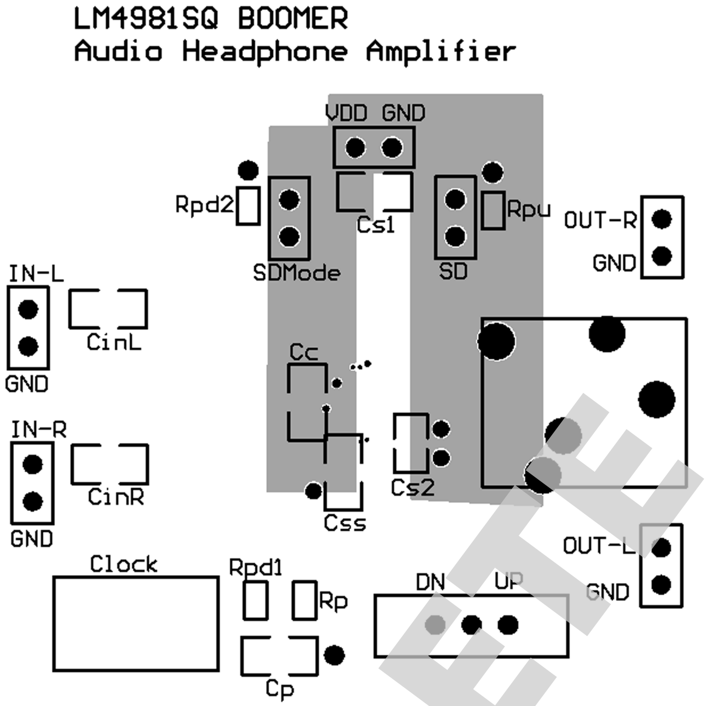
Mid Layer 2



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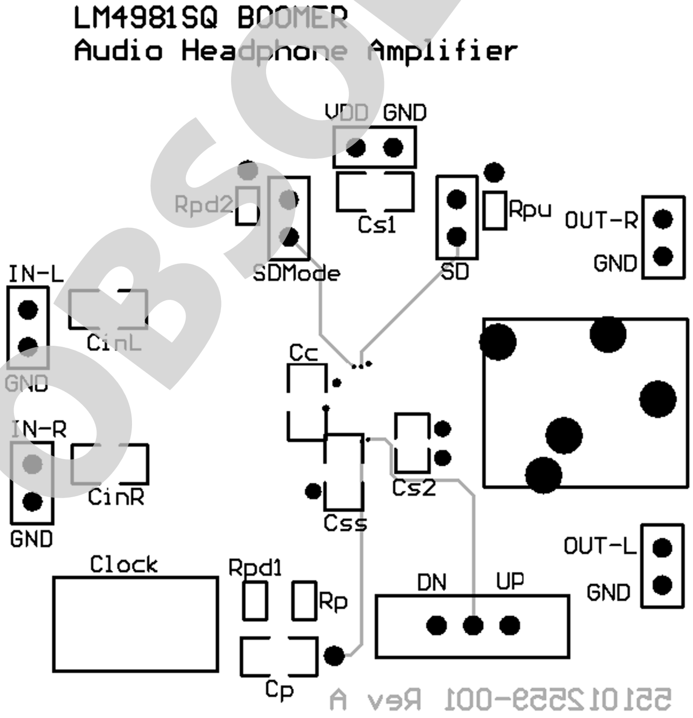
Bottom Layer



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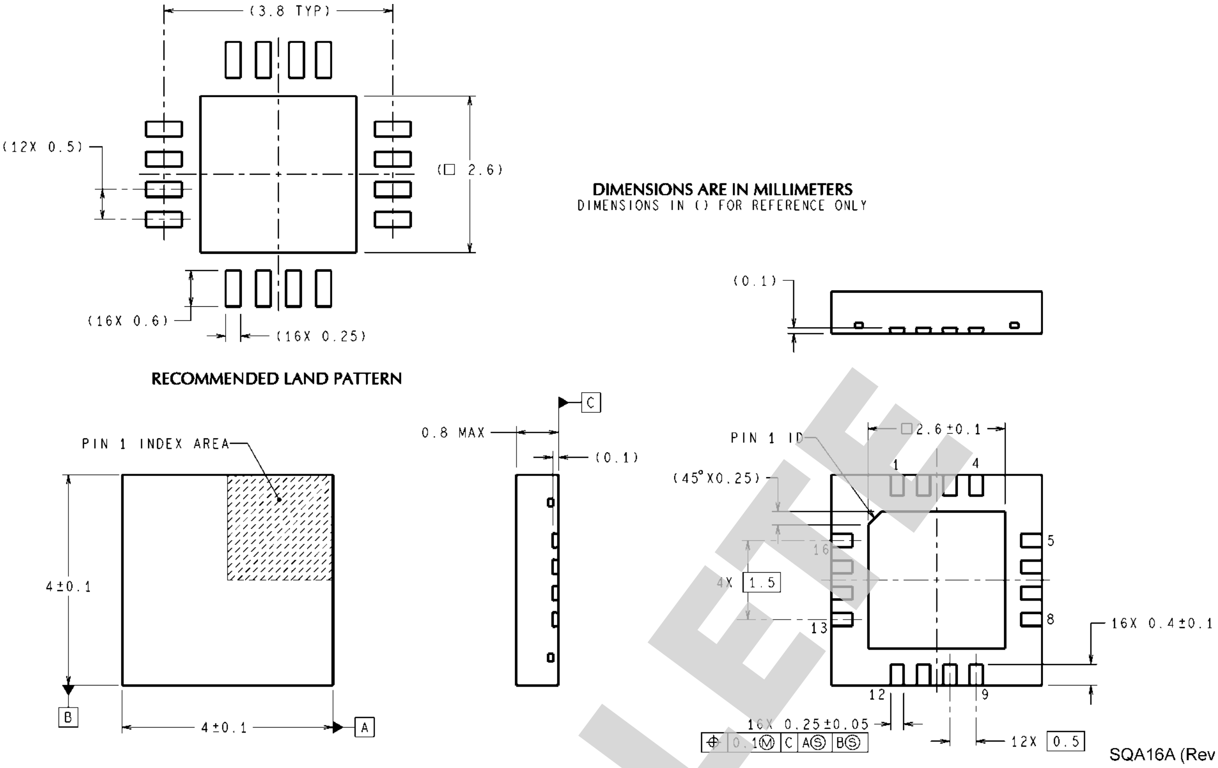
Revision History

Rev	Date	Description
1.0	11/9/05	Initial WEB release.
1.1	12/21/05	Edited the EXPOSED-DAP CONSIDERATIONS (Application Info section), edited the doc title; then re-released D/S to the WEB.
1.2	03/09/06	Deleted the AUTOMATIC STANDBY MODE section (per Vera T.) and Idd (Standby Power Supply Current) from the EC table (per Genevieve), then re-released D/S to the WEB.
1.3	06/05/06	Edited the LLP markings (per Genevieve), then released D/S to the WEB.
1.4	06/21/06	The D/S was taken off the WEB per Genevieve Vansteeg (due to some problems found).
1.5	07/06/06	Released the D/S into the WEB as "PRELIMINARY" per Genevieve Vansteeg.

Physical Dimensions inches (millimeters) unless otherwise noted



SQA16A (Rev A)

Order Number LM4981SQ
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Notes

Notes

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