UNITRODE

Dual 3A MOSFET Driver

UCC17423/4/5
UCC27423/4/5
UCC37423/4/5
PRELIMINARY

FEATURES

- Built using BCDMOS Process
- High Peak Output Current (3A)
- Self Biasing Active Off Outputs
- Pinout Compatible with Industry Standard Drivers
- Undervoltage Lockout (UVLO)
- High Capacitive Load Drive Capability
- CMOS Compatible Input Threshold
- Wide Operating Voltage Range from 4.5V to 18V

DESCRIPTION

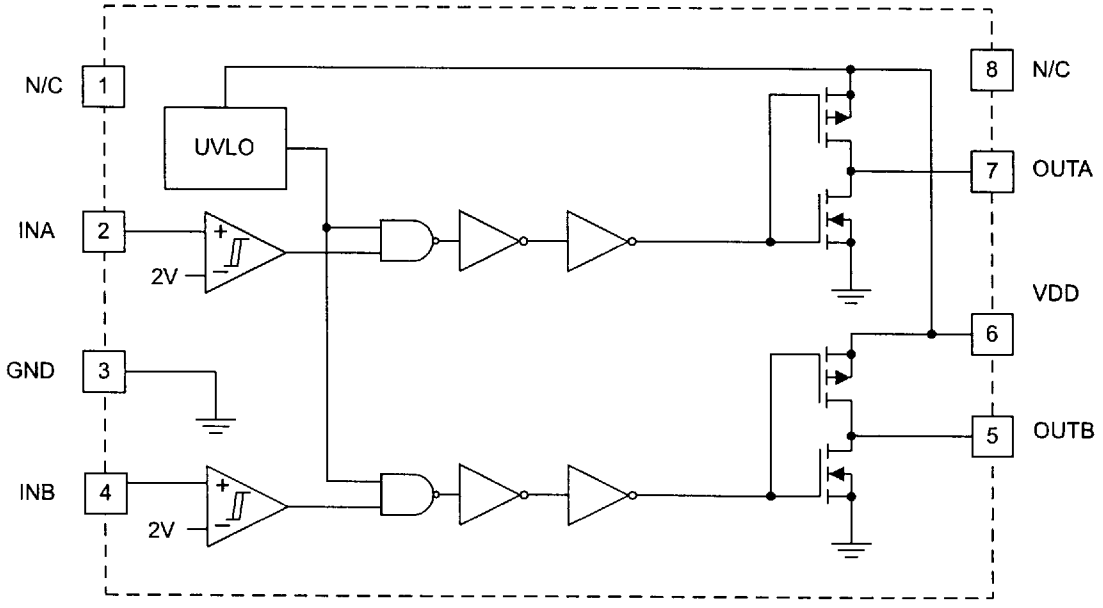
The UCC37423/37424/37425 devices are high speed, dual MOSFET drivers using the BiCMOS/DMOS process. All three devices are designed to be pin and performance compatible with industry standard '423, '424, '425, '426A, '427A, and '428A drivers. Each of the dual outputs is capable of providing 3A peak current and 6A in parallel. In addition, the devices feature Undervoltage Lockout (UVLO) protection and an improved input noise immunity.

The UCC37423 is a dual inverting driver. The UCC37424 is a dual non-inverting driver. The UCC37425 contains one inverting and one non-inverting driver.

In addition to driving two power MOSFETs in high power and high frequency switch mode power supply and motion control applications, these drivers are also capable of driving capacitive and inductive loads in applications such as small motor, relay, solenoid and actuator drivers. Unlike Bipolar Gate Driver ICs, these BCDMOS drivers do not require external Schottky clamp diodes for slight negative voltage overshoot protection.

UCC37423/37424/37425 family of drivers are available in 8 pin SOIC (D), PDIP (N) or CDIP (J), 16 pin SOIC-Wide (DW) or 16 pin SOIC-Power (DP) packages.

BLOCK DIAGRAM



UCC37424 shown. Pin numbers refer to an 8-pin package.

UDG-98135

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ABSOLUTE MAXIMUM RATINGS

Supply voltage 20V
Supply current 25mA
Output Current (OUTA, OUTB) DC 0.2A
Output Current (OUTA, OUTB) DC . . . . . Pulsed (0.5 usec) 5A
Input voltage (pins INA, INB) . . . . . -5V to VDD+0.3V
Storage Temperature Range . . . . . -65 °C to +150 °C
Lead Temperature (soldering 10 sec) . . . . . +300 °C

Unless otherwise indicated, voltages are referenced to GND pin and currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal limitations and considerations of the packages.

ORDERING INFORMATION

UCC☐742☐–☐

PACKAGE SUFFIX
OUTPUT CONFIGURATION
TEMPERATURE RANGE

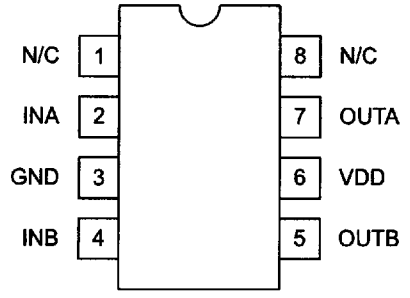
	Temperature Range	Package Suffix
UCC1742X	–55°C to +125°C	J
UCC2742X	–40°C to +85°C	D, DP, DW, N
UCC3742X	0°C to +70°C	D, DP, DW, N

PACKAGE THERMAL RESISTANCE

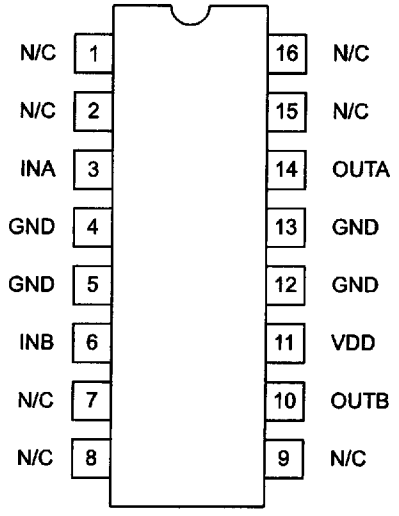
Package	Suffix	Theta (jc)	Theta (ja)
8 pin SOIC	D	42°C/W	84-160°C/W
8 pin plastic DIP	N	49	110
16 pin Power SOIC	DP	20	36-58
16 pin SOIC-wide	DW	27	50-100
8 pin ceramic DIP	J	26	160

CONNECTION DIAGRAMS

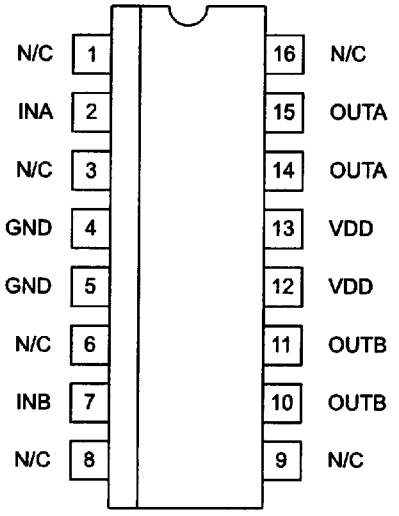
DIP-8, SOIC-8 (TOP VIEW)
N or J, D Packages



DIL-16 (TOP VIEW)
DP Package



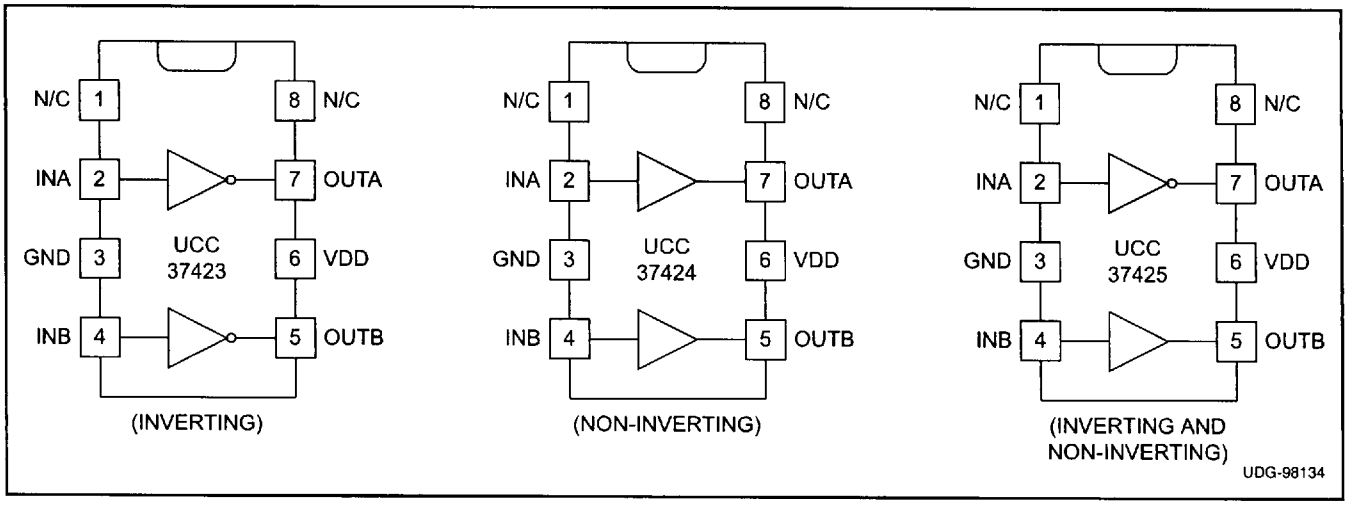
DIL-16 (TOP VIEW)
DW Package



INPUT/OUTPUT TABLE

INPUTS (V_{IN_L}, V_{IN_H})		UCC37423		UCC37424		UCC37425	
INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
> 1.6V	< 1.6V	VOH	VOH	VOL	VOL	VOH	VOL
> 1.6V	> 2.4V	VOH	VOL	VOL	VOH	VOH	VOH
< 2.4V	< 1.6V	VOL	VOH	VOH	VOL	VOL	VOL
< 2.4V	> 2.4V	VOL	VOL	VOH	VOH	VOL	VOH

PART VERSIONS



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, the MIN and MAX specifications apply for 4.5V≤ VDD ≤18V, $T_J = T_A$. Unless otherwise specified, the TYP specifications apply for VDD = 12V, T_A = 25 °C, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Section					
V_{IN_H}, Logic 1 Input Threshold (INA, INB)		2.4			V
V_{IN_L}, Logic 0 Input Threshold (INA, INB)				1.6	V
Input current (INA, INB)	0V ≤ V(IN[AB]) ≤ VDD	–10	0	10	µA
Output Section					
V_{OH}, Output OUTA, OUTB High Level	$V_{OH} = V_{DD} - V_{OUT}$		0.001	0.025	V
V_{OL}, Output OUTA, OUTB Low Level			0.001	0.025	V
Output Resistance High	I(OUT)=10mA, VDD = 18V		1.2	8	Ω
Output Resistance Low	I(OUT)=10mA, VDD = 18V		3.5	8	Ω
Peak Output Current	(Note 1)		3		A
Latch-up Protection	(Note 1)	> 500			mA
Switching Time Section					
t_R, OUTA,OUTB Rise Time	C_{LOAD} = 1800 pF (See Figure 1)		20	60	ns
t_F, OUTA,OUTB Fall Time	C_{LOAD} = 1800 pF (See Figure 1)		25	60	ns
t_{D1}, Delay (IN[AB] to OUT[AB]) Rising	C_{LOAD} = 1800 pF (See Figure 1)		50	100	ns
t_{D2}, Delay (IN[AB] to OUT[AB]) Falling	C_{LOAD} = 1800 pF (See Figure 1)		50	100	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, the MIN and MAX specifications apply for 4.5V≤ VDD ≤18V, $T_J = T_A$. Unless otherwise specified, the TYP specifications apply for VDD = 12V, T_A = 25 °C, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout Section					
Start Threshold		4.2	4.3	4.5	V
Start to Stop Hysteresis		0.4	0.6	0.9	V
Power Supply Section					
Operating Current	Static, Inputs = 0V		3.5	5	mA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

GND: Common ground. This ground should be connected very closely to the source of the power MOSFET which the driver is driving.

INA: Input A. Input signal for the A driver, logic compatible threshold and hysteresis.

INB: Input B. Input signal for the B driver, logic compatible threshold and hysteresis.

OUTA: Driver output A. This complementary MOS output swings to both VDD and GND.

OUTB: Driver output B. This complementary MOS output swings to both VDD and GND.

VDD: Supply voltage. This is the supply voltage for the IC. Good bypassing is required between VDD and GND.

APPLICATION INFORMATION

Supply Section

The IC operates over a wide supply range, from 4.5V to 18V.

Input Section

The input circuit contains hysteresis to maximize noise immunity. The inputs are designed such that they can swing up to 5V below GND without damage to the IC.

Output Section

The output circuit is designed to drive a MOSFET gate on and off in 25nsec typically. The output will supply a high peak output current (3A peak). The output of the driver uses complementary devices and will swing the gate fully between the two supply rails. The outputs are designed to withstand 500mA reverse current without either damage or logic upset. The outputs are actively pulled down during undervoltage lockout even in the absence of VDD power.

Inverting outputs of UCC37423 and OUTA of UCC37425 are intended to drive external P-channel MOSFETs. Non-inverting outputs of UCC37424 and OUTB of UCC37425 are intended to drive N-channel MOSFETs.

Undervoltage Lockout Section

The under voltage detection circuit prevents the outputs from turning on the external power MOSFET when VDD is below a preset value.

When the IC is in an Undervoltage mode, the output states will be the same as if the input was low during normal operation. For example, outputs of UCC37423 (inverting) will be held high, outputs of UCC37424 (non-inverting) will be held low and outputs of UCC37425 (inverting + non-inverting) will be held high and low respectively for OUTA and OUTB. Under this mode, the inverting outputs on UCC37423 and OUTA of UCC37425 will track VDD.

APPLICATION INFORMATION

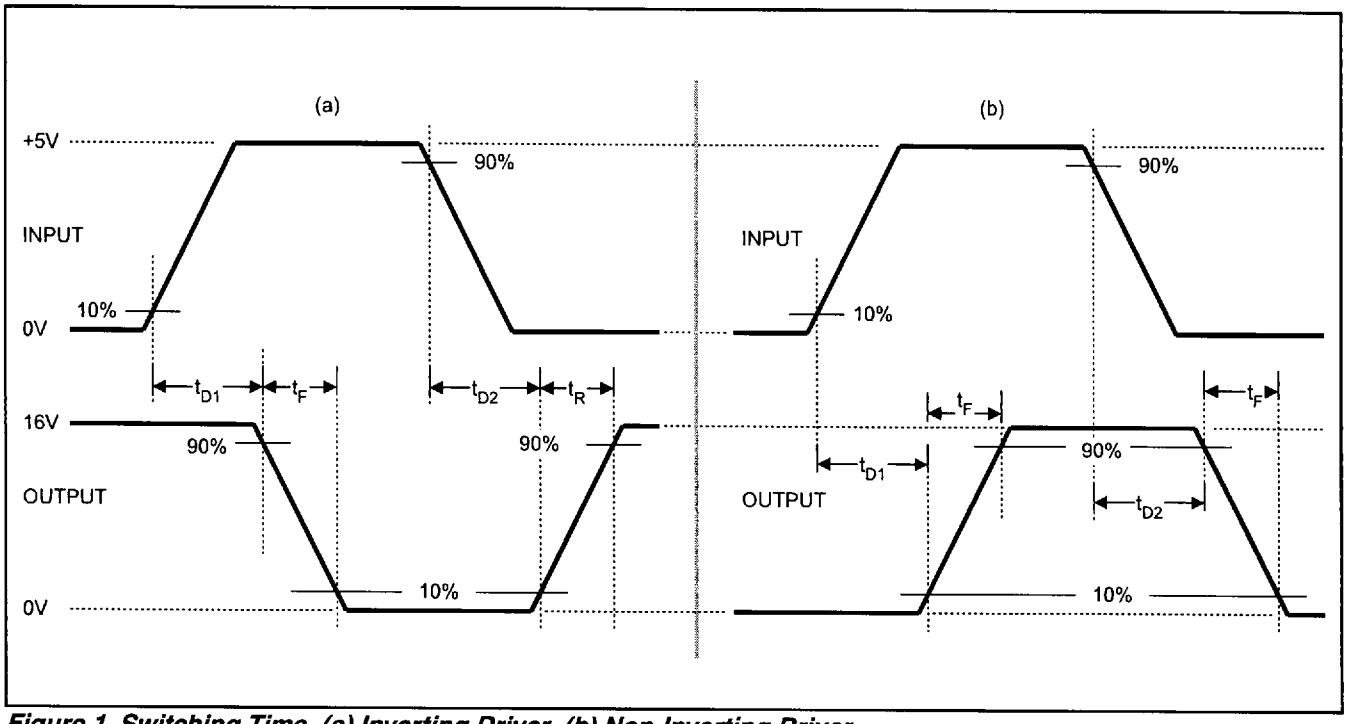


Figure 1. Switching Time (a) Inverting Driver (b) Non-Inverting Driver

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Mechanical Drawings

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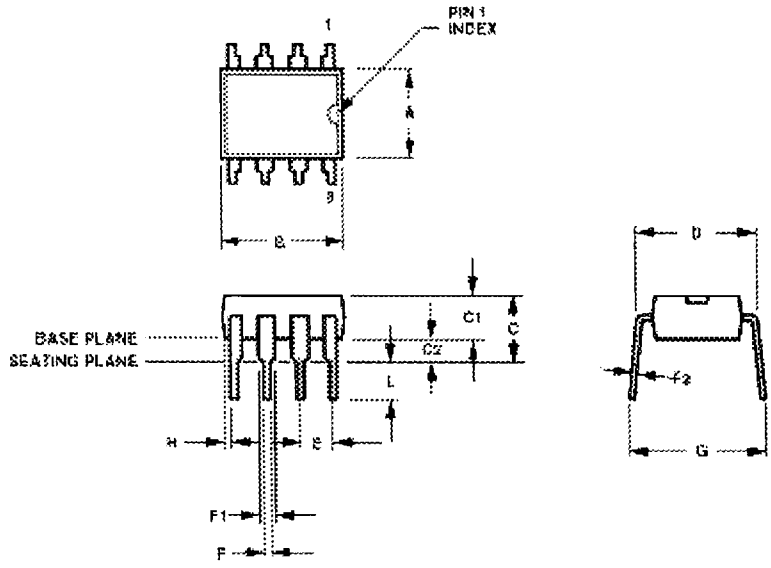
8-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	-	.210	-	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	-	0.13	-	
L	.115	.160	2.92	4.06	



NOTES:

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

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Mechanical Drawings

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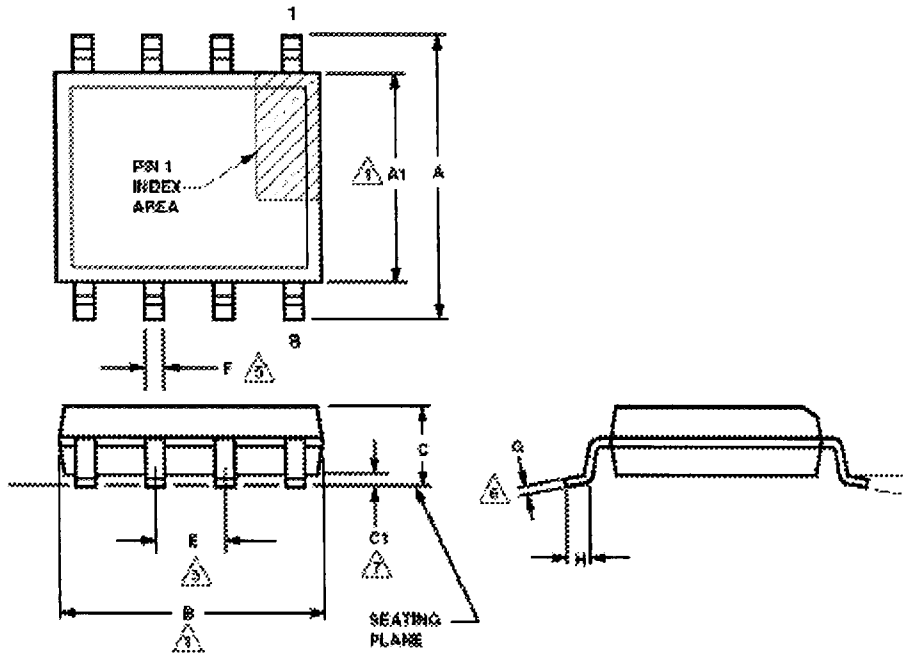
8-PIN SOIC SURFACE MOUNT~ D, DP PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

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Mechanical Drawings

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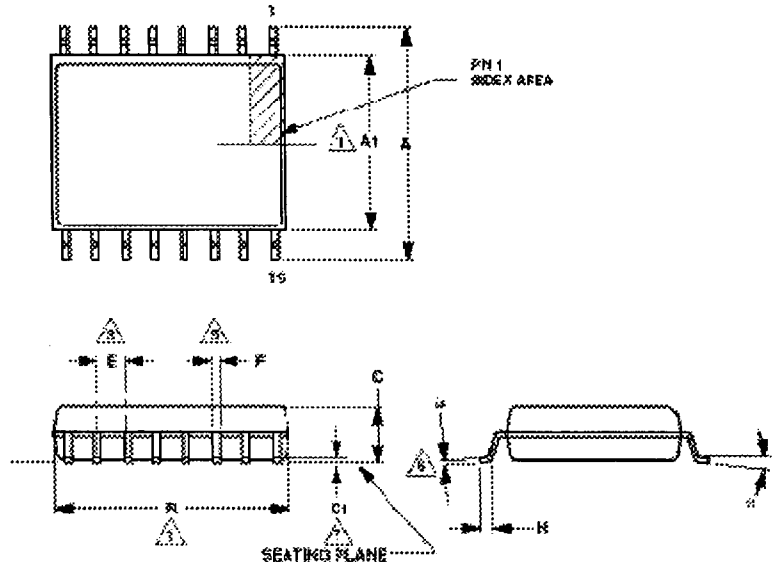
16-PIN SOIC SURFACE MOUNT~ DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.403	.413	10.24	10.49
C	.097	.104	2.48	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°



NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

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Mechanical Drawings

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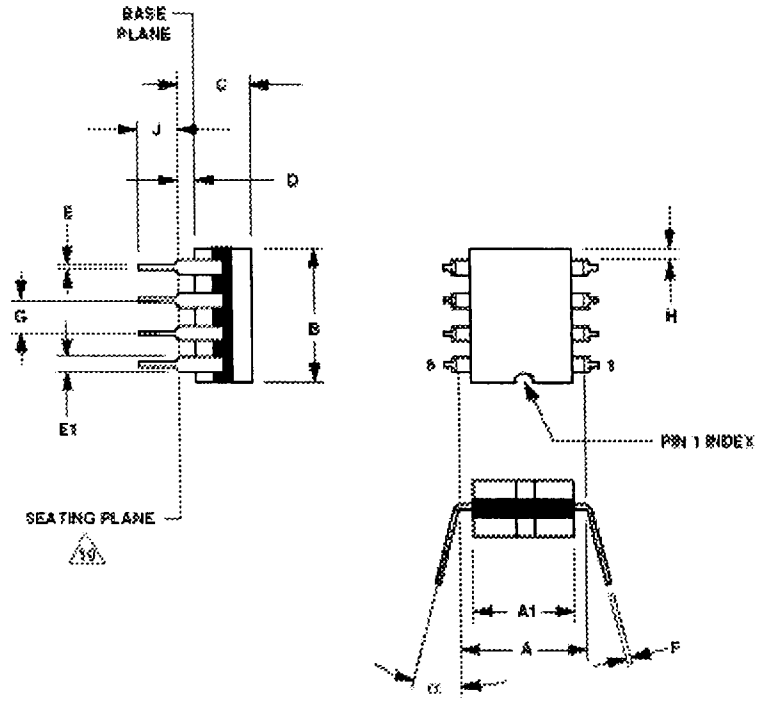
8-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	-	0.405	-	10.29	4
C	-	0.200	-	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	-	0.13	-	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'E1' MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION 'D' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION 'A' SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS 'E' AND 'F' SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.