Freescale Semiconductor Data Sheet: Technical Data Document Number: MPXA6115A Rev 7.2, 10/2012

High Temperature Accuracy Integrated Silicon Pressure Sensor for Measuring Absolute Pressure, On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MPXxx6115A series sensor integrates on-chip, bipolar op amp circuitry and thin film resistor networks to provide a high output signal and temperature compensation. The small form factor and high reliability of onchip integration make the pressure sensor a logical and economical choice for the system designer.

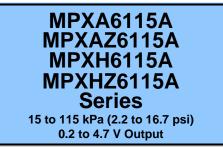
The MPXxx6115A series piezoresistive transducer is a state-of-the-art, monolithic, signal conditioned, silicon pressure sensor. This sensor combines advanced micromachining techniques, thin film metallization, and bipolar semiconductor processing to provide an accurate, high level analog output signal that is proportional to applied pressure.

Features

- · Resistant to High Humidity and Common Automotive Media
- Improved Accuracy at High Temperature
- · Available in Small and Super Small Outline Packages
- 1.5% Maximum Error over 0° to 85°C
- · Ideally suited for Microprocessor or Microcontroller-Based Systems
- Temperature Compensated from -40° to +125°C
- Durable Thermoplastic (PPS) Surface Mount Package

ORDERING INFORMATION									
Device Name	Package			# of Ports	5		Pressure Type	e	Device
Device Name	Option	Case No.	None	Single	Dual	Gauge	Differential	Absolute	Marking
Small Outline Package	e (MPXA6115A Ser	ies)							
MPXA6115A6U	Rails	482	•					•	MPXA6115A
MPXA6115A6T1	Tape and Reel	482	•					•	MPXA6115A
MPXA6115AC6U	Rails	482A		•				•	MPXA6115A
MPXA6115AC6T1	Tape and Reel	482A		•				•	MPXA6115A
MPXA6115AC7U	Rails	482C		•				•	MPXA6115A
Small Outline Package	e (Media Resistant	Gel) (MPXAZ	6115A S	eries)					
MPXAZ6115A6U	Rails	482	•					•	MPXAZ6115A
MPXAZ6115AC6U	Rails	482A		•				•	MPXAZ6115A
MPXAZ6115AC6T1	Tape and Reel	482A		•				•	MPXAZ6115A
MPXAZ6115AP	Trays	1369		•				•	MPXAZ6115A
MPXAZ6115APT1	Tape and Reel	1369		•				•	MPXAZ6115A
Super Small Outline P	ackage (MPXH611	5A Series)							
MPXH6115A6U	Rails	1317	•					•	MPXH6115A
MPXH6115A6T1	Tape and Reel	1317	•					•	MPXH6115A
MPXH6115AC6U	Rails	1317A		•				•	MPXH6115A
MPXH6115AC6T1	Tape and Reel	1317A		•				•	MPXH6115A

© 2007-2012 Freescale Semiconductor, Inc. All rights reserved.



Application Examples

- Aviation Altimeters
- Industrial Controls
- Engine Control/Manifold Absolute Pressure (MAP)
- Weather Station and Weather Reporting Device Barometers

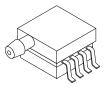


ORDERING INFORMATION									
Small Outline Package (Small Outline Package (Media Resistant Gel) (MPXHZ6115A Series)								
MPXHZ6115A6U	Rails	1317	•					•	MPXHZ6115A
MPXHZ6115A6T1	Tape and Reel	1317	•					•	MPXHZ6115A
MPXHZ6115AC6U	Rails	1317A		•				•	MPXHZ6115A
MPXHZ6115AC6T1	Tape and Reel	1317A		•				•	MPXHZ6115A

SMALL OUTLINE PACKAGES



MPXA6115AC7U CASE 482C



MPXAZ6115AP/T1 CASE 1369



MPXA6115AC6U/T1 MPXAZ6115AC6U/T1 CASE 482A



MPXA6115A6U/T1 MPXAZ6115A6U CASE 482

SUPER SMALL OUTLINE PACKAGES



MPXH6115A6U/T1 MPXHZ6115A6U/T1 CASE 1317



MPXH6115AC6U/T1 MPXHZ6115AC6U/T1 CASE 1317A

Operating Characteristics

Table 1. Operating Characteristics ($V_S = 5.0 \text{ Vdc}$, $T_A = 25^{\circ}\text{C}$ unless otherwise noted, P1 > P2)

Characteristic	Symbol	Min	Тур	Max	Unit
Pressure Range	P _{OP}	15	—	115	kPa
Supply Voltage ⁽¹⁾	Vs	4.75	5.0	5.25	Vdc
Supply Current	I _o	—	6.0	10	mAdc
Minimum Pressure Offset ⁽²⁾ (0 to 85°C) @ $V_S = 5.0$ Volts	V _{off}	0.133	0.200	0.268	Vdc
Full Scale Output ⁽³⁾ (0 to 85°C) @ $V_S = 5.0$ Volts	V _{FSO}	4.633	4.700	4.768	Vdc
Full Scale Span ⁽⁴⁾ (0 to 85°C) @ V _S = 5.0 Volts	V _{FSS}	4.433	4.500	4.568	Vdc
Accuracy ⁽⁵⁾ (0 to 85°C)				±1.5	%V _{FSS}
Sensitivity	V/P	—	45.0	—	mV/kPa
Response Time ⁽⁶⁾	t _R	_	1.0	—	ms
Warm-Up Time ⁽⁷⁾	_	—	20	—	ms
Offset Stability ⁽⁸⁾	—	—	±0.25	—	%V _{FSS}

1. Device is ratiometric within this specified excitation range.

2.Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.

3. Full Scale Output (V_{FSO}) is defined as the output voltage at the maximum or full rated pressure.

4. Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.

5. Accuracy is the deviation in actual output from nominal output over the entire pressure range and temperature range as a percent of span at 25°C due to all sources of error including the following:

Linearity:Output deviation from a straight line relationship with pressure over the specified pressure range.Temperature Hysteresis:Output deviation at any temperature within the operating temperature range, after the temperature is cycled to
and from the minimum or maximum operating temperature points, with zero differential pressure applied.Pressure Hysteresis:Output deviation at any pressure within the specified range, when this pressure is cycled to and from minimum or
maximum rated pressure at 25°C.TcSpan:Output deviation over the temperature range of 0° to 85°C, relative to 25°C.TcOffset:Output deviation with minimum pressure applied, over the temperature range of 0° to 85°C, relative to 25°C.

6. Response Time is defined as the time for the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.

7. Warm-up Time is defined as the time required for the product to meet the specified output voltage after the pressure has been stabilized.

8. Offset Stability is the product's output deviation when subjected to 1000 cycles of Pulsed Pressure, Temperature Cycling with Bias Test.

Maximum Ratings

 Table 2. Maximum Ratings⁽¹⁾

Rating	Symbol	Value	Units
Maximum Pressure (P1 > P2)	P _{max}	400	kPa
Storage Temperature	T _{stg}	-40° to +125°	°C
Operating Temperature	T _A	-40° to +125°	°C
Output Source Current @ Full Scale Output ⁽²⁾	I _o +	0.5	mAdc
Output Sink Current @ Minimum Pressure Offset ⁽²⁾	I _o -	-0.5	mAdc

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.

2. Maximum Output Current is controlled by effective impedance from Vout to Gnd or Vout to Vs in the application circuit.

Figure 1 shows a block diagram of the internal circuitry integrated on a pressure sensor chip.

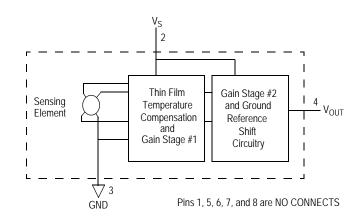


Figure 1. Fully Integrated Pressure Sensor Schematic

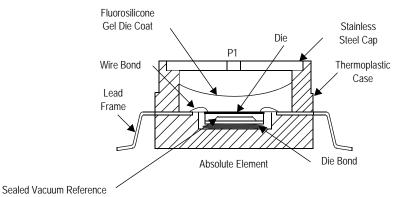
On-chip Temperature Compensation and Calibration

Figure 2 illustrates the absolute sensing chip in the basic Super Small Outline chip carrier (Case 1317).

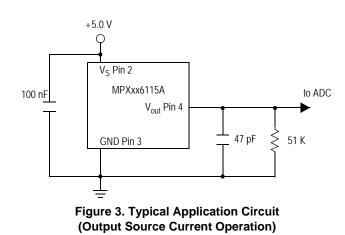
Figure 3 shows a typical application circuit (output source current operation).

Figure 4 shows the sensor output signal relative to pressure input. Typical minimum and maximum output curves are shown for operation over 0° to 85°C temperature range. The output will saturate outside of the rated pressure range.

A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm. The MPXxx6115A series pressure sensor operating characteristics, internal reliability and qualification tests are based on use of dry air as the pressure media. Media other than dry air may have adverse effects on sensor performance and long-term reliability. Contact the factory for information regarding media compatibility in your application.







Δ

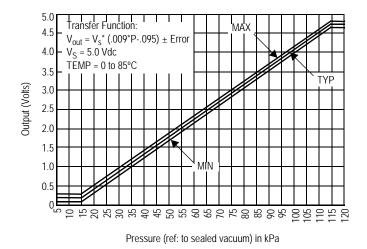
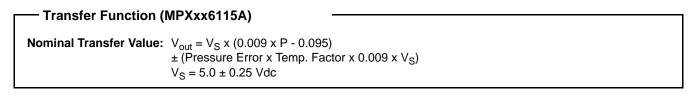
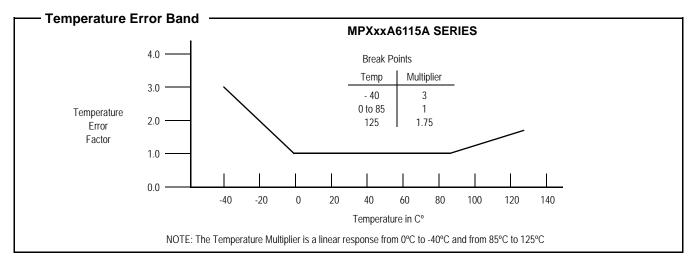
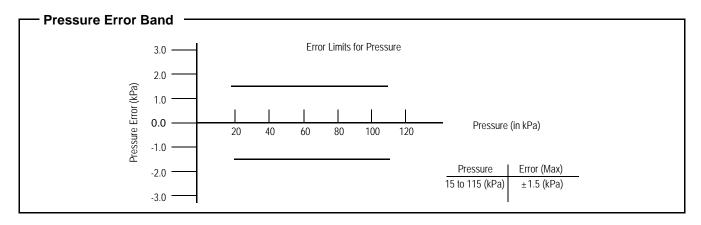


Figure 4. Output vs. Absolute Pressure







MINIMUM RECOMMENDED FOOTPRINT FOR SMALL AND SUPER SMALL PACKAGES

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor package must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a

solder reflow process. It is always recommended to fabricate boards with a solder mask layer to avoid bridging and/or shorting between solder pads, especially on tight tolerances and/or tight layouts.

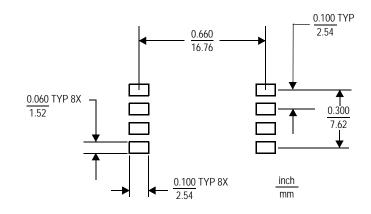


Figure 5. SOP Footprint (Case 482)

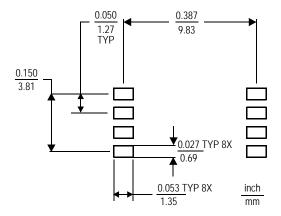
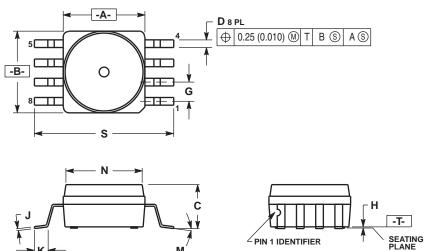


Figure 6. SSOP Footprint (Case 1317 and 1317A)

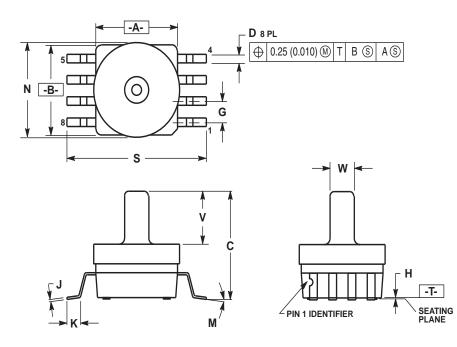


M

NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006). 5. ALL VERTICAL SURFACES 5' TYPICAL DRAFT.

	INC	HES	MILLIM	ETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.415	0.425	10.54	10.79	
В	0.415	0.425	10.54	10.79	
С	0.212	0.230	5.38	5.84	
D	0.038	0.042	0.96	1.07	
G	0.100	BSC	2.54	2.54 BSC	
Н	0.002	0.010	0.05	0.25	
J	0.009	0.011	0.23	0.28	
K	0.061	0.071	1.55	1.80	
Μ	0°	7°	0°	7°	
N	0.405	0.415	10.29	10.54	
S	0.709	0.725	18.01	18.41	

CASE 482-01 **ISSUE O** SMALL OUTLINE PACKAGE

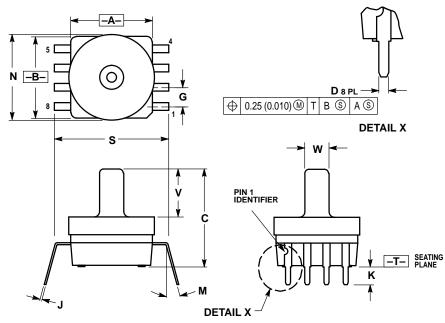


NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006). 5. ALL VERTICAL SURFACES 5' TYPICAL DRAFT.

	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.415	0.425	10.54	10.79
В	0.415	0.425	10.54	10.79
С	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100	BSC	2.54	BSC
Н	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
Κ	0.061	0.071	1.55	1.80
М	0°	7°	0°	7°
Ν	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
۷	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

CASE 482A-01 **ISSUE A** SMALL OUTLINE PACKAGE

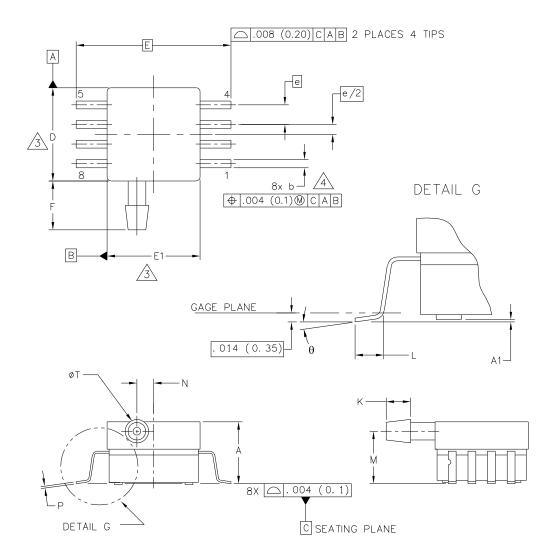
Downloaded from Arrow.com.



NOTES:
 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
 DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.415	0.425	10.54	10.79
В	0.415	0.425	10.54	10.79
С	0.500	0.520	12.70	13.21
D	0.026	0.034	0.66	0.864
G	0.100	BSC	2.54	BSC
J	0.009	0.011	0.23	0.28
Κ	0.100	0.120	2.54	3.05
М	0 °	15 °	0 °	15 °
Ν	0.444	0.448	11.28	11.38
S	0.540	0.560	13.72	14.22
٧	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

CASE 482C-03 **ISSUE B** SMALL OUTLINE PACKAGE



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. MECHANICA		L OUTLINE	PRINT VERSION NO	DT TO SCALE
TITLE:	DOCUMENT NO): 98ASA99303D	REV: D	
8 LD SOP, SIDE PO	CASE NUMBER	8: 1369-01	13 DEC 2010	
		STANDARD: NO	N-JEDEC	

PAGE 1 OF 2

CASE 1369-01 ISSUE B SMALL OUTLINE PACKAGE

NOTES:

- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- ▲ DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.
- A DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

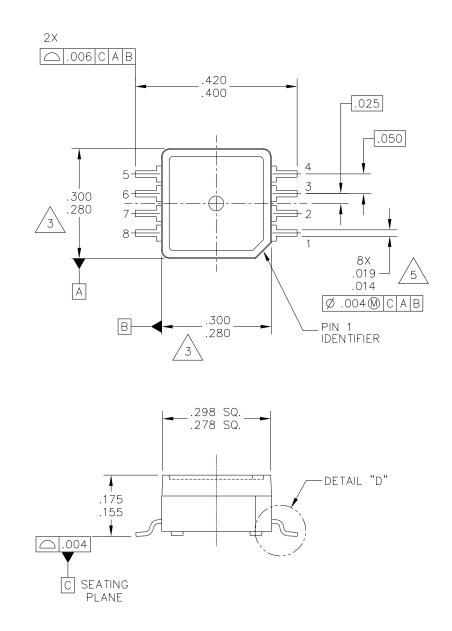
	INC	HES	MIL	LIMETERS		11	NCHES	MI	LLIMETERS
DIM	MIN	MAX	Min	MAX	DIM	Min	MAX	MIN	MAX
А	.300	.330	7.62	8.38	θ	0.	7.	0.	7.
A1	.002	.010	0.05	0.25	-				
b	.038	.042	0.96	1.07	-				
D	.465	.485	11.81	12.32	-				
E	.717	BSC	18	3.21 BSC	-				
E1	.465	.485	11.81	12.32	-				
е	.100	BSC	2.	54 BSC	-				
F	.245	.255	6.22	6.47	-				
к	.120	.130	3.05	3.30	-				
L	.061	.071	1.55	1.80	-				
М	.270	.290	6.86	7.36	-				
N	.080	.090	2.03	2.28	-				
Ρ	.009	.011	0.23	0.28	-				
Т	.115	.125	2.92	3.17	-				
©	FREESCALE SEN ALL RIGH	ICONDUCTOR, TS RESERVED.	INC.	MECHANICA	AL OUTLINE PRINT VERSION NOT TO SCALE			DT TO SCALE	
TITL	_E:				DOCUMENT NO: 98ASA99303D REV: D				REV: D
	8 LC) SOP, S	IDE PO	DRT	CASE NUMBER: 1369-01 13 DEC 2010				13 DEC 2010
STANDARD: NON-JEDEC									

PAGE 2 OF 2

Freescale Semiconductor, Inc.

Sensors

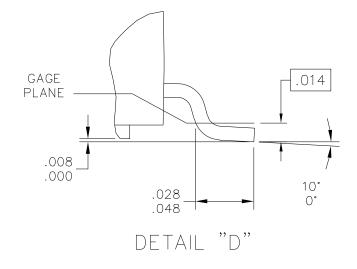
CASE 1369-01 ISSUE B SMALL OUTLINE PACKAGE



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NO	T TO SCALE
TITLE: 8 FAD	DOCUME	NT NO: 98ARH99066A	REV: H
SSOP	CASE NU	JMBER: 1317–04	13 APR 2012
3301	STANDA	RD: NON-JEDEC	

PAGE 1 OF 3

CASE 1317-04 ISSUE H SUPER SMALL OUTLINE PACKAGE



	ALE SEMICONDUCTOR, INC. L RIGHTS RESERVED.	MECHANICAL OU	TLINE	PRINT VERSION NO	T TO SCALE
TITLE:	8 I F A D		DOCUME	NT NO: 98ARH99066A	REV: H
			CASE NU	JMBER: 1317-04	13 APR 2012
	5501		STANDAF	RD: NON-JEDEC	

PAGE 2 OF 3

CASE 1317-04 **ISSUE H** SUPER SMALL OUTLINE PACKAGE

NOTES:

- 1. ALL DIMENSIONS IN INCHES.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

Z. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .006 INCHES PER SIDE.

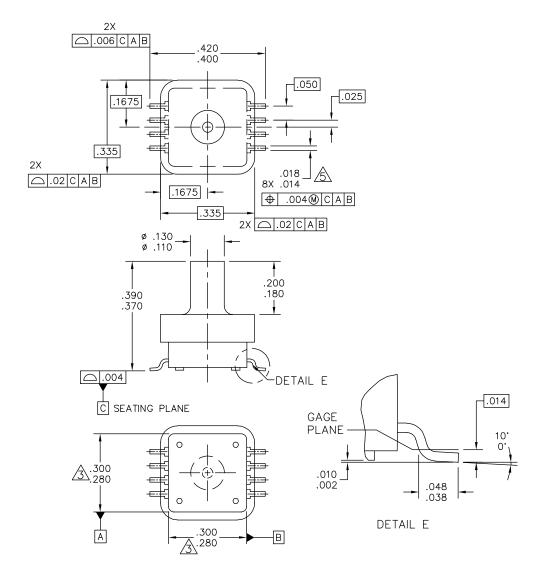
4. ALL VERTICAL SURFACES TO BE 5' MAXIMUM.

25. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 INCHES MAXIMUM.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLIN	E PRINT VERSION NO	T TO SCALE
TITLE: 8 FAD	DOC	UMENT NO: 98ARH99066A	REV: H
	CAS	E NUMBER: 1317-04	13 APR 2012
330P	STA	NDARD: NON-JEDEC	

PAGE 3 OF 3

CASE 1317-04 ISSUE H SUPER SMALL OUTLINE PACKAGE



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	IICAL OUTLINE PRINT VERSION NOT		
TITLE:	DOCUMENT N	10: 98ARH99089A	REV: D	
8 LD, PORTED S	SOP CASE NUMBE	CR: 1317A-04	26 OCT 2006	
	STANDARD: 1	STANDARD: NON-JEDEC		

PAGE 1 OF 2

CASE 1317A-04 ISSUE D SUPER SMALL OUTLINE PACKAGE

NOTES:

- 1. ALL DIMENSIONS IN INCHES.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .006 INCHES PER SIDE.



- 4. ALL VERTICAL SURFACES TO BE 5' MAXIMUM.
- <u>_5</u>. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 INCHES MAXIMUM.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE:		DOCUMENT NO	: 98ARH99089A	REV: D
8 LD, PORTED SSOP		CASE NUMBER	R: 1317A-04	26 OCT 2006
		STANDARD: NO	N-JEDEC	

PAGE 2 OF 2

CASE 1317A-04 **ISSUE D** SUPER SMALL OUTLINE PACKAGE

Table 3. Revision History

Revision number	Revision date	Description of changes	
7.1	05/2012	 Updated Package Drawing 98ARH99066A was Rev. F, updated to Rev. H, 	
7.2	10/2012	 On page 1, changed typical output voltage from 4.8V to 4.7V to match typical output voltage listed on page 3 of document 	

How to Reach Us: Home Page: freescale.com Web Support: freescale.com/support Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/salestermsandconditions.

Freescale, the Freescale logo, Energy Efficient Solutions logo, are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Xtrinsic is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2012 Freescale Semiconductor, Inc.



