HS-4424DRH, HS4424DEH

Dual, Noninverting Power MOSFET Radiation Hardened Drivers

FN8747
Rev 2.00
October 15, 2015

The radiation hardened HS-4424 family are noninverting, dual, monolithic high-speed MOSFET drivers designed to convert low voltage control input signals into higher voltage, high current outputs. The HS-4424DRH, HS-4424DEH are fully tested across the 8V to 18V operating range.

The inputs of these devices can be directly driven by the HS-1825ARH PWM device or by our ACS/ACTS and HCS/HCTS type logic devices. The fast rise times and high current outputs allow very quick control of high gate capacitance power MOSFETs in high frequency applications.

The high current outputs minimize power losses in MOSFETs by rapidly charging and discharging the gate capacitance. The output stage incorporates a low voltage lockout circuit that puts the outputs into a three-state mode when the supply voltage is below its Undervoltage Lockout (UVLO) threshold voltage.

Constructed with Intersil's dielectrically isolated Rad Hard Silicon Gate (RSG) BiCMOS process, these devices are immune to single event latch-up and have been specifically designed to provide highly reliable performance in harsh radiation environments.

TABLE 1. HS4424 PRODUCT FAMILY SPECIFIC UVLO Vth

PART NUMBER	UVLO (V)
HS-4424RH HS-4424EH	<10
HS4424BRH HS4424BEH	<7.5
HS4424DRH HS4424DEH	<8

Features

- Electrically screened to DLA SMD# 5962-99560
- QML qualified per MIL-PRF-38535 requirements
- Latch-up immune
- Radiation environment
- High dose rate (50-300rad(Si)/s). . . . . 300krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . 50krad(Si)*
  *Limit established by characterization
- I_{PEAK}. . . . . >2A (minimum)
- Matched rise and fall times (C_L = 4300pF). . 75ns (maximum)
- Low voltage lockout feature . . . . . <8V
- Wide supply voltage range . . . . . 8V to 18V
- Propagation delay . . . . . .250ns (maximum)
- Consistent delay times with V_{CC} changes
- Low power consumption
  - 40mW with inputs high
  - 20mW with inputs low
- Low equivalent input capacitance . . . . . 3.2pF (typical)
- ESD protected. . . . . >4kV

Applications

- Switching power supplies
- DC/DC converters
- Motor controllers

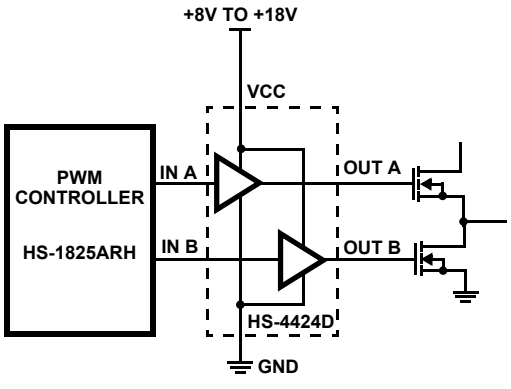


FIGURE 1. TYPICAL APPLICATION

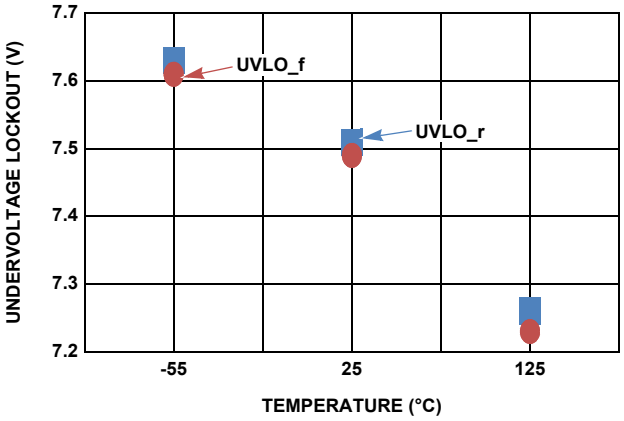
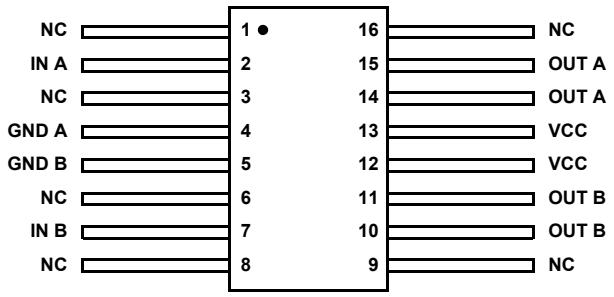


FIGURE 2. UNDERVOLTAGE LOCKOUT vs TEMPERATURE

Pin Configuration

HS-4424DRH, HS-4424DEH
(16 LD FLATPACK)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	EQUIVALENT ESD CIRCUIT	DESCRIPTION
1, 3, 6, 8, 9, 16	NC	NA	No Internal Connection
2	IN A	Circuit 2	Driver A Input
4	GND A	NA	Ground Reference A
5	GND B	NA	Ground Reference B
7	IN B	Circuit 2	Driver B Input
10, 11	OUT B	NA	Driver B Output
12, 13	VCC	Circuit 1	Positive Power Supply
14, 15	OUT A	NA	Driver A Output

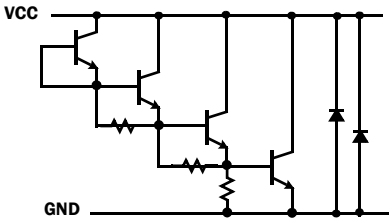


FIGURE 3. CIRCUIT 1

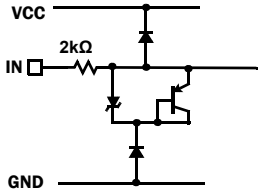


FIGURE 4. CIRCUIT 2

Functional Block Diagram

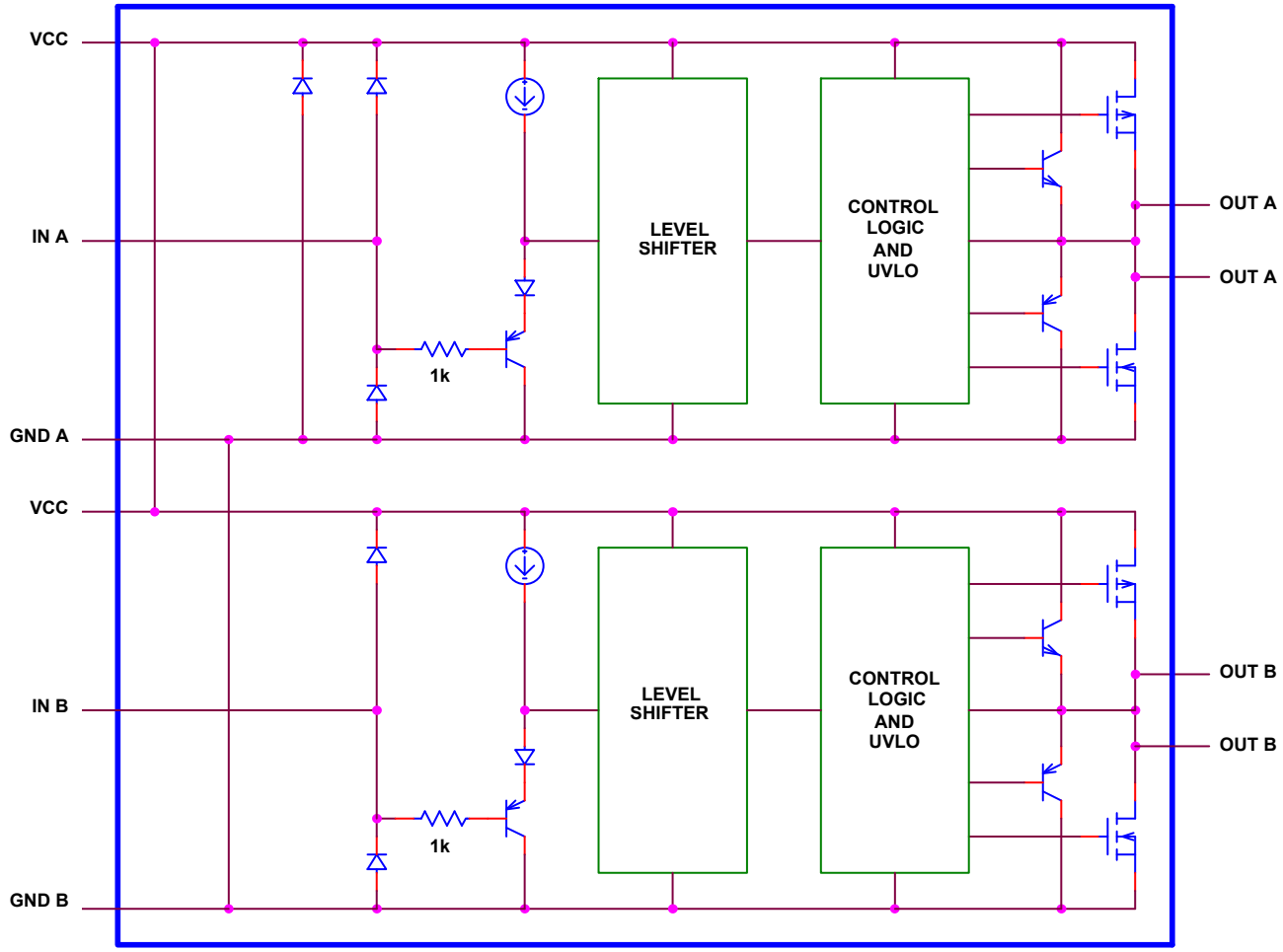


FIGURE 5. BLOCK DIAGRAM

Ordering Information

SMD NUMBER ORDERING (Note 2)	PART NUMBER (Note 1)	TEMPERATURE RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F9956005V9A	HS0-4424DRH-Q	-55 to +125	DIE	
HS0-4424DRH/SAMPLE	HS0-4424DRH/SAMPLE	-55 to +125	DIE SAMPLE	
5962F9956005VXC	HS9-4424DRH-Q	-55 to +125	16 Ld Flatpack	K16.A
HS9-4424DRH/PROTO	HS9-4424DRH/PROTO	-55 to +125	16 Ld Flatpack	K16.A
5962F9956006V9A	HS0-4424DEH-Q	-55 to +125	DIE	
5962F9956006VXC	HS9-4424DEH-Q	-55 to +125	16 Ld Flatpack	K16.A

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table must be used when ordering.

Absolute Maximum Ratings

Maximum Supply Voltage 20V
Min/Max Input Voltage . . . . . - 0.3V to V_{CC}
Output Short-circuit Duration (1 output at a time). . . . . Indefinite
ESD Rating
Human Body Model (Tested per MIL-PRF-883 3015.7). 5kV
Machine Model (Tested per MIL-PRF-883 3015.7) 200V
Charged Device Model (Tested per JESD22-C101D) 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld Flatpack Package (Notes 3, 4).	34	5

Storage Temperature Range. . . . . -65°C to +150°C
Maximum Operating Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10 secs). . . . . +265°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Supply Voltage . . . . . 8V to 18V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the package underside.

Electrical Specifications

V_{CC} = 8V, 12V, 18V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over radiation total ionizing dose.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
V_{SUPPLY}	Supply Voltage Range		**8**		**18**	V
$I_{CCSB\ LOW}$	18V Bias Current	V_S = 18V, Inputs = 0V			3.5	mA
		V_S = 18V, Inputs = 0V			**4**	mA
		V_S = 18V, Inputs = 0V, post radiation			**4**	mA
$I_{CCSB\ HIGH}$	18V Bias Current	V_S, Inputs = 18V			3.5	mA
		V_S, Inputs = 18V			**4**	mA
		V_S, Inputs = 18V, post radiation			**4**	mA
$I_{CCSB\ LOW}$	8V Bias Current	V_S = 8V, Inputs = 0V			3.5	mA
		V_S = 8V, Inputs = 0V			**4**	mA
		V_S = 8V, Inputs = 0V, post radiation			**4**	mA
$I_{CCSB\ HIGH}$	8V Bias Current	V_S, Inputs = 8V			3.5	mA
		V_S, Inputs = 8V			**4**	mA
		V_S, Inputs = 8V, post radiation			**4**	mA
I_{IL_18}	Input Current Low	V_S = 18V, Inputs = 0V	-5	0.08	5	µA
		V_S = 18V, Inputs = 0V	**-10**		**10**	µA
		V_S = 18V, Inputs = 0V, post radiation	**-10**		**10**	µA
I_{IH_18}	Input Current High	V_S, Inputs = 18V	-5	0.08	5	µA
		V_S, Inputs = 18V	**-10**		**10**	µA
		V_S, Inputs = 18V, post radiation	**-10**		**10**	µA
I_{IL_8}	Input Current Low	V_S = 8V, Inputs = 0V	-5	0.08	5	µA
		V_S = 8V, Inputs = 0V	**-10**		**10**	µA
		V_S = 8V, Inputs = 0V, post radiation	**-10**		**10**	µA
I_{IH_8}	Input Current High	V_S, Inputs = 8V	-5	0.08	5	µA
		V_S, Inputs = 8V	**-10**		**10**	µA
		V_S, Inputs = 8V, post radiation	**-10**		**10**	µA
V_{OH}	Output Voltage High	V_S = 8V, I_{OUT} = 5mA	V_S - 0.75	V_S - 0.45		V
			V_S - 0.9			V

Electrical Specifications V_{CC} = 8V, 12V, 18V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over radiation total ionizing dose. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
V_{OL}	Output Voltage Low	V_S = 8V, I_{OUT} = 5mA		0.45	0.8	V
					0.8	V
V_{OH}	Output Voltage High	V_S = 8V, I_{OUT} = 50mA	V_S - 0.95	V_S - 0.75		V
			V_S - 1.1			V
V_{OL}	Output Voltage Low	V_S = 8V, I_{OUT} = 50mA		0.75	0.95	V
					1.1	V
V_{OH}	Output Voltage High	V_S = 12V, I_{OUT} = 5mA	V_S - 0.75	V_S - 0.45		V
			V_S - 0.75			V
V_{OL}	Output Voltage Low	V_S = 12V, I_{OUT} = 5mA		0.45	0.8	V
					0.8	V
V_{OH}	Output Voltage High	V_S = 12V, I_{OUT} = 50mA	V_S - 0.95	V_S - 0.75		V
			V_S - 1.1			V
V_{OL}	Output Voltage Low	V_S = 12V, I_{OUT} = 50mA		0.75	0.95	V
					1.1	V
V_{OH}	Output Voltage High	V_S = 18V, I_{OUT} = 5mA	V_S - 0.75	V_S - 0.45		V
			V_S - 0.75			V
V_{OL}	Output Voltage Low	V_S = 18V, I_{OUT} = 5mA		0.45	0.8	V
					0.8	V
V_{OH}	Output Voltage High	V_S = 18V, I_{OUT} = 50mA	V_S - 0.95	V_S - 0.75		V
			V_S - 1.1			V
V_{OL}	Output Voltage Low	V_S = 18V, I_{OUT} = 50mA		0.75	0.95	V
					1.1	V
V_{IH_18}	Input Voltage High Threshold	V_S = 18V	3			V
			3.1			V
V_{IL_18}	Input Voltage Low Threshold	V_S = 18V			0.8	V
					0.8	V
V_{IHYS_18}	Input Voltage Threshold Hysteresis	V_S = 18V	100			mV
V_{IH_12}	Input Voltage High Threshold	V_S = 12V	3			V
			3.1			V
V_{IL_12}	Input Voltage Low Threshold	V_S = 12V			0.8	V
					0.8	V
V_{HYS_12}	Input Voltage Threshold Hysteresis	V_S = 12V	100			mV
V_{IH_8}	Input Voltage High Threshold	V_S = 8V	3			V
			3.1			V
V_{IL_8}	Input Voltage Low Threshold	V_S = 8V			0.8	V
					0.8	V
V_{HYS_8}	Input Voltage Threshold Hysteresis	V_S = 8V	100			mV
UVLO_r	Rising Undervoltage Lockout		7.2	7.5	7.8	V
			6.9		**7.95**	V
UVLO_f	Falling Undervoltage Lockout		7.1	7.45	7.75	V
			6.8		**7.9**	V
HYS_UVLO	Undervoltage Lockout Hysteresis	UVLO_r - UVLO_f		23		mV
				24		mV
Min_PW	Minimum Input Pulse Width		100			ns

Electrical Specifications V_{CC} = 8V, 12V, 18V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over radiation total ionizing dose. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
TRANSIENT RESPONSE						
t_r, t_f,	Rise Time 10% to 90% of V_{OUT}	V_S = 18V, C_L = 4300pF			75	ns
		V_S = 18V, C_L = 4300pF			**95**	ns
		V_S = 18V, C_L = 4300pF, post radiation			**95**	ns
	Fall Time 90% to 10% of V_{OUT}	V_S = 18V, C_L = 4300pF			75	ns
		V_S = 18V, C_L = 4300pF			**95**	ns
		VS = 18V, C_L = 4300pF, post radiation			**95**	ns
	Rise Time 10% to 90% of V_{OUT}	V_S = 12V, C_L = 4300pF			75	ns
		V_S = 12V, C_L = 4300pF			**95**	ns
		V_S = 12V, C_L = 4300pF, post radiation			**95**	ns
	Fall Time 90% to 10% of V_{OUT}	V_S = 12V, C_L = 4300pF			75	ns
		V_S = 12V, C_L = 4300pF			**95**	ns
		V_S = 12V, C_L = 4300pF, post radiation			**95**	ns
	Rise Time 10% to 90% of V_{OUT}	V_S = 8V, C_L = 4300pF			75	ns
		V_S = 8V, C_L = 4300pF			**95**	ns
		V_S = 8V, C_L = 4300pF, post radiation			**95**	ns
	Fall Time 90% to 10% of V_{OUT}	V_S = 8V, C_L = 4300pF			75	ns
		V_S = 8V, C_L = 4300pF			**95**	ns
		V_S = 8V, C_L = 4300pF, post radiation			**95**	ns
t_{PHL}, t_{PLH},	50% of Rising Input to 10% of Rising Output	V_S = 18V, C_L = 4300pF			200	ns
		V_S = 18V, C_L = 4300pF			**300**	ns
		V_S = 18V, C_L = 4300pF, post radiation			**300**	ns
	50% of Falling Input to 90% of Falling Output	V_S = 18V, C_L = 4300pF			200	ns
		V_S = 18V, C_L = 4300pF			**300**	ns
		V_S = 18V, C_L = 4300pF, post radiation			**300**	ns
	50% of Rising Input to 10% of Rising Output	V_S = 12V, C_L = 4300pF			250	ns
		V_S = 12V, C_L = 4300pF			**350**	ns
		V_S = 12V, C_L = 4300pF, post radiation			**350**	ns
	50% of Falling Input to 90% of Falling Output	V_S = 12V, C_L = 4300pF			250	ns
		V_S = 12V, C_L = 4300pF			**350**	ns
		V_S = 12V, C_L = 4300pF, post radiation			**350**	ns
	50% of Rising Input to 10% of Rising Output	V_S = 8V, C_L = 4300pF			300	ns
		V_S = 8V, C_L = 4300pF			**400**	ns
		V_S = 8V, C_L = 4300pF, post radiation			**400**	ns
	50% of Falling Input to 90% of Falling Output	V_S = 8V, C_L = 4300pF			300	ns
		V_S = 8V, C_L = 4300pF			**400**	ns
		V_S = 8V, C_L = 4300pF, post radiation			**400**	ns

NOTE:

5. Compliance to datasheet limits is assured by one or more methods; production test, characterization and/or design.

Typical Performance Curves

Unless otherwise specified, V_S = 8V, 12V, 18V, C_L = 4300pF, T_A = +25°C.

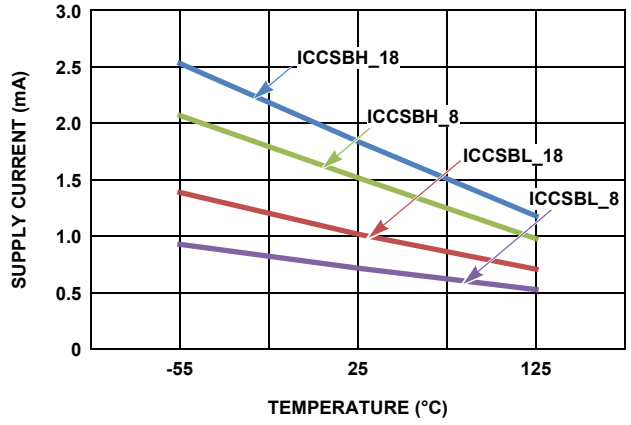


FIGURE 5. SUPPLY CURRENT vs TEMPERATURE

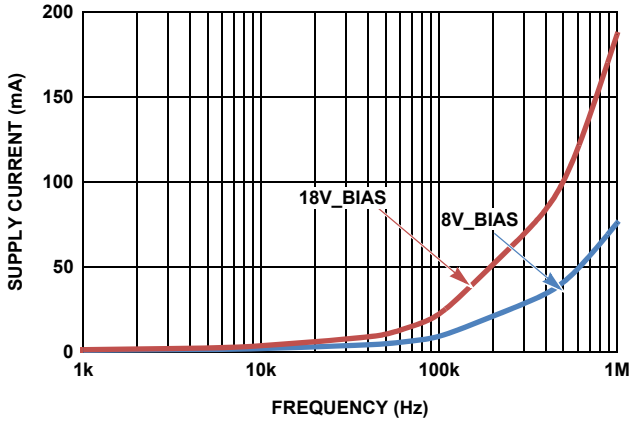


FIGURE 6. SUPPLY CURRENT vs DUAL SWITCHING AT FREQUENCY

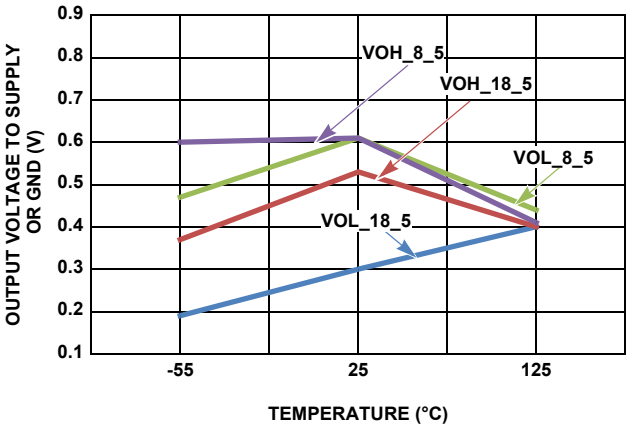


FIGURE 7. OUTPUT VOLTAGE vs TEMPERATURE (5mA)

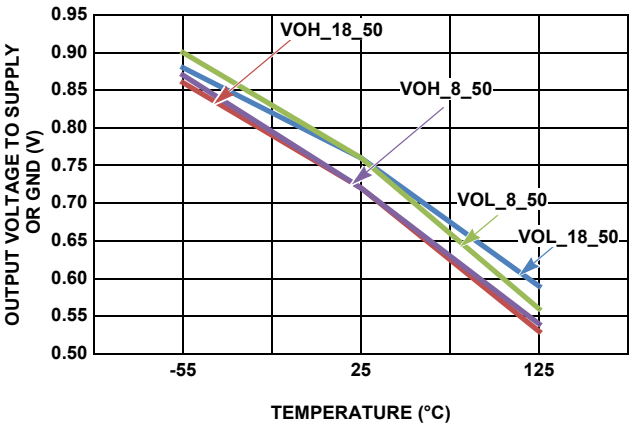


FIGURE 8. OUTPUT VOLTAGE vs TEMPERATURE (50mA)

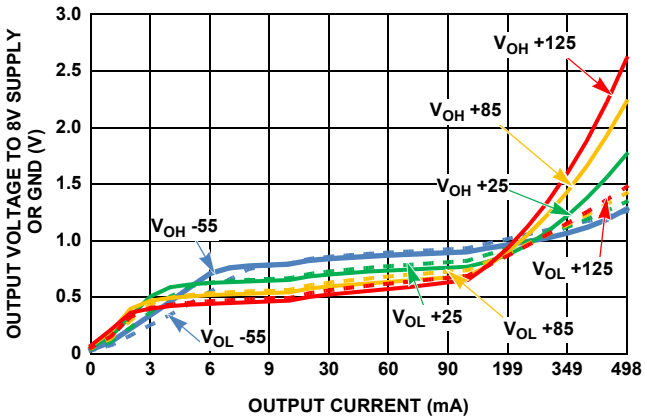


FIGURE 9. OUTPUT VOLTAGE vs OUTPUT CURRENT

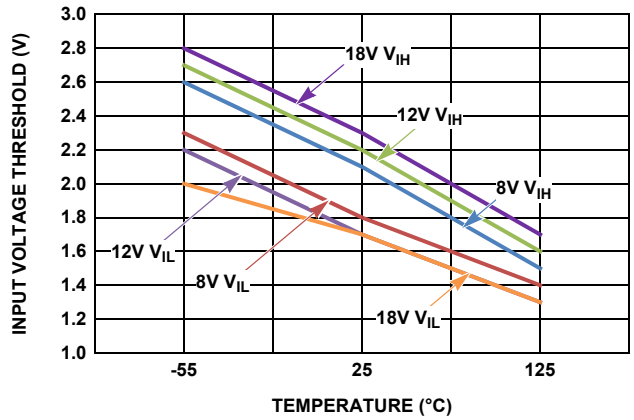


FIGURE 10. INPUT VOLTAGE THRESHOLD vs TEMPERATURE AND BIAS VOLTAGE

Typical Performance Curves

Unless otherwise specified, V_S = 8V, 12V, 18V, C_L = 4300pF, T_A = +25°C. **(Continued)**

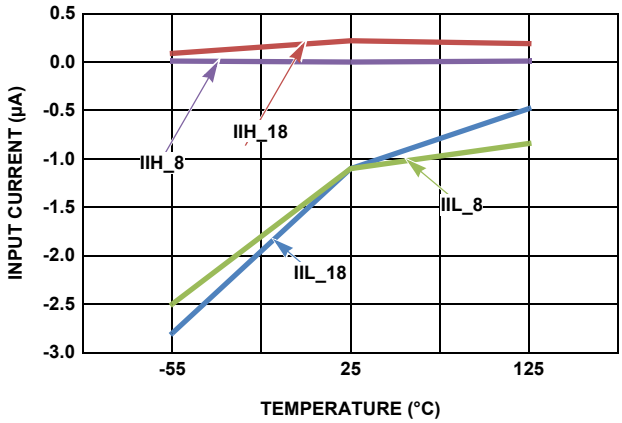


FIGURE 11. INPUT CURRENT vs TEMPERATURE AND BIAS VOLTAGE

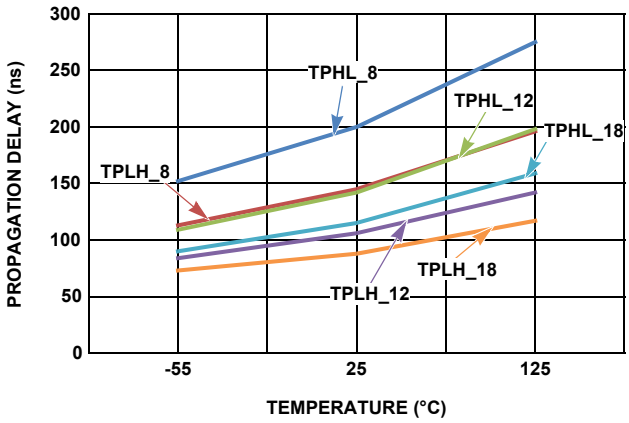


FIGURE 12. PROPAGATION DELAY vs TEMPERATURE

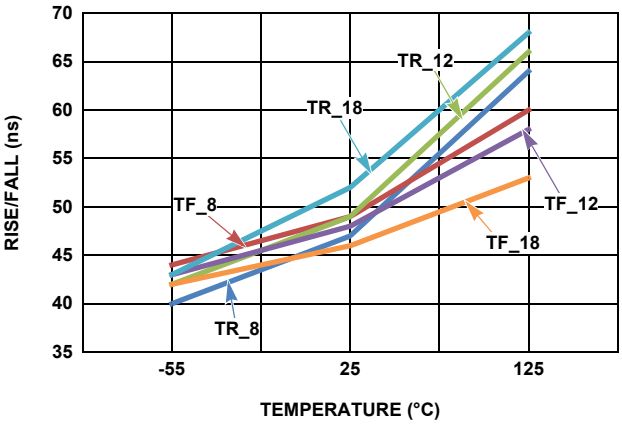


FIGURE 13. RISE/FALL TIME vs TEMPERATURE

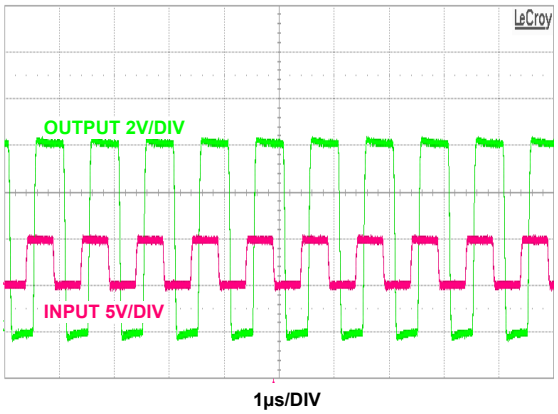


FIGURE 14. 1MHz AT 8V BIAS

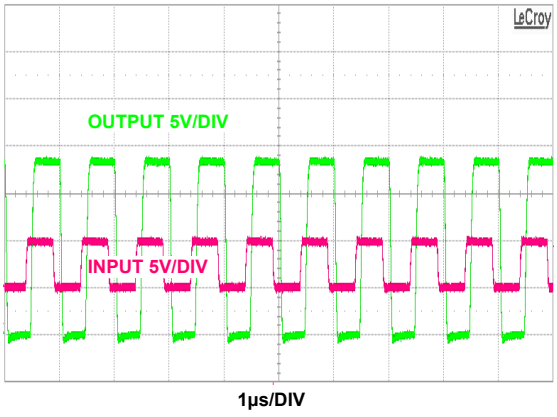


FIGURE 15. 1MHz AT 18V BIAS

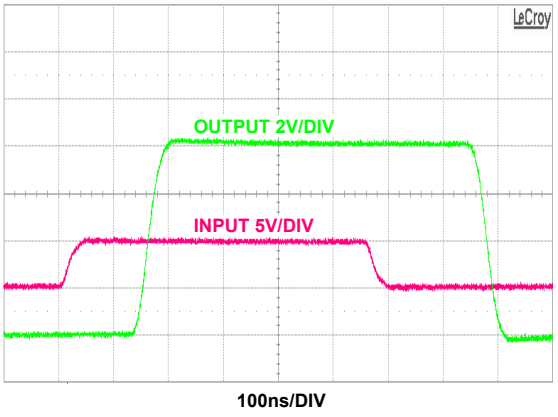


FIGURE 16. 8V RISING/FALLING PROPAGATION TIME

Typical Performance Curves

Unless otherwise specified, V_S = 8V, 12V, 18V, C_L = 4300pF, T_A = +25°C. **(Continued)**

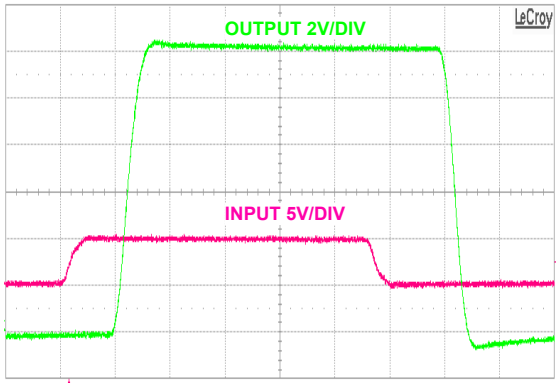


FIGURE 17. 12V RISING/FALLING PROPAGATION TIME

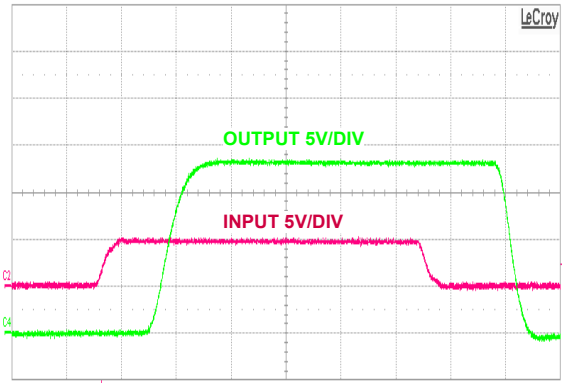


FIGURE 18. 18V RISING/FALLING PROPAGATION TIME

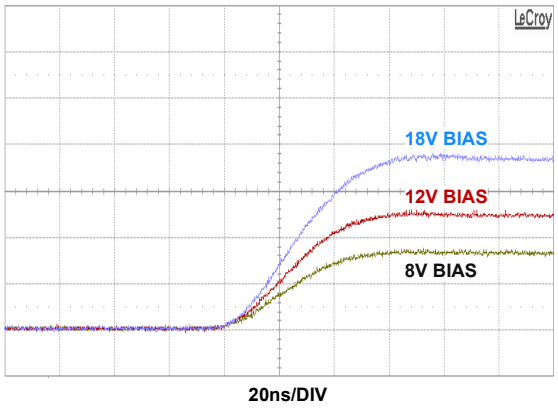


FIGURE 19. RISE TIME

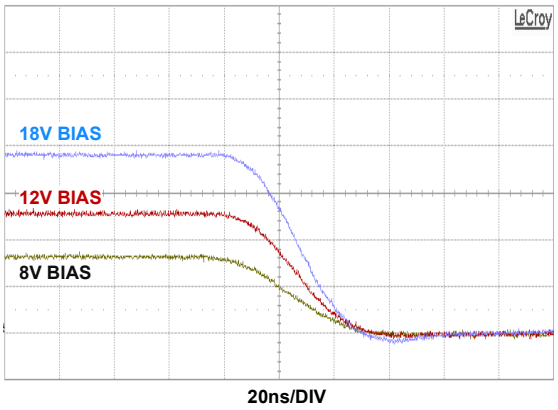


FIGURE 20. FALL TIME

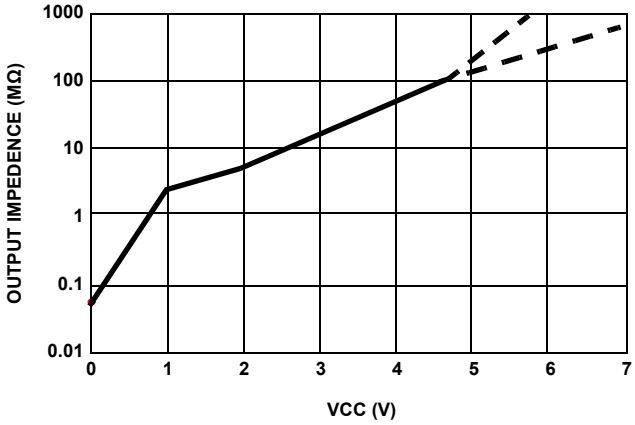


FIGURE 21. UVLO OUTPUT HIGH Z vs VCC

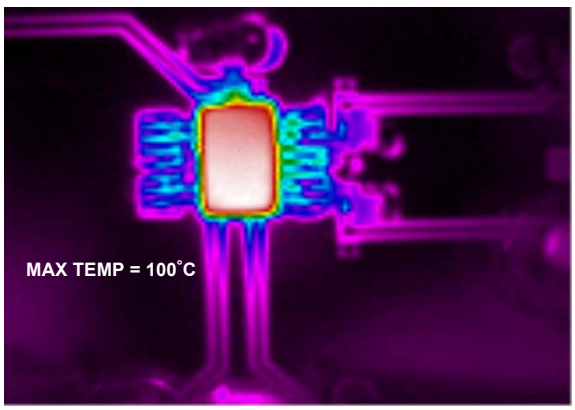


FIGURE 22. 18V, 1MHz OPERATING IR TEMP

Post High, Low Dose Rate Radiation Characteristics

Unless otherwise specified, V_S = 12V, T_A = +25°C. This data is typical mean test data post 300kRAD (Si) radiation exposure at a high dose exposure rate of 50 to 300rad(Si)/s and post 50kRAD (Si) radiation exposure at a high dose exposure rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

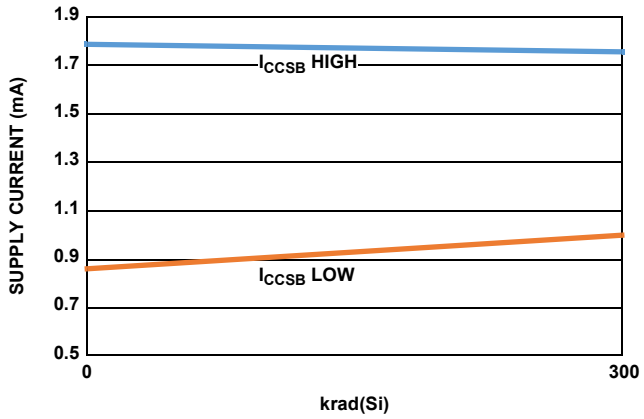


FIGURE 23. 18V SUPPLY CURRENT vs HDR RADIATION

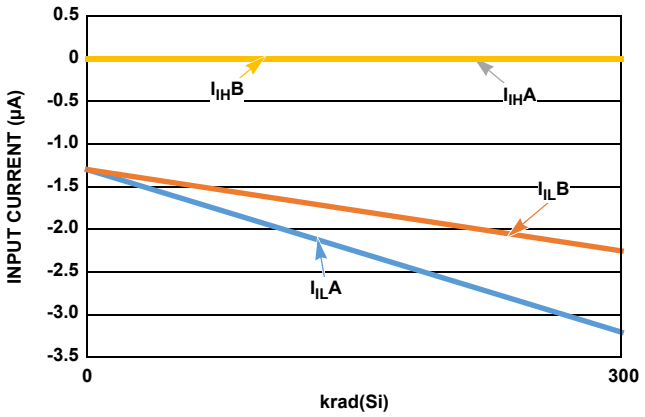


FIGURE 24. 18V INPUT CURRENT vs HDR RADIATION

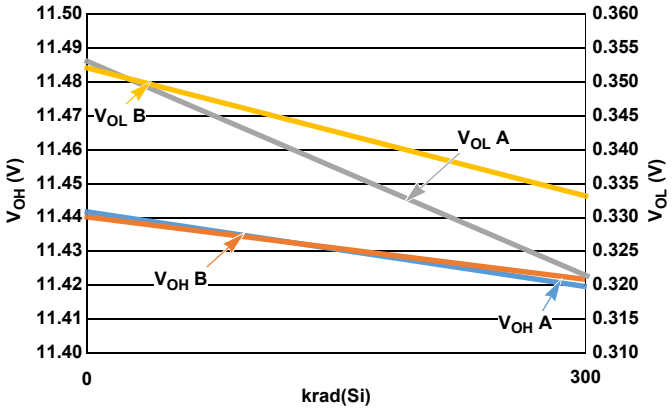


FIGURE 25. OUTPUT VOLTAGE vs HDR RADIATION

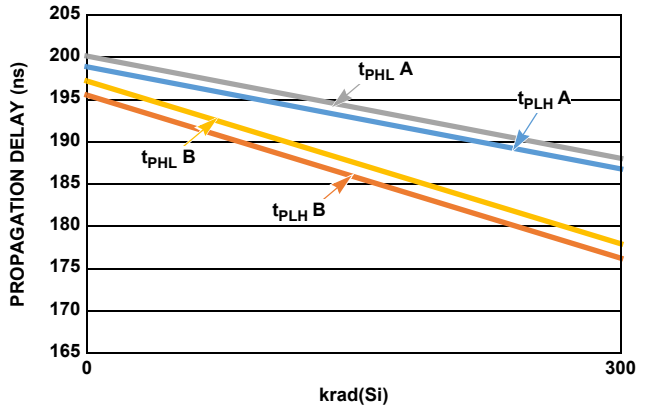


FIGURE 26. PROPAGATION DELAY vs HDR RADIATION

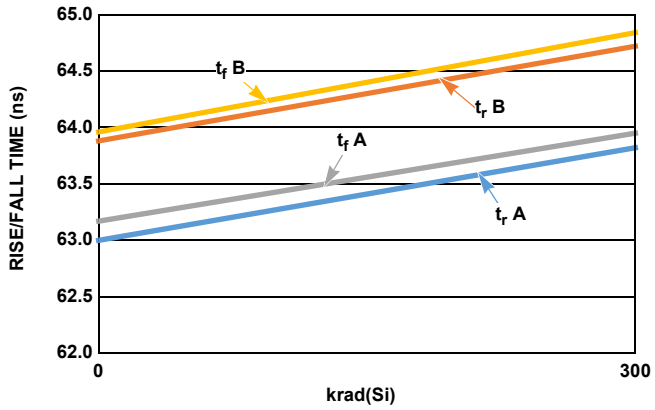


FIGURE 27. RISE/FALL TIME vs HDR RADIATION

Post High, Low Dose Rate Radiation Characteristics

Unless otherwise specified, V_S = 12V, T_A = +25°C. This data is typical mean test data post 300kRAD (Si) radiation exposure at a high dose exposure rate of 50 to 300rad(Si)/s and post 50kRAD (Si) radiation exposure at a high dose exposure rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

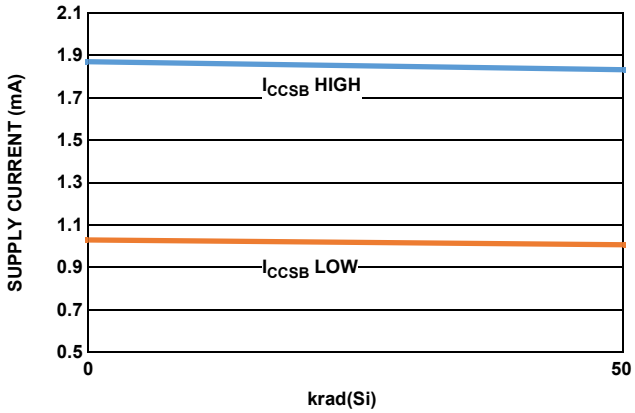


FIGURE 28. 18V SUPPLY CURRENT vs LDR RADIATION

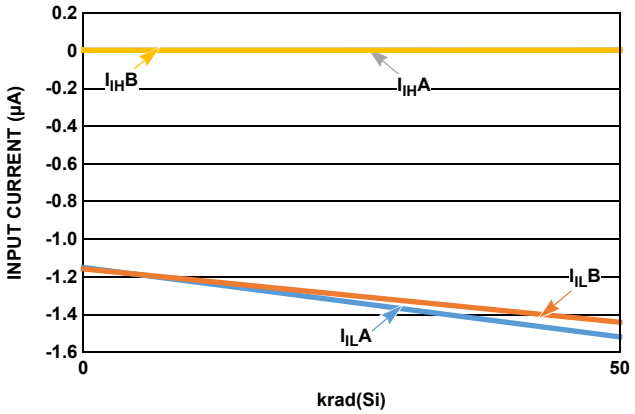


FIGURE 29. 18V INPUT CURRENT vs LDR RADIATION

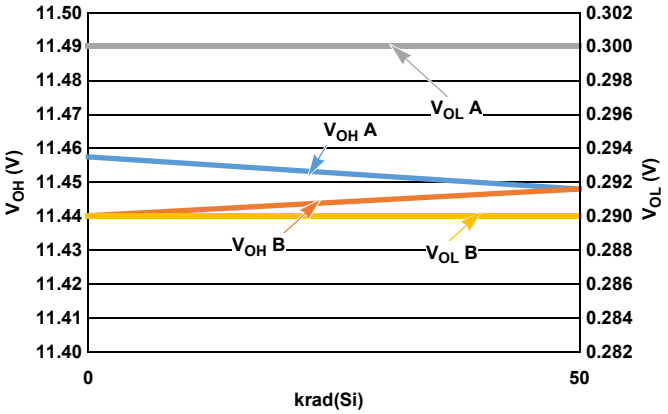


FIGURE 30. OUTPUT VOLTAGE vs LDR RADIATION

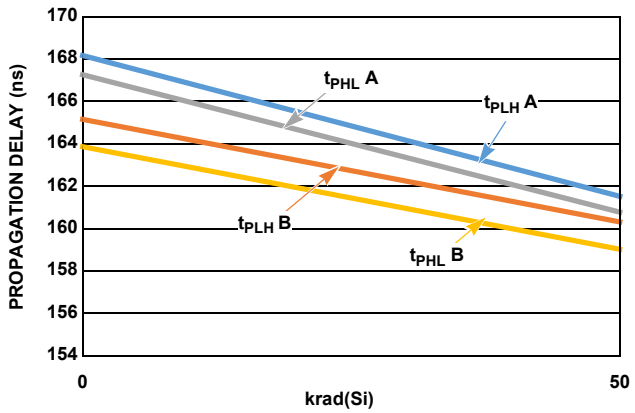


FIGURE 31. PROPAGATION DELAY vs LDR RADIATION

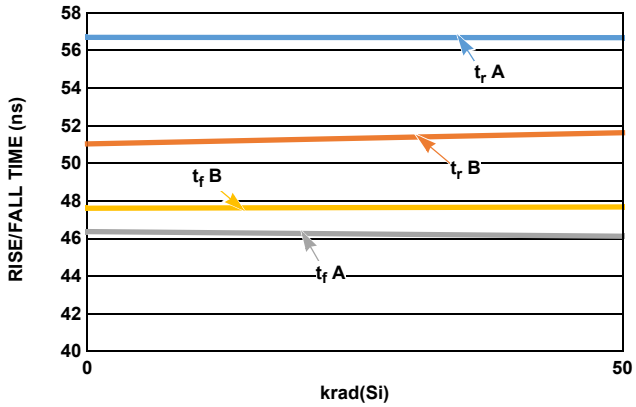


FIGURE 32. RISE/FALL TIME vs LDR RADIATION

Applications Information

Functional Description

The HS-4424DxH MOSFET drivers are designed for easy implementation with a PWM controller, such as the HS-1825ARH, as the input control signal driver. The HS-4424DxH consist of two independent drivers sharing bias voltage and ground connections at the die level.

Undervoltage Lockout and Operating Voltage Range

The HS-4424DxH have a guaranteed UVLO of <8V across the operating temperature range. All devices are recommended to operate up to and are characterized and tested at a bias of 18V. The UVLO feature ensures that the internal MOSFET drivers have sufficient gate drive to operate in their saturated mode. When in a UVLO condition the HS-4424DxH outputs are put into a high impedance tri-stated mode.

Characterization and testing occurs (as appropriate) at 8V, 12V and 18V and across the -55°C to +125°C operating temperature range.

Input Characteristics

The HS-4424DxH inputs are designed to be used with low voltage level signals (<1V for a low input level and >3V for a high input level) and also be capable of accepting input voltages up to the VCC level.

Output Buffer

The HS-4424DxH output buffers are designed to drive >2A of peak output current into high capacitance loads and can be paralleled to increase the output current capability.

The output buffer uses a final drive stage comprised of a PNP lower and NPN upper complimentary pair of transistors for the high output current drive. To enhance the pull-up and pull-down of this bipolar pair, they are each paralleled with MOS devices to do so.

Power Dissipation and Junction Temperature

It is possible to exceed the +150°C maximum recommended junction temperature under certain load and power supply conditions.

Calculate power dissipation using Equation 1;

$$Pd = V \bullet I + 2 \bullet C \bullet V^2 \bullet f \quad \text{(EQ. 1)}$$

Where

Pd = Power dissipation
V = Supply voltage
I = Operating supply current
C = Load capacitance
f = Operating frequency

Calculate junction temperature T_J using Equation 2:

$$T_J = Pd \bullet \text{Theta JC} + T_C \quad \text{(EQ. 2)}$$

Where

T_J = Junction temperature
Pd = Power dissipation
Theta JC = Junction-to-case thermal resistance
T_C = Case temperature

PCB Layout Guidelines

Use a ground plane in the PCB design, connect GND A and GND B pins directly to the ground plane in the same area, preferably close to the IC. Reference all input circuitry including IN A and IN B to a common node and reference all output circuitry including all OUT A and OUT B pins to a common node.

Bypass each VCC pin to the ground plane with a 0.047µF ceramic chip capacitor in parallel with a 4.7µF low ESR solid tantalum capacitor.

Clamp both OUT pins to VCC, each with a single diode. The 1n5819 (1A, 40V) Schottky diode is recommended.

Die Characteristics

Die Dimensions

4890µm x 3370µm (193mils x 133mils)
Thickness: 483µm ±25.4µm (19mils ±1mil)

Interface Materials

GLASSIVATION

Type: PSG (Phosphorous Silicon Glass)
Thickness: 8.0kÅ ±1.0kÅ

TOP METALLIZATION

Type: AlSiCu
Thickness: 16.0kÅ ±2kÅ

BACKSIDE FINISH

Silicon

PROCESS

Radiation Hardened Silicon Gate (DI)

Assembly Related Information

SUBSTRATE POTENTIAL

Floating (DI)

LID POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

$< 2 \times 10^5$ A/cm^2

TRANSISTOR COUNT

125

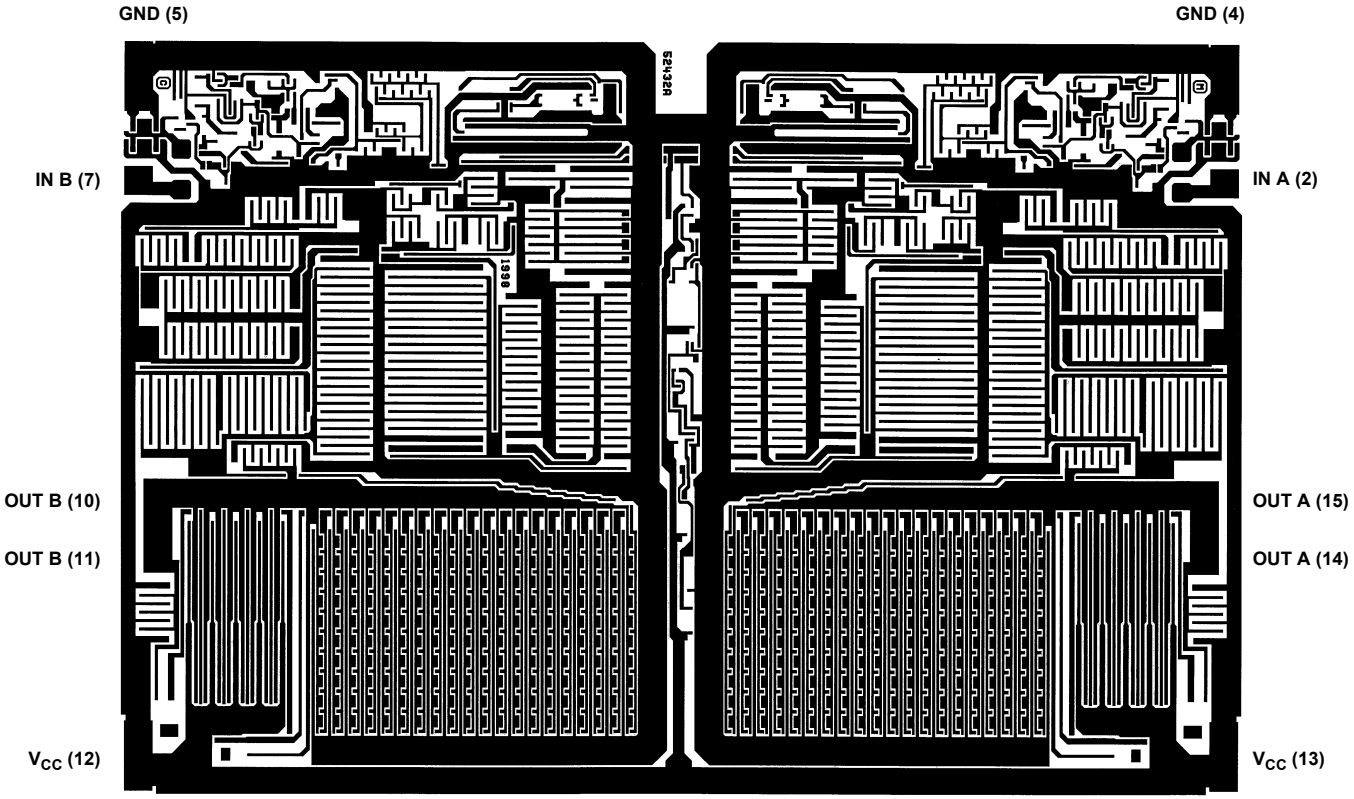
Weight of Packaged Device

0. 591 grams (typical)

Lid Characteristics

Finish: Gold
Case isolation to any lead: $20 \times 10^9 \Omega$ (minimum)

Metallization Mask Layout



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 15, 2015	FN8747.2	Added part number HS-4424DEH throughout datasheet.
July 1, 2015	FN8747.1	Abs Max ratings on page 4 - removed abs max input current and related text on page 13. ESD Ratings - changed Machine Model from: 1kV to: 200V and Charged Device Model from: 4kV to: 750V Changed over temp limits for UVLO Rising from: MIN/MAX 7.0/7.9 to: 6.9/7.95 and Falling MIN/MAX from: 6.9/7.85 to: 6.8/7.9. Changed over temp 8V, 5mA VOH limit MIN from V_S - 0.75 to V_S - 0.9.
June 8, 2015	FN8747.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

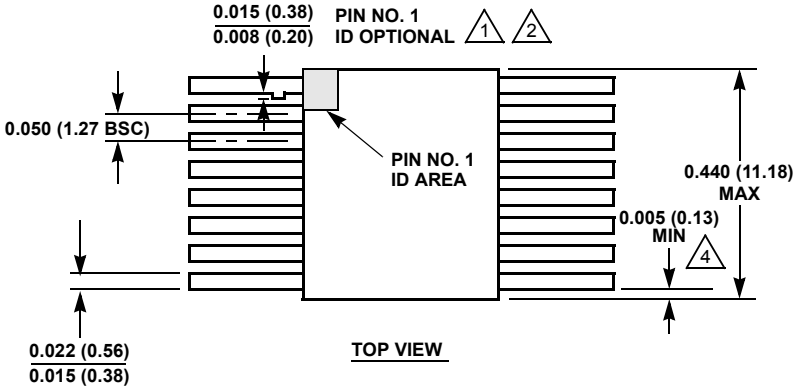
Reliability reports are also available from our website at www.intersil.com/support.

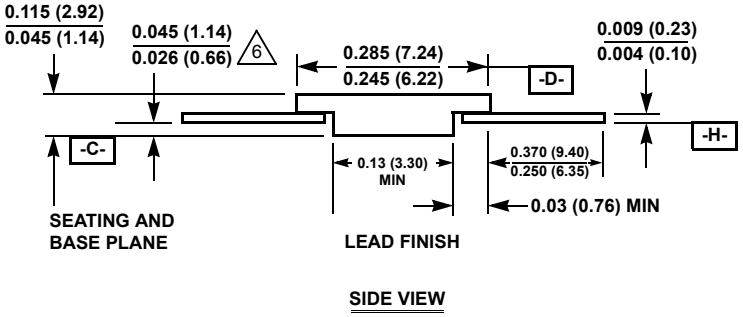
Package Outline Drawing

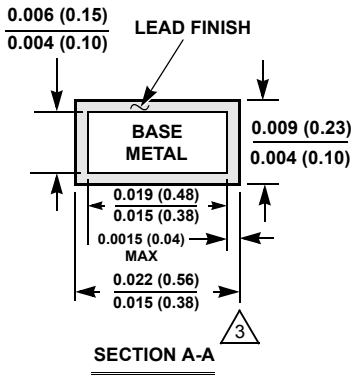
K16.A

16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 2, 1/10







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.