Advance Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt474

85 MHz Monolithic CMOS 256 x 24 Color Palette RAMDAC™

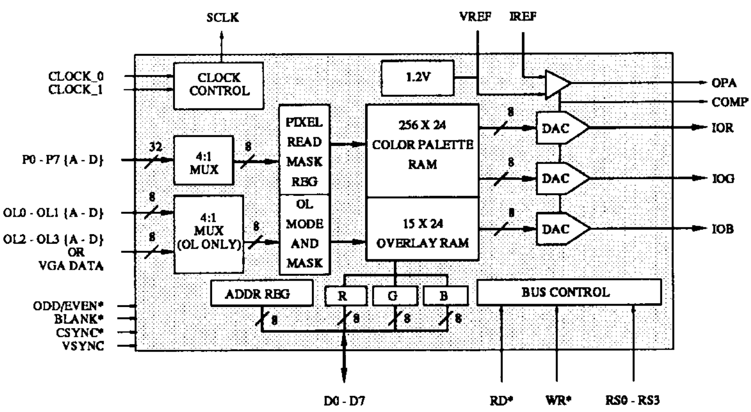
Distinguishing Features

- 85, 66 MHz Pipelined Operation
- 4:1 Multiplexed Pixel Ports
- VGA Pass-through Option via Overlays
- Triple 8-bit D/A Converters
- 256 x 24 Color Palette RAM
- 15 x 24 Overlay Color Palette
- Optional Sync on All Three Channels
- 0 or 7.5 IRE Blanking Pedestal
- Voltage or Current Reference
- Analog Output Comparators
- Anti-Sparkle Circuitry
- Power-Down Mode
- 84-pin PLCC Package

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram



Product Description

The Bt474 RAMDAC is designed specifically for high-performance color graphics.

Included are four byte-wide pixel input ports (multiplexed 4:1), a 256 x 24 color lookup table with triple 8-bit video D/A converters (configurable for either 6-bit or 8-bit D/A converter operation), and four overlay input ports (multiplexed 4:1) for supporting overlay/cursor information. The 4:1 multiplexed pixel ports ease interfacing to a high-resolution graphics frame buffer.

The Bt474 may alternately be configured for a lower performance VGA mode, where 8 bits of VGA pixel data (from a VGA controller) are input via two of the overlay input ports and displayed.

The Bt474 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt474 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM. MPU data is transferred into and out of the Bt474 via the D0–D7 data pins. The read/write timing is controlled by the RD* and WR* inputs.

The RS0–RS3 select inputs specify which control register the MPU is accessing, as shown in Tables 1 and 2. The 8-bit address register is used to address the color palette RAM, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written. Refer to Figure 15 for MPU read write timing.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the

RS0 - RS3	Access	Addressed by MPU
$0	R/W	address register (RAM write mode)
$1	R/W	color palette RAM
$2	R/W	pixel read mask register
$3	R/W	address register (RAM read mode)
$4	R/W	address register (overlay write mode)
$5	R/W	overlay registers
$6	-	reserved
$7	R/W	address register (overlay read mode)
$8	R/W	command register_0
$9	R/W	command register_1
$A	read only	ID register ($11)
$B	read only	status register
$C	-	reserved
$D	-	reserved
$E	-	reserved
$F	-	reserved

Table 1. Control Input Truth Table.

Circuit Description (continued)

RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

6-Bit / 8-Bit Operation

The command bit CR01 is used to specify whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are a logical zero.

Note that in the 6-bit mode, the Bt474's full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the two LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

Power-Down Mode

The Bt474 incorporates a power-down capability, controlled by command bit CR03. While command bit CR03 is a logical zero, the Bt474 functions normally.

While command bit CR03 is a logical one, the DACs and power to the RAM are turned off. Note that the RAM still retains the data. Also, the RAM may be read or written to by the MPU as long as the pixel clock is running. The RAM automatically powers up during MPU read/write cycles, and shuts down when the MPU access is completed. SCLK is forced into the three-state mode, bidirectional buses are forced to be inputs, the DACs output no current, and the two command registers may still be written to or read by the MPU. Note that the output DACs require about one second to turn off (sleep mode) or turn on (normal).

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				red value green value blue value
ADDR0–7 (counts binary)	$00–$FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	color palette RAM reserved overlay color 1 : overlay color 15

Table 2. Address Register (ADDR) Operation (RS3 = 0).

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Circuit Description (continued)

The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If using an external current reference, external circuitry should turn the current reference off (IREF = 0 mA) during sleep mode.

When using an external voltage reference, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption due to biasing of portions of the internal voltage reference.

Frame Buffer Clocking

The Video DRAM shift clock (SCLK) is generated by the Bt474. SCLK is 1/4 the pixel clock rate in overlay modes 2 and 3. In overlay modes 0 and 1, SCLK is equal to the pixel clock rate.

P0–P7 {A–D} are pixel data (8 bits per pixel) for four horizontally consecutive pixels. P0–P7 {A–D} are always latched on the rising edge of SCLK.

The pixel clock is specified to be either CLOCK_0 or CLOCK_1 by command bit CR12.

Frame Buffer Pixel Port Interface

There are four 8-bit pixel ports, P0–P7 {A–D}, used to interface to the frame buffer memory.

Video input data ports A through D are designated in this manner to represent the order of pixel data presentation. Port A always corresponds to the first pixel of the first line of the display. This would be the first pixel fed to the analog outputs, followed by B, then C, and finally D, repeating the pattern ABCD, ABCD, ABCD, etc. until the first scan line is completely displayed.

At this point, the output sequence is dependent on the CR05 command bit and the ODD/EVEN* input, i.e.,, whether interlaced or noninterlaced operation is selected, the current field being displayed, and whether or not an interleaved frame buffer memory is being used.

Scan line 0 is always displayed first in the interlaced mode and is considered the first line of the EVEN field. In the noninterlaced mode, scan line 1 immediately follows scan line 0. In the interlaced mode, scan line 1 is considered to be the first line of the ODD field and is displayed only after the entire EVEN field has been displayed.

Tables 3 and 4 demonstrate the display sequence. Table 3 shows the display sequence for interleaved frame buffer memory, while Table 4 shows the display sequence for noninterleaved frame buffer memory. The CR00 control bit determines whether or not the Bt474 uses an interleaved frame buffer memory configuration.

Figures 1 through 9 and Tables 3 and 4 show the interlaced and noninterlaced display timing including the interleave operation.

Pixel Read Mask

Each pixel clock cycle, P0–P7 pixel data is bit-wise logically ANDed with the contents of the pixel read mask register. The result is used to address the 256 x 24 color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters.

Circuit Description (continued)

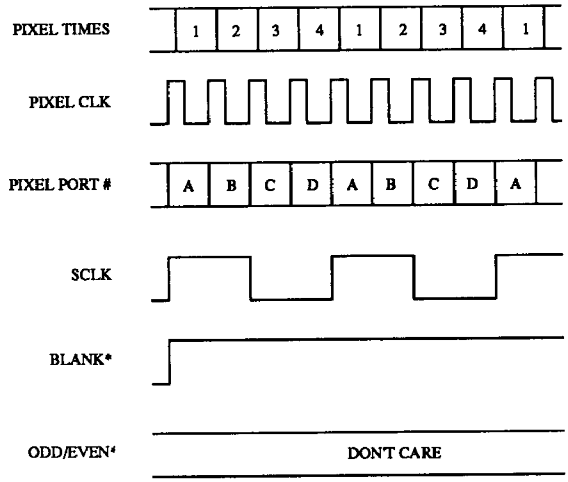

Figure 1. Timing, Interleaved (CR00 = 1), Noninterlaced (CR05 = 0), Scan Line 0.

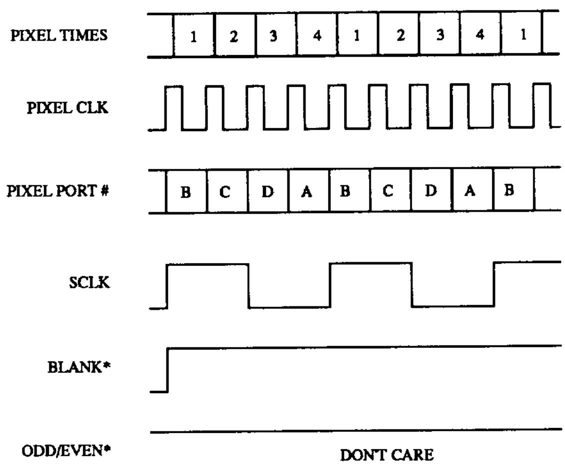

Figure 2. Timing, Interleaved (CR00 = 1), Noninterlaced (CR05 = 0), Scan Line 1.

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Circuit Description (continued)

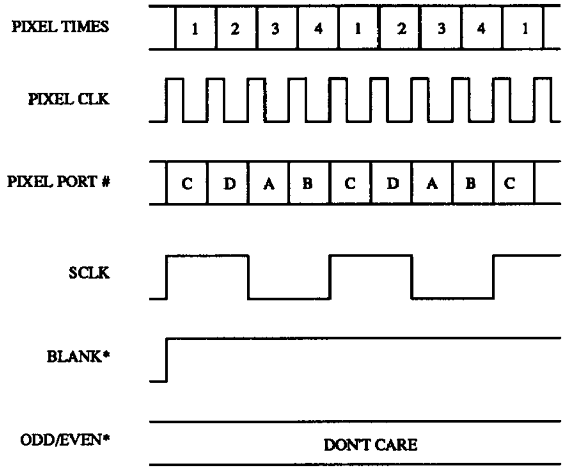

Figure 3. Timing, Interleaved (CR00 = 1), Noninterlaced (CR05 = 0), Scan Line 2.

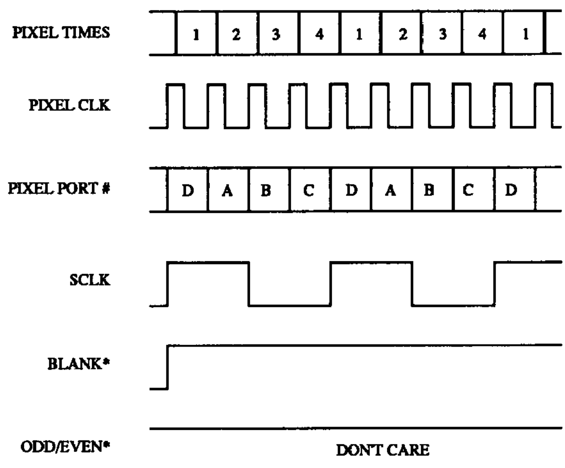

Figure 4. Timing, Interleaved (CR00 = 1), Noninterlaced (CR05 = 0), Scan Line 3.

Circuit Description (continued)

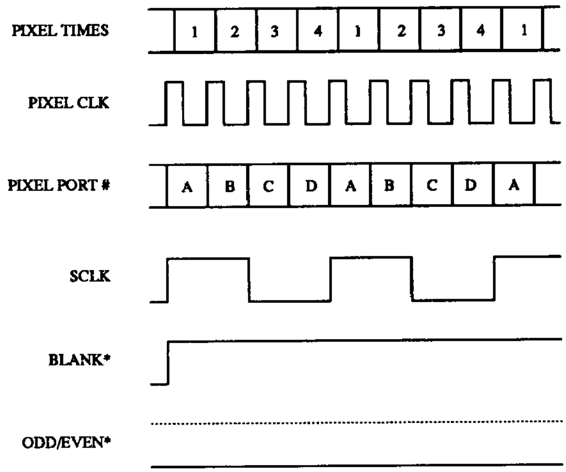

Figure 5. Timing, Interleaved (CR00 = 1), Interlaced (CR05 = 1), Even Field, Scan Line 0.

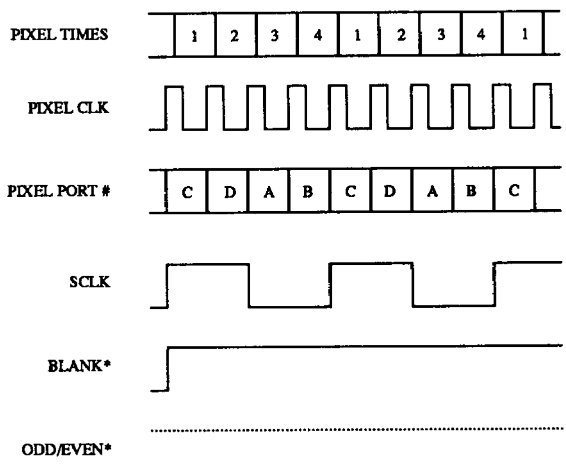

Figure 6. Timing, Interleaved (CR00 = 1), Interlaced (CR05 = 1) Even Field, Scan Line 2.

Circuit Description (continued)

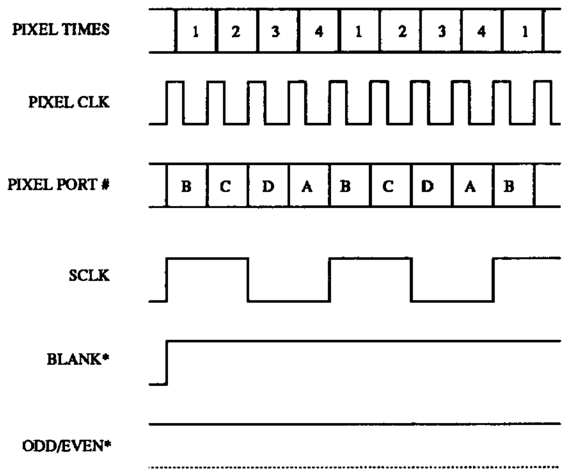

Figure 7. Timing, Interleaved (CR00 = 1), Interlaced (CR05 = 1), Odd Field, Scan Line 1.

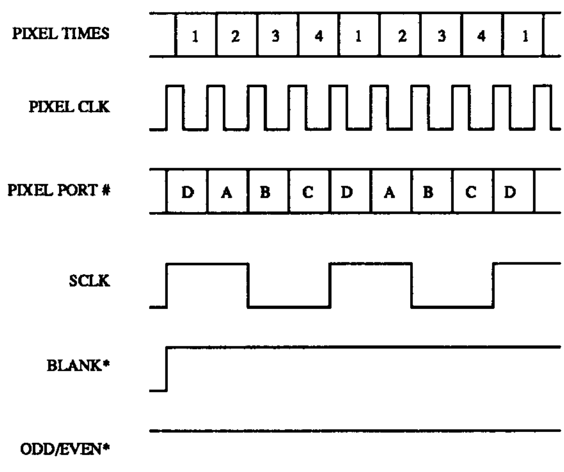

Figure 8. Timing, Interleaved (CR00 = 1), Interlaced (CR05 = 1), Odd Field, Scan Line 3.

Circuit Description (continued)

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CR05	ODD/EVEN*	Scan Line #	Pixel Port Access Sequence		
Noninterlaced					
0	x	0	ABCD	ABCD	ABCD...
0	x	1	BCDA	BCDA	BCDA...
0	x	2	CDAB	CDAB	CDAB...
0	x	3	DABC	DABC	DABC...
0	x	4	ABCD	ABCD	ABCD...
0	x	5	BCDA	BCDA	BCDA...
0	x	6	CDAB	CDAB	CDAB...
0	x	7	DABC	DABC	DABC...
Interlaced, Even Field					
1	0	0	ABCD	ABCD	ABCD...
1	0	2	CDAB	CDAB	CDAB...
1	0	4	ABCD	ABCD	ABCD...
1	0	6	CDAB	CDAB	CDAB...
Interlaced, Odd Field					
1	1	1	BCDA	BCDA	BCDA...
1	1	3	DABC	DABC	DABC...
1	1	5	BCDA	BCDA	BCDA...
1	1	7	DABC	DABC	DABC...

Table 3. Interleaved Operation (CR00 = 1).

Circuit Description (continued)

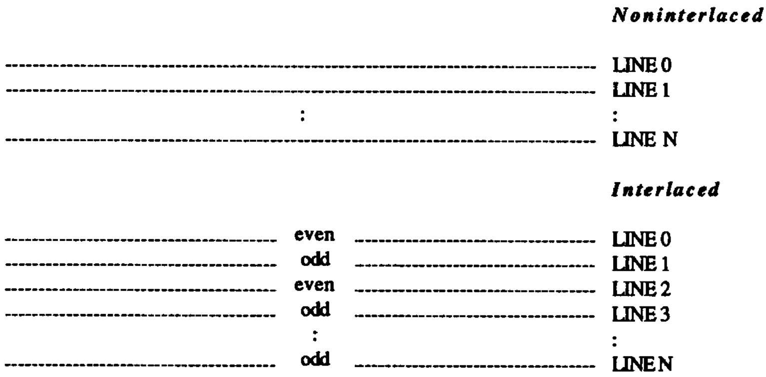

Figure 9. Interlaced / Noninterlaced Display Operation.

CR05	ODD/EVEN*	Scan Line #	Pixel Port Access Sequence		
Noninterlaced					
0	x	0	ABCD	ABCD	ABCD
0	x	1	ABCD	ABCD	ABCD
0	x	2	ABCD	ABCD	ABCD
0	x	3	ABCD	ABCD	ABCD
0	x	4	ABCD	ABCD	ABCD
0	x	5	ABCD	ABCD	ABCD
0	x	6	ABCD	ABCD	ABCD
0	x	7	ABCD	ABCD	ABCD
Interlaced, Even Field					
1	0	0	ABCD	ABCD	ABCD
1	0	2	ABCD	ABCD	ABCD
1	0	4	ABCD	ABCD	ABCD
1	0	6	ABCD	ABCD	ABCD
Interlaced, Odd Field					
1	1	1	ABCD	ABCD	ABCD
1	1	3	ABCD	ABCD	ABCD
1	1	5	ABCD	ABCD	ABCD
1	1	7	ABCD	ABCD	ABCD

Table 4. Noninterleaved Operation (CR00 = 0).

Circuit Description (continued)

Overlay Operation

The four 4-bit overlay inputs, OL0–OL3 {A–D}, are used to input overlay and other information. OL0, OL1, OL2, and OL3 inputs each have a read mask bit (CR14, CR15, CR16, and CR17, respectively). The mask bits are logically ANDed with the respective overlay bit after the overlay mode circuitry.

As shown in Table 5, the overlay inputs may be configured to operate in four different modes, as determined by the CR10 and CR11 command bits.

Note the overlay inputs are never interleaved.

Mode 0 Operation

In mode 0, the OL2 and OL3 inputs are used to input VGA pixel data from a VGA controller, while the OL0 and OL1 inputs are used to provide overlay (or a three-color cursor) information. (See Table 6.)

In this mode, the P0–P7 pixel inputs are ignored—pixel data is input using both OL2 and OL3 (as OL2 and OL3 provide a total of eight inputs, 8 bits per pixel of VGA pixel data may be input).

The selected clock input (CLOCK_0 or CLOCK_1) is output directly onto SCLK (without dividing by four) since the VGA pixel inputs will be input using a 1:1 multiplex mode. CLOCK_0 should be selected as the pixel clock while in this mode.

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Mode	CR11	CR10	OL3 {A–D}	OL2 {A–D}	OL1 {A–D}	OL0 {A–D}
0	0	0	VGA data (4 bits)	VGA data (4 bits)	cursor data	cursor data
1	0	1	VGA data (4 bits)	VGA data (4 bits)	cursor enable	cursor data
2	1	0	cursor data	cursor data	cursor data	cursor data
3	1	1	cursor enable	cursor data	cursor enable	cursor data

Table 5. Overlay Configurations.

	VGA Data		Overlay Data		
	OL3D, OL3C, OL3B, OL3A	OL2D, OL2C, OL2B, OL2A	OL1	OL0	Color Palette Addressed
No Overlay	0000	0000	0	0	color palette RAM location $00
	0000	0001	0	0	color palette RAM location $01
	:	:	:	:	:
	1111	1111	0	0	color palette RAM location $FF
3-Color Overlay	xxxx	xxxx	0	1	overlay color 1
	xxxx	xxxx	1	0	overlay color 2
	xxxx	xxxx	1	1	overlay color 3

Table 6. Mode 0 (VGA Mode, 3-Color Overlay) Overlay Configuration.

Circuit Description (continued)

	VGA Data		Overlay Data		
	OL3D, OL3C, OL3B, OL3A	OL2D, OL2C, OL2B, OL2A	OL1	OL0	Color Palette Addressed
No Overlay	0000 0000 : 1111	0000 0001 : 1111	0 0 : 0	x x : x	color palette RAM location $00 color palette RAM location $01 : color palette RAM location $FF
2-Color Overlay	xxxx xxxx	xxxx xxxx	1 1	0 1	overlay color 2 overlay color 3

Table 7. Mode 1 (VGA Mode, 2-Color Overlay) Overlay Configuration.

	Overlay Data	Video	
	OL3–OL0	P7–P0	Color Palette Addressed
No Overlay	0000 0000 : 0000	0000 0000 0000 0001 : 1111 1111	color palette RAM location $00 color palette RAM location $01 : color palette RAM location $FF
15 Color Overlay	0001 0010 : 1111	xxxx xxxx xxxx xxxx : xxxx xxxx	overlay color 1 overlay color 2 : overlay color 15

Table 8. Mode 2 (15-Color Overlay) Overlay Configuration.

	Enable	Data	Enable	Data	
	OL3	OL2	OL1	OL0	Color Palette Addressed
No Overlay	0	x	0	x	color palette RAM location specified by P0–P7
Dual 2-Color Overlays	0 0 1 1	x x 0 1	1 1 0 0	0 1 x x	overlay color 2 overlay color 3 overlay color 8 overlay color 12
Overlay Collisions	1 1 1 1	0 0 1 1	1 1 1 1	0 1 0 1	overlay color 10 overlay color 11 overlay color 14 overlay color 15

Table 9. Mode 3 (Dual 2-Color Overlays) Overlay Configuration.

Circuit Description (continued)

Mode 1 Operation

In mode 1, the OL2 and OL3 inputs are used to input VGA pixel data from a VGA controller, while the OL0 and OL1 inputs are used to provide overlay (or a two-color cursor) information. (See Table 7.)

In this mode, the P0–P7 pixel inputs are ignored —pixel data is input using both OL2 and OL3 (as OL2 and OL3 provide a total of eight inputs, 8 bits per pixel of VGA pixel data may be input).

The selected clock input (CLOCK_0 or CLOCK_1) is output directly onto SCLK (without dividing by four) since the VGA pixel inputs will be input using a 1:1 multiplex mode. CLOCK_0 should be selected as the pixel clock while in this mode.

Mode 2 Operation

In the normal overlay mode (mode 2), 4 bits of overlay (or cursor) information are used to enable 15 overlay colors to be displayed. If OL0–OL3 = 0000, P0–P7 pixel data is displayed; otherwise overlay data is displayed.

Table 8 shows the pixel and overlay color palette selection for this mode.

In this mode, OL0–OL3 {A–D} are latched on the rising edge of SCLK and have the same timing as the P0–P7 {A–D} pixel data.

SCLK is 1/4 the selected pixel clock (CLOCK_0 or CLOCK_1).

Mode 3 Operation

In mode 3, two two-color cursors may be displayed. Table 9 shows the operation of the pixel and overlay inputs in this mode. Note that OL3 and OL2 are logically ANDed together, while OL1 and OL0 are logically ANDed together. Thus, OL1 and OL3 become configured as enable bits for OL0 and OL2, respectively.

In this mode, OL0–OL3 {A–D} are latched on the rising edge of SCLK and have the same timing as the P0–P7 {A–D} pixel data.

SCLK is 1/4 the selected pixel clock (CLOCK_0 or CLOCK_1).

Video Generation

The CSYNC* and BLANK* inputs, also latched on the rising edge of SCLK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 10 and 11. Tables 10 and 11 detail how the CSYNC* and BLANK* inputs modify the output levels.

The CR04 command bit is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used. Command bit CR06 specifies whether or not the RGB outputs contain sync information.

The analog outputs of the Bt474 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

ESD and Latchup Considerations

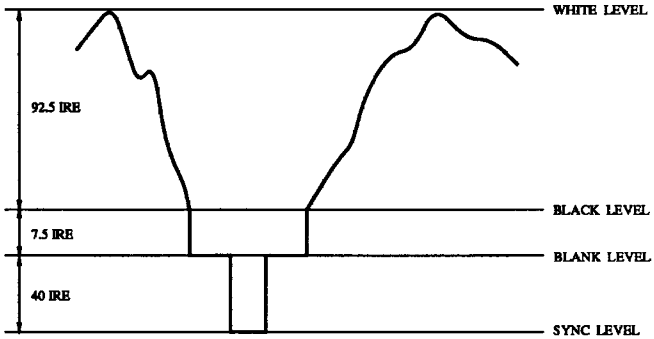
Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Circuit Description (continued)

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly terminated load, VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 10. Composite Video Output Waveforms (SETUP = 7.5 IRE).

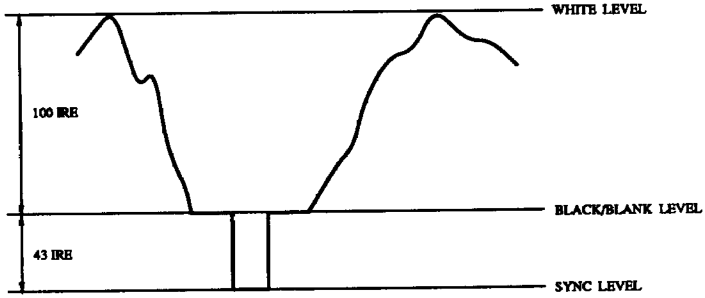
Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly terminated load, VREF = 1.235 V, RSET = 147 Ω.

Table 10. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)

NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly terminated load, VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 11. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled Iout (mA)	Sync Enabled Iout (mA)	CSYNC*	BLANK*	DAC Input Data
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly terminated load, VREF = 1.235 V, RSET = 147 Ω.

Table 11. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0, the least significant data bit.

CR07	reserved (logical one)	A logical one must be written to this bit when writing to the command register.
CR06	Sync enable (0) no sync (1) sync	This bit specifies whether the RGB outputs are to contain sync information or not.
CR05	Display mode select (0) noninterlace (1) interlace	This bit specifies whether the display is interlaced or noninterlaced and selects the appropriate interleave patterns.
CR04	Setup select (0) 0 IRE (1) 7.5 IRE	This bit specifies whether the IOR, IOG, and IOB outputs contain a 0 or 7.5 IRE blanking pedestal.
CR03	Power down enable (0) normal operation (1) reduce power	While this bit is a logical zero, the Bt474 functions normally. If this bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data and CPU reads and writes can occur with no loss of data.
CR02	Nibble swap (0) normal input (1) swap MSN and LSN	When set, this bit swaps the two nibbles of color data addressing the color palette RAM. This bit affects only pixel ports P0–P7 {A–D}.
CR01	Color value select (0) 6-bit (1) 8-bit	When set, 8-bit color data is used in the color palette RAM. When reset, 6-bit color data is used.
CR00	Interleave enable (0) no interleave (1) interleave	A logical zero inhibits the internal logic from interleaving the P0–P7 {A–D} inputs. A logical one enables the P0–P7 {A–D} inputs to be interleaved.

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0, the least significant data bit.

CR17	OL3 enable (0) force OL3 to logical zero (1) pass OL3 data	This bit is logically ANDed with OL3 data immediately after the overlay mode circuitry.
CR16	OL2 enable (0) force OL2 to logical zero (1) pass OL2 data	This bit is logically ANDed with OL2 data immediately after the overlay mode circuitry.
CR15	OL1 enable (0) force OL1 to logical zero (1) pass OL1 data	This bit is logically ANDed with OL1 data immediately after the overlay mode circuitry.
CR14	OL0 enable (0) force OL0 to logical zero (1) pass OL0 data	This bit is logically ANDed with OL0 data immediately after the overlay mode circuitry.
CR13	Test path enable (0) normal mode (1) test mode	A logical one enables certain test paths to be internally set up. This involves any input mode and any inputs which affect access to the color palette RAMs.
CR12	Clock selection (0) CLOCK_0 (1) CLOCK_1	This bit selects which pixel clock input to use.
CR11, CR10	Overlay operation select (00) mode 0 (01) mode 1 (10) mode 2 (11) mode 3	These bits select the mode of operation for the OL0–OL3 {A–D} inputs as shown in Tables 5–9. When selecting modes 0 or 1, the CLOCK_0 input should be selected to be the pixel clock.

4

Internal Registers (continued)

Pixel Read Mask Register

The 8-bit pixel read mask register may be written to or read by the MPU at any time, and is not initialized. D0 is the least significant bit. The contents of this register are bit-wise ANDed with the P0–P7 pixel data prior to addressing the color palette RAM.

ID Register

This 8-bit register may be read by the MPU at any time and contains the ID number $11. MPU write cycles to this register are ignored.

Status Register

The 8-bit status register may be read by the MPU at any time; MPU write cycles to this register are ignored. D0 is the least significant bit.

D1–D7 are always a logical zero.

D0 is the SENSE* bit. If it is a logical zero, one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This bit is used to determine the presence of a CRT monitor and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned.

The 335 mV reference has a ±5% minimum tolerance when using an external voltage reference or a ±10% tolerance when using an external current reference or the internal voltage reference.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 10 and 11. It is latched on the rising edge of SCLK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
CSYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 10 and 11). CSYNC* does not override any other control or data input, as shown in Tables 10 and 11; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of SCLK. If sync information is not to be generated on the analog outputs, this pin should be connected to GND.
VSYNC	Vertical sync control input (TTL compatible). VSYNC is sampled on the falling edge of BLANK* in the first field/frame to determine the polarity of VSYNC. If a logical one is latched, VSYNC is assumed to be an active low signal; if a logical zero is latched, VSYNC is assumed to be an active high signal.
ODD / EVEN*	Odd/even field input (TTL compatible). This input is latched on the rising edge of SCLK. This input is ignored if noninterlaced operation (command bit CR05) is selected.
CLOCK_0, CLOCK_1	Pixel clock inputs (TTL compatible). It is recommended that each clock input be driven by a dedicated buffer to avoid reflection-induced jitter.
SCLK	Shift clock output (TTL compatible). SCLK is 1/4 the pixel clock rate, except when the overlays are in the VGA mode (overlay modes 0 and 1).
P0–P7 {A–D}	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of SCLK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3 {A–D}	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information. When accessing the overlay palette, the P0–P7 {A–E} inputs are ignored. They are latched on the rising edge of SCLK. OL0 is the LSB. Unused inputs should be connected to GND.
COMP	Compensation pin. If an external or the internal voltage reference is used (Figures 12 and 13), this pin should be connected to OPA. If an external current reference is used (Figure 14), this pin should be connected to IREF. A 0.1 μF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
VREF	Voltage reference input. If an external voltage reference is used (Figure 13), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 14), this pin should be left floating, except for the bypass capacitor. A 0.1 μF ceramic capacitor is used to decouple this input to GND, as shown in Figures 12 and 13. If the VAA supply is very clean, better performance may be obtained by decoupling VREF to VAA. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When using the internal reference, this pin should not drive any external circuitry, except for the decoupling capacitor (Figure 12).
OPA	Reference amplifier output. If an external or the internal voltage reference is used (Figures 12 and 13), this pin must be connected to COMP. When using an external current reference (Figure 14), this pin should be left floating.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

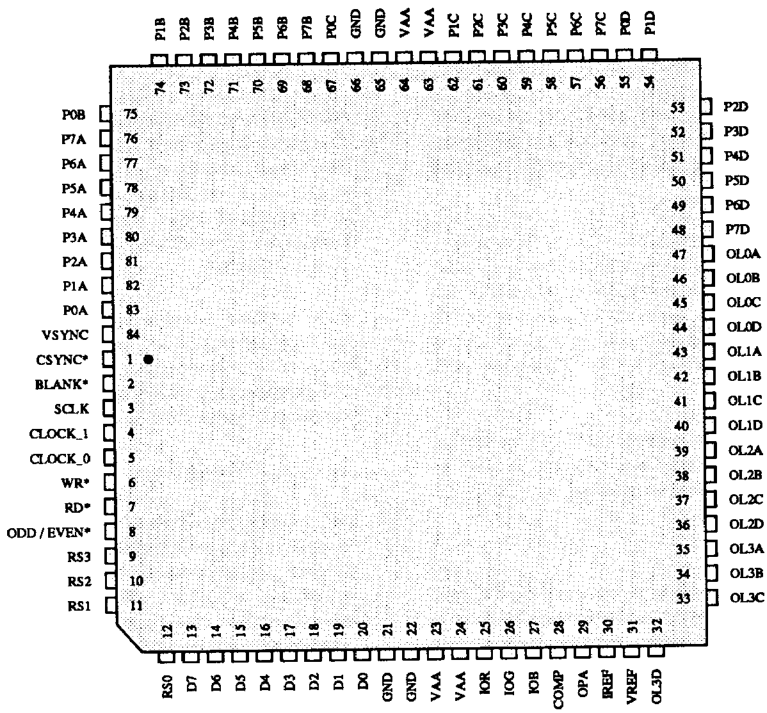
Pin Descriptions (continued)

Pin Name	Description
IREF	Full-scale adjust control. Note that the IRE relationships in Figures 10 and 11 are maintained, regardless of the full-scale output current. When using an external or the internal voltage reference (Figures 12 and 13), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is: RSET (Ω) = K * 1,000 * VREF (v) / Iout (mA) K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly terminated 75 Ω loads (i.e., RS-343A applications). When using an external current reference (Figure 14), the relationship between IREF and the full-scale output current on each output is: IREF (mA) = Iout (mA) / K

	Sync Enabled		Sync Disabled	
Setup	0 IRE	7.5 IRE	0 IRE	7.5 IRE
K=	3.025	3.195	3.000	3.170

IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figures 12, 13, and 14).
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS3 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS3 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0–RS3	Register select inputs (TTL compatible). RS0–RS3 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)



PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in Bt451/7/8 Evaluation Module Operation and Measurements, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt474 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a four-layer PC board is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt474 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt474.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and reference circuitry (if used) should be used, as shown in Figures 12, 13, and 14. Another isolated ground plane is used for the GND pins of the Bt474 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt474 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 12, 13, and 14. This bead should be located within 3 inches of the Bt474 and provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.001 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic chip capacitor. Low frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt474 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt474 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt474 to minimize reflections. Unused analog outputs should be connected to GND.

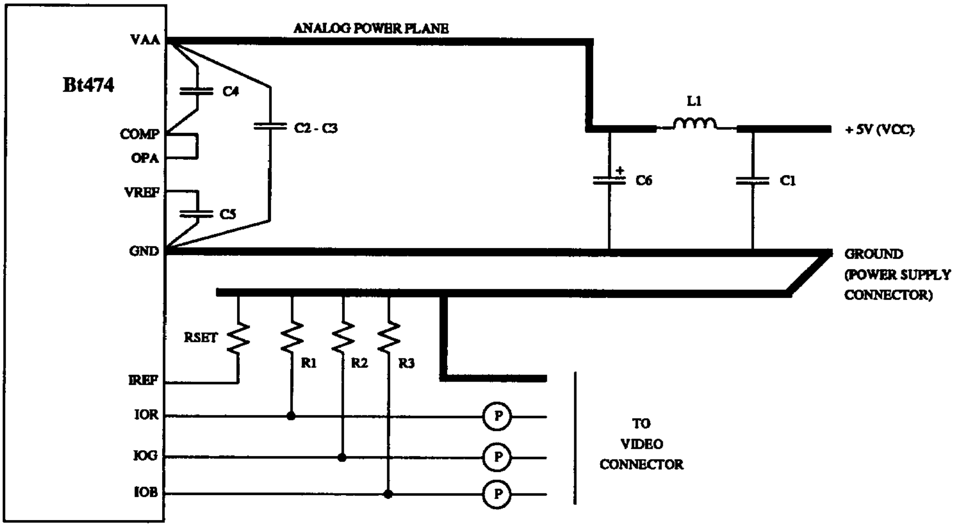
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

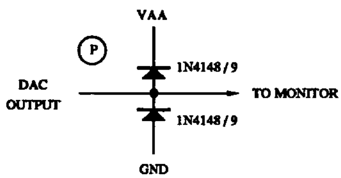
Analog Output Protection

The Bt474 analog outputs should be protected against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figures 12, 13, and 14 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



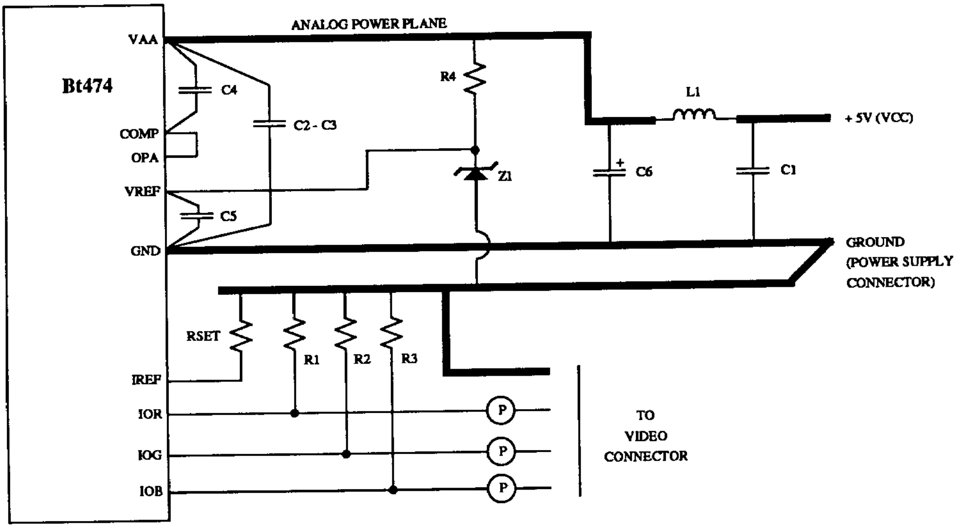


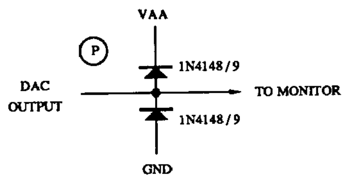
Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt474.

Figure 12. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations (continued)



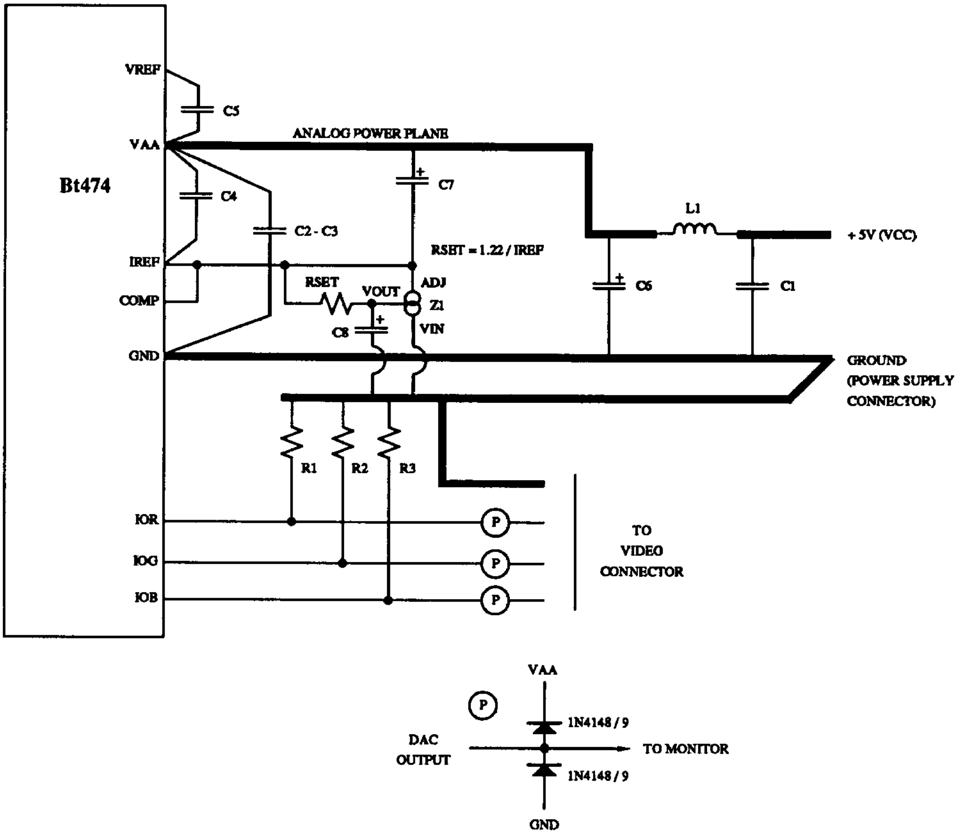


Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	147 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt474.

Figure 13. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt474.

Figure 14. Typical Connection Diagram and Parts List (External Current Reference).

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
Voltage Reference Configuration	VREF				
Reference Voltage		1.14	1.235	1.26	Volts
Current Reference Configuration	IREF				
IREF Current		-3	-8.88	-10	mA

Absolute Maximum Ratings

4

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	−1.0		+1.5	Volts
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Voltage Reference Input Current	IREF IN		10		µA
Power Supply Rejection Ratio** (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with SETUP = 7.5 IRE, RSET = 147 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note: When using the internal voltage reference, RSET may need to be adjusted to meet these limits. Also, the "gray-scale" output current (white level relative to black) will have a typical tolerance of ±10% rather than the ±5% specified above.

*In the 6-bit mode, the output levels are approximately 1.5% lower than these values.

**Guaranteed by characterization, not tested.

AC Characteristics

Parameter	Symbol	85 MHz Devices			66 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
CLOCK_0, CLOCK_1 Rate	Fmax			85			66	MHz
RS0–RS3 Setup Time	1	10			10			ns
RS0–RS3 Hold Time	2	10			10			ns
RD* Asserted to D0–D7 Driven	3	2			2			ns
RD* Asserted to D0 -D7 Valid	4			40			40	ns
RD* Negated to D0–D7 3-Stated	5			20			20	ns
Read D0–D7 Hold Time	6	2			2			ns
Write D0–D7 Setup Time	7	10			10			ns
Write D0–D7 Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*pclk			6*pclk			ns
Setup Time (4:1 Mux Mode)	11	3			3			ns
P0–P7 and OL0–OL3 {A–D},								ns
CSYNC*, VSYNC, BLANK*,								
ODD/EVEN*								ns
Hold Time (4:1 Mux Mode)	12	3			3			ns
P0–P7 and OL0–OL3 {A–D},								ns
CSYNC*, VSYNC, BLANK*,								
ODD/EVEN*								ns
SCLK High Time (4:1 Mux Mode)	13	15			20			ns
SCLK Low Time (4:1 Mux Mode)	14	15			20			ns
SCLK Output Delay	15	4			4			ns
CLOCK_0, CLOCK_1 Low Time	16	4			5			ns
CLOCK_0, CLOCK_1 High Time	17	4			5			ns
CLOCK_0, CLOCK_1 Cycle Time	18	11.7			15.15			ns
Setup Time (1:1 Mux Mode)	19	3			3			ns
OL0A, OL1A, OL2–OL3 {A–D},								
CSYNC*, VSYNC, BLANK*,								
ODD/EVEN*								
Hold Time (1:1 Mux Mode)	20	3			3			ns
OL0A, OL1A, OL2–OL3 {A–D},								
CSYNC*, VSYNC, BLANK*,								
ODD/EVEN*								

Test conditions on next page.

AC Characteristics (continued)

Parameter	Symbol	85 MHz Devices Min	85 MHz Devices Typ	85 MHz Devices Max	66 MHz Devices Min	66 MHz Devices Typ	66 MHz Devices Max	Units
Analog Output Delay	21			30			30	ns
Analog Output Rise/Fall Time	22		3			3		ns
Analog Output Settling Time*	23		12			14		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			150			150		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		5	5	5	5	5	5	Clocks
VAA Supply Current**	IAA							
Normal Operation			170	tbd		170	tbd	mA
"Sleep" Mode***			10	tbd		10	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with SETUP = 7.5 IRE, VREF = 1.235 V, RSET = 147 Ω. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF; D0–D7 output load ≤ 75 pF. SCLK output load = 80 pF. See timing notes in Figures 16 and 17. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

***External current or voltage reference disabled during sleep mode.

Note: "pclk" symbol refers to either CLOCK_0 or CLOCK_1 cycle time, whichever is selected.

Timing Waveforms

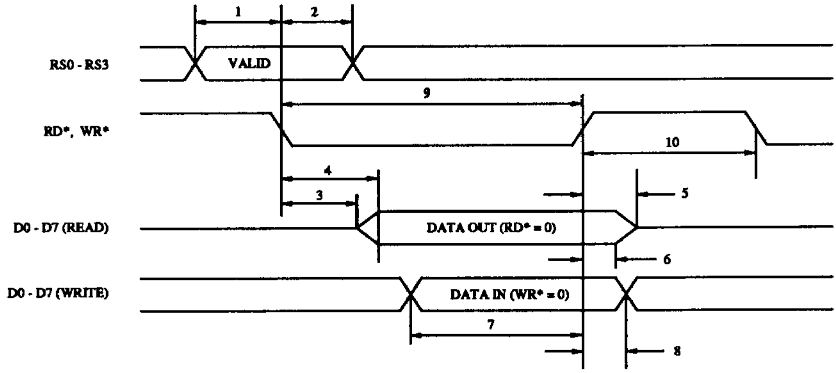
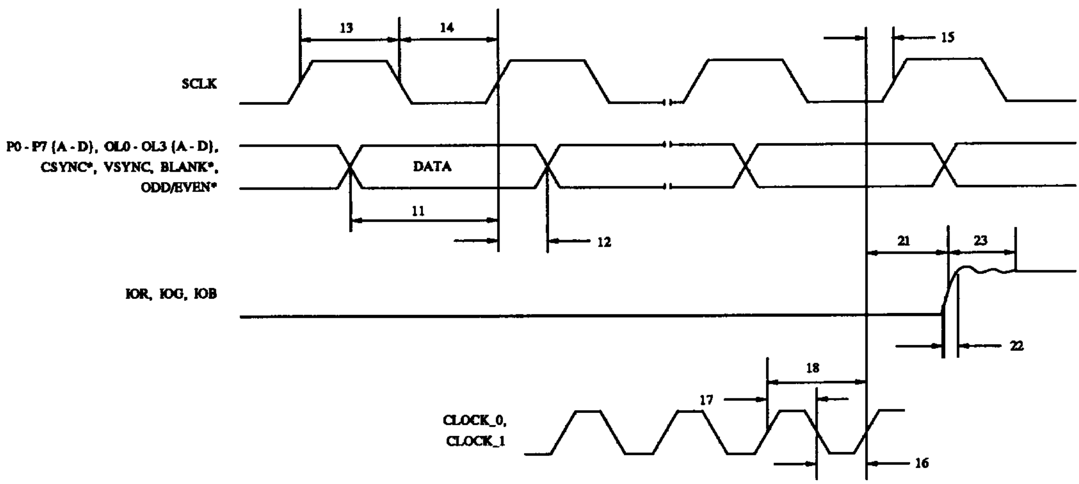


Figure 15. MPU Read/Write Timing.



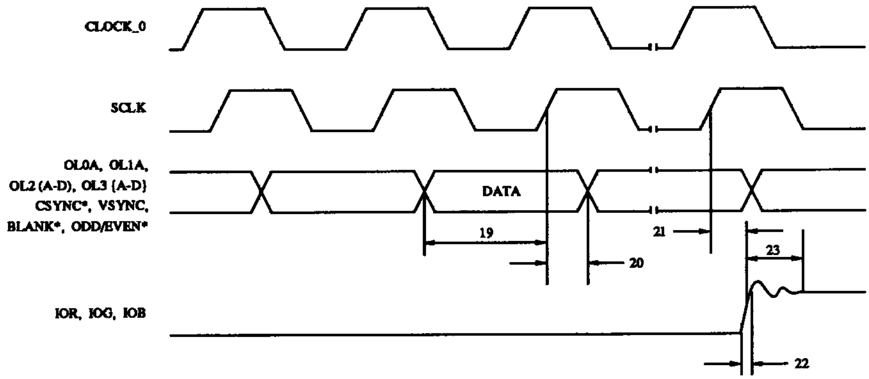
Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 16. Video Input/Output Timing.

Timing Waveforms (continued)



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 17. Video Input/Output Timing (VGA Modes Operation).

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt474KPJ85	85 MHz	84-pin Plastic J-Lead	0° to +70° C
Bt474KPJ75	66 MHz	84-pin Plastic J-Lead	0° to +70° C

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Revision History

Datasheet Revision	*Change from Previous Revision*
B	Changed speed grade listing from 75 MHz to 66 MHz. Revised PCB layout section.