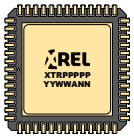
XTR25010

High Temperature Power Gate Driver

Rev 3 – August 2021 (DS-00395-13)

Data Sheet

PRODUCTION



LJCC52

XTR25011

FEATURES

- Operational beyond the -60°C to +230°C temperature range.
- High voltage supply from 7V to 35V.
- Low voltage supply from 4.5V to 5.5V
- Integrated charge-pump inside pull-up drivers allowing 100% duty-cycle PWM control signal.
- Double pull-up drivers with combined 8A peak and 2A continuous current capability at T_C=230°C.
- Two pull-down drivers with 3A peak current capability at T_C=230°C for each driver.
- Nonoverlapped pull-up and pull-down outputs.
- Enable input signal for driver outputs reset.
- Latch-up free.
- Ruggedized SMT packages and also available as bare die.

APPLICATIONS

- Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- Intelligent Power Modules (IPM).
- Power inverters.
- Power conversion and motor drive.
- DC-DC converters and switched mode power supplies.

DESCRIPTION

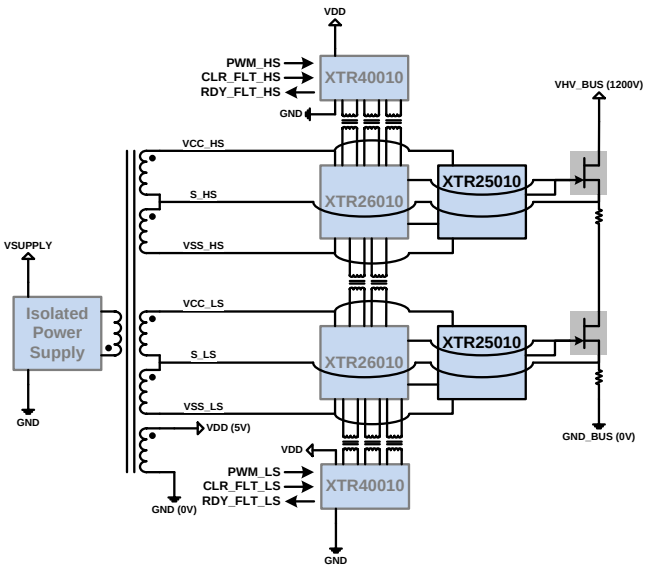
XTR25010 is a high-temperature, high reliability power transistor driver integrated circuit designed to drive normally ON and normally-OFF power transistors in Silicon Carbide (SiC), Gallium Nitride (GaN) and standard silicon, including JFETs, MOSFETs, BJTs, SJTs and MESFETs.

For turning on the power transistors, the XTR25010 includes two independent pull-up gate-drive-channels (PU_DR1 and PU_DR2) capable of sourcing 4A at 230°C peak current each. For turning off the power transistors, the XTR25010 includes two pull-down gate-drive-channels capable of sinking 3A at 230°C peak current each (PD_DR and PD_MC).

For driving wide bandgap transistors, it is recommended to use XTR25010 as a power stage extension for the XTR26010, which generates the needed control signals and additional protection functions (see XTR26010 datasheet and application note for more details).

XTR25010 can also be used standalone as a half-bridge driver for DC-DC converters and motor drive.

PRODUCT HIGHLIGHT



ORDERING INFORMATION

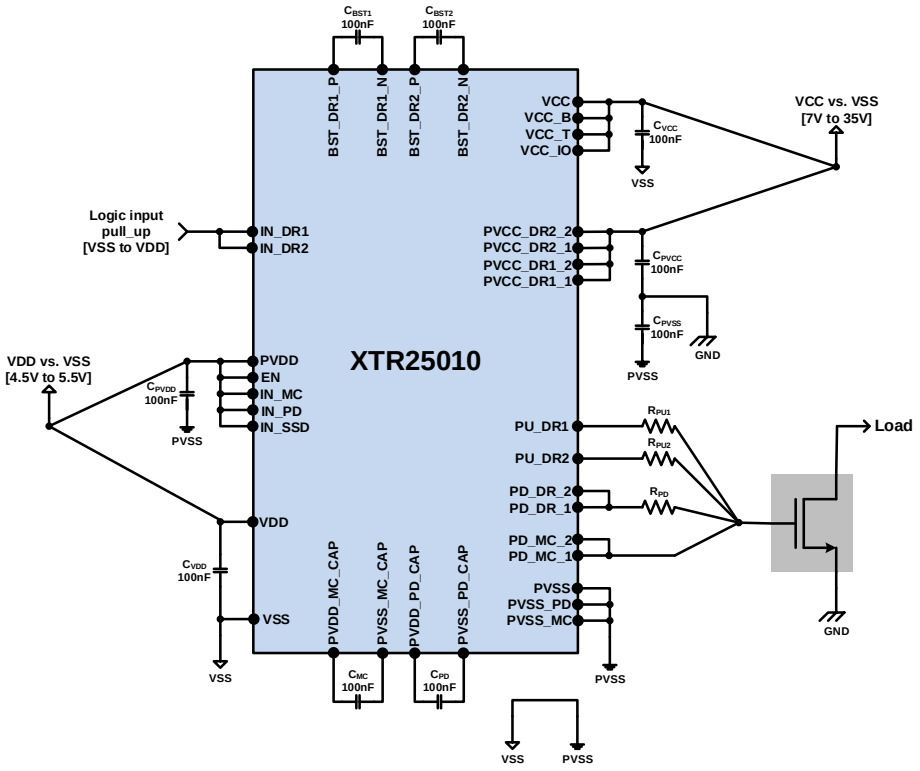
X	TR	25	010
Source: X = X-REL Semi	Process: TR = HiTemp, HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR25010-TD	-60°C to +230°C	Bare die		
XTR25011-LJ	-60°C to +230°C	Ceramic LJCC52	52	XTR25011

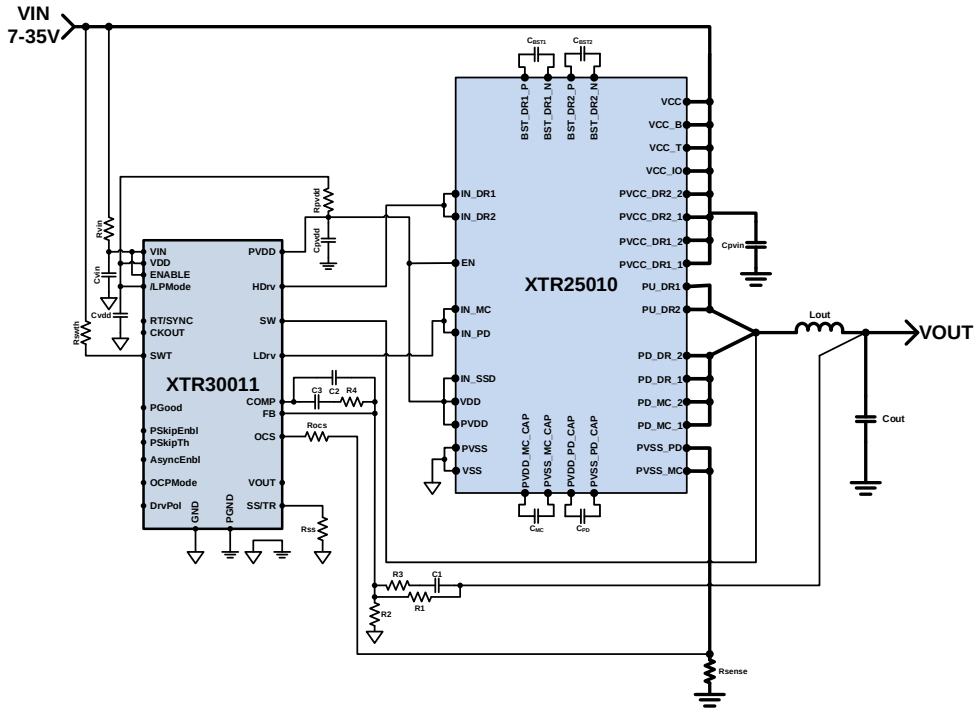
Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

TYPICAL APPLICATIONS

Power Transistor Driver



Step-down (Buck) DC-DC Converter



ABSOLUTE MAXIMUM RATINGS

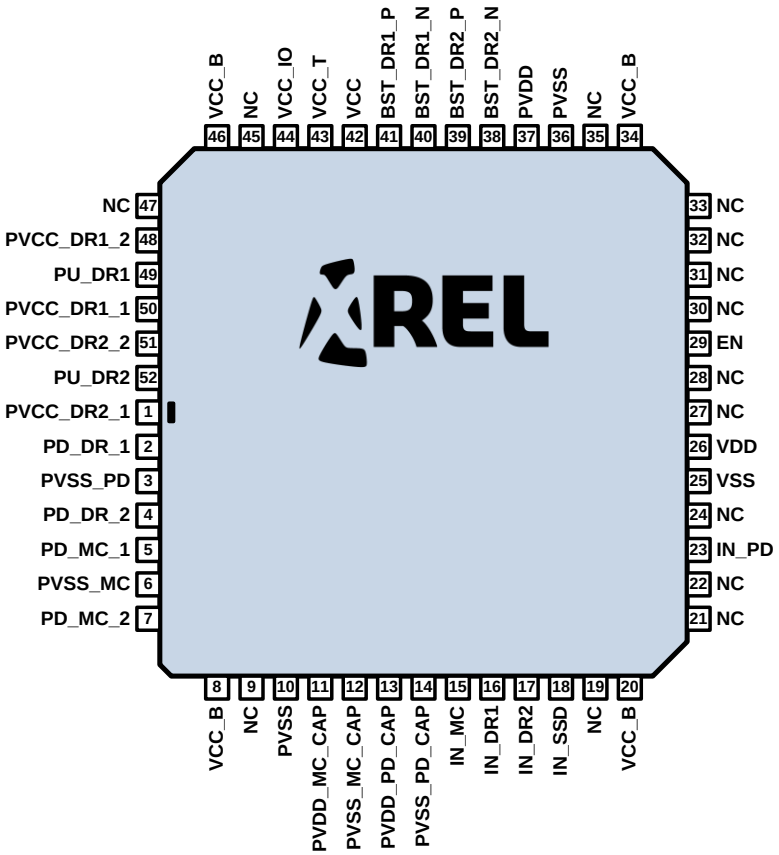
Supply voltage	VCC_IO-PVSS	-0.5V to 40V
	VCC, VCC_B, VCC_T, and PVCC_DRx_x	PVSS-0.5V to VCC_IO+0.5V
	PVDD-PVSS	-0.5V to 5.5V
	VDD, PVDD_PD_CAP and PVDD_MC_CAP	PVSS-0.5V to PVDD+0.5V
	VSS, PVSS_MC, PVSS_PD	PVSS-0.5V to PVSS+0.5v
Inputs pins	EN, IN_SSD, IN_DR1, IN_DR2, IN_MC and IN_PD	PVSS-0.5V to PVDD+0.5V
Outputs pins	PD_MC_x and PD_DR_x	PVSS-0.5V to VCC_IO+0.5V
	PU_DR1	PVSS-0.5V to PVCC_DR1+0.5V
	PU_DR2	PVSS-0.5V to PVCC_DR2+0.5V
Bootstrap pins	BST_DRx_P versus BST_DRx_N	-0.5V to 6V
Storage Temperature Range		-70°C to +230°C
Operating Junction Temperature Range		-70°C to +300°C
ESD Classification		1kV HBM MIL-STD-883

Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

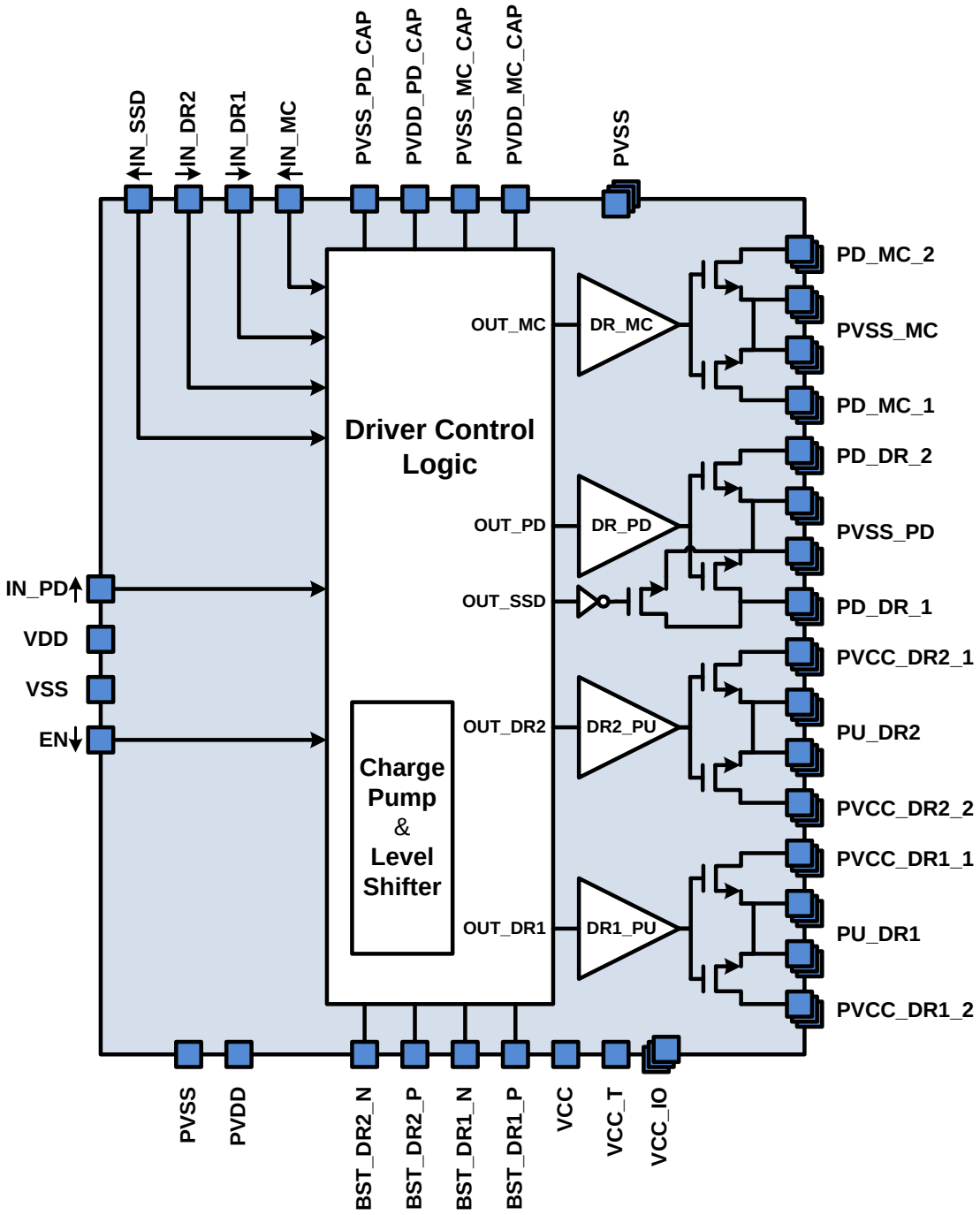
PACKAGING

J-formed Leaded Chip Carrier LJCC52
XTR25011-LJ

Top view



BLOCK DIAGRAM



Die level block diagram showing all available functionalities and bond-pads. Arrows aside pad names indicate whether the input is internally pulled up or down by default (with about 100kΩ strength).

PIN DESCRIPTION

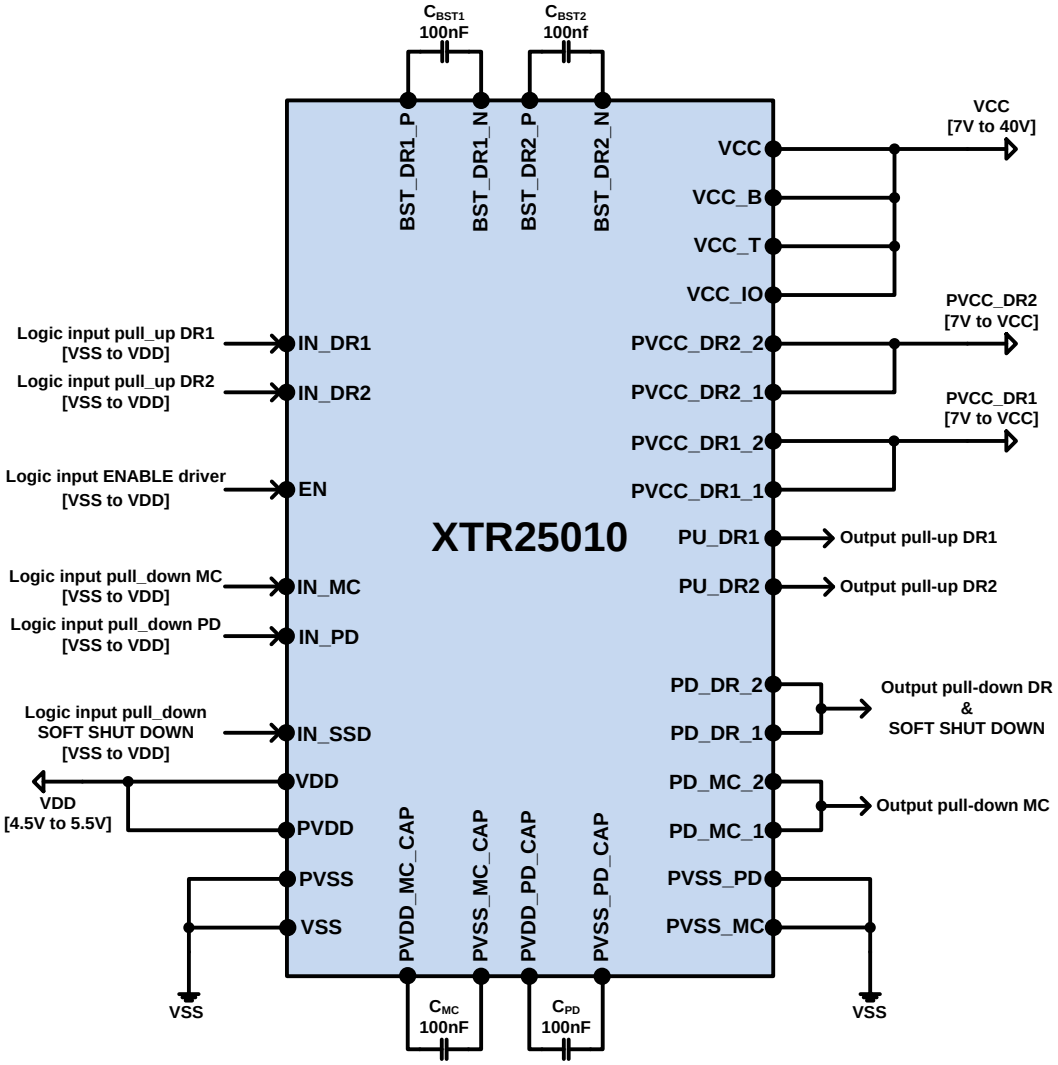
XTR25011		
Pin Number	Name	Description
1	PVCC_DR2_1	Positive supply voltage of PU_DR2 driver (PVCC_DR2). Connect together with PVCC_DR2_2 and decouple with respect to PVSS with a capacitor of at least 100nF.
2	PD_DR_1	Connect to output of the pull-down driver PD_DR_2.
3	PVSS_PD[1]	Negative power supply of PD driver. Connect to PVSS plane.
4	PD_DR_2	Connect to output of the pull-down driver PD_DR_1.
5	PD_MC_1	Connect to Miller Clamp pull-down driver PD_MC_2
6	PVSS_MC[1]	Negative power supply of MC driver. Connect to PVSS plane.
7	PD_MC_2	Connect to Miller Clamp pull-down driver PD_MC_1
8	VCC_B	Connect to VCC plane.
9	NC	No internal connection.
10	PVSS[1]	Negative power supply of power IOs. Connect to PVSS plane.
11	PVDD_MC_CAP	Top plate of bypassing capacitor (100nF typ) of the Miller clamp (MC) pre-driver. This pin is internally connected to PVDD.
12	PVSS_MC_CAP	Bottom plate of bypassing capacitor (100nF typ) of the Miller clamp (MC) pre-driver. This pin is internally connected to PVSS_MC. Do not connect to VSS plane.
13	PVDD_PD_CAP	Top plate of bypassing capacitor (100nF typ) of the pull-down (PD) pre-driver. This pin is internally connected to PVDD.
14	PVSS_PD_CAP	Bottom plate of bypassing capacitor (100nF typ) of the pull-down (PD) pre-driver. This pin is internally connected to PVSS_PD_1/PVSS_PD_2. Do not connect to VSS plane.
15	IN_MC	Digital schmitt triggered input control signal of Active Miller Clamp pull-down driver PD_MC (0/5V vs. VSS). Internally pulled-up to PVDD with equivalent 100kΩ strength.
16	IN_DR1	Digital schmitt triggered input control signal of pull-up driver PU_DR1 (0/5V vs. VSS). Internally pulled-down to PVSS with equivalent 100kΩ strength.
17	IN_DR2	Digital schmitt triggered input control signal of pull-up driver PU_DR2 (0/5V vs. VSS). Internally pulled-down to PVSS with equivalent 100kΩ strength.
18	IN_SSD	Digital schmitt triggered input control signal of soft-shutdown driver (0/5V vs. VSS). Internally pulled-up to PVDD with equivalent 100kΩ strength.
19	NC	No internal connection.
20	VCC_B	Connect to VCC plane.
21	NC	No internal connection.
22	NC	No internal connection.
23	IN_PD	Digital schmitt triggered input control signal of pull-down driver PD_DR (0/5V vs. VSS). Internally pulled-up to PVDD with equivalent 100kΩ strength.
24	NC	No internal connection.
25	VSS[1]	Negative supply voltage of the logic blocks of the circuit. Its value depends on the power transistor to be driven. Connect to the same voltage than PVSS through a star-like connection.
26	VDD	Positive 5V supply voltage versus VSS, supplying all logic except the output stage of the drivers. Connect to the same voltage than PVDD through a star-like connection. Decouple with respect to VSS with a capacitor of at least 100nF.
27	NC	No internal connection.
28	NC	No internal connection.
29	EN	Digital schmitt triggered input enable signal for the driver outputs (0/5V vs. VSS). Internally pulled-down to PVSS with equivalent 100kΩ strength.
30	NC	No internal connection.
31	NC	No internal connection.
32	NC	No internal connection.
33	NC	No internal connection.

[1] *PVSS and VSS are internally connected through two anti-parallel diodes. PVSS and VSS shall be connected to the same voltage through a star-like connection.*

THERMAL CHARACTERISTICS

Parameter	Condition	Min	Typ	Max	Units
XTR25011-LJ (LJCC52)					
Thermal Resistance: J-C $R_{Th\_J\text{-}C}$			TBD		°C/W
Thermal Resistance: J-A $R_{Th\_J\text{-}A}$			TBD		°C/W

RECOMMENDED OPERATING CONDITIONS



Parameter	Min	Typ	Max	Units
High voltage power supply[1] **VCC-VSS (VCC_B, VCC_T and VCC_IO connected to VCC)**	7		35	V
High voltage driver power supplies: **PVCC_DR1 (PVCC_DR1_1 connect to PVCC_DR1_2)**	VSS+7		VCC	V
High voltage driver power supplies: **PVCC_DR2 (PVCC_DR2_1 connect to PVCC_DR2_2)**	VSS+7		VCC	V
Low voltage power supply **VDD-VSS (PVDD connected to VDD)**[2]	4.5		5.5	V
Inputs: **IN_DR1, IN_DR2, IN_MC, IN_PD, IN_SSD, EN**	VSS		VDD	
Junction Temperature[3] T_j	-60		230	°C

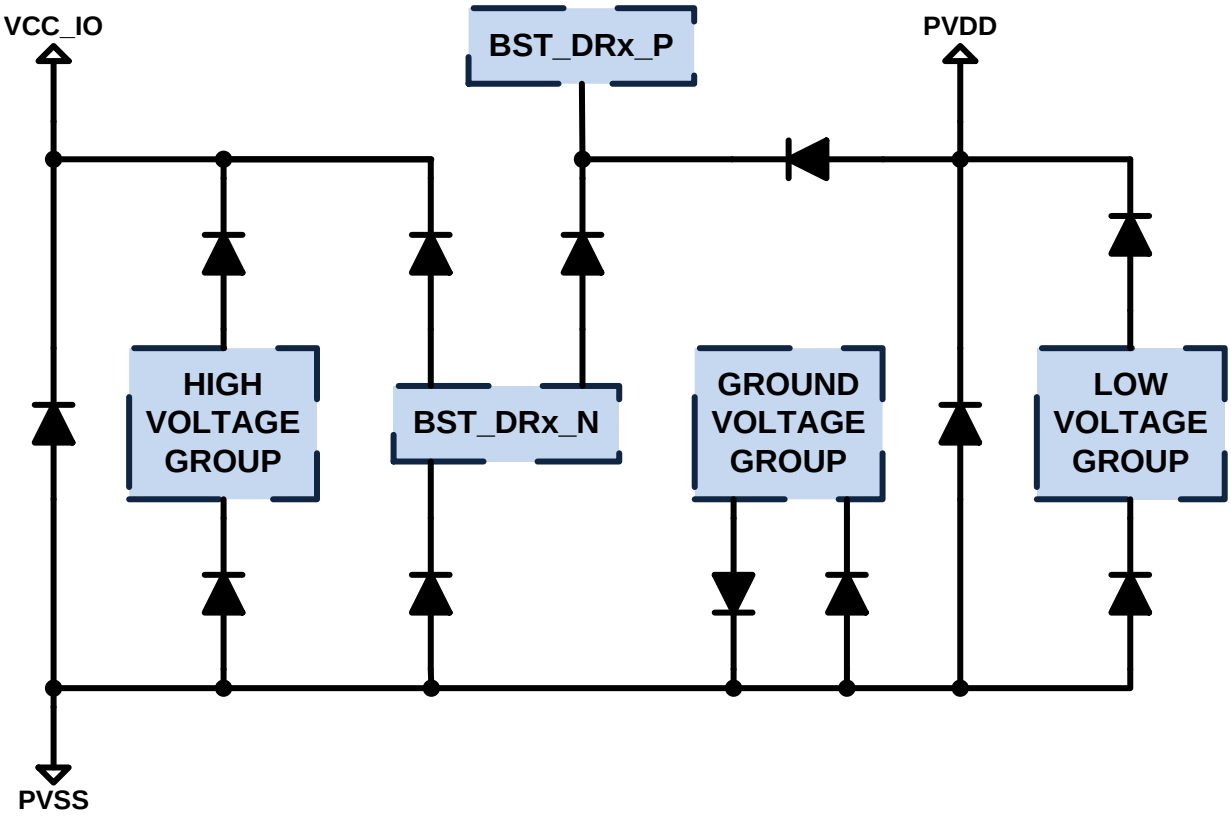
[1] *For gate drive application, it is recommended to add two decoupling capacitors in the range of 100nF to 1µF, one between VCC and SOURCE terminal of the power transistor and the other between VSS and SOURCE terminal of the power transistor. These capacitors must be placed close to the power transistor to minimize the transient gate current paths for EMI reduction.*

[2] *Add a decoupling capacitor in the range of 100nF to 1µF between VDD and VSS supply planes as close as possible to pins VDD and PVDD.*

[3] *Operation beyond the specified temperature range is achieved*

ESD CLAMPING SCHEME

Pin Groups	Pins
High voltage power supply	VCC_IO-PVSS
High voltage group	PVCC_DR2_1, PD_DR_1, PD_DR_2, PU_DR2, PU_DR1, BST_DR1_N, BST_DR2_N, VCC_T, VCC PD_MC_2, PD_MC_1, PVCC_DR1_2, PVCC_DR1_1, PVCC_DR2_2
Low voltage power supply	PVDD-PVSS
Low voltage group	IN_DR1, IN_DR2, IN_MC, IN_PD, IN_SSD, EN, PVDD_PD_CAP, PVDD_MC_CAP, VDD
Bootstrap voltages	BST_DR1_N, BST_DR1_P, BST_DR2_N, BST_DR2_P
Ground voltage group	VSS, PVSS_PD_CAP, PVSS_MC_CAP, PVSS_MC, PVSS_PD



ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for VDD-VSS=5V, VCC-VSS=25V (PVCC_DR1 and PVCC_DR2 connected to VCC) and -60°C≤T_C≤230°C. Typical values are given at T_C=25°C.

Parameter		Condition	Min	Typ	Max	Units
Supply voltage						
VCC-VSS			7		35	V
VDD-VSS			4.5		5.5	
Quiescent current consumption	I_{qVCC}	EN=0	0.10		0.45	mA
	I_{qVDD}		0.5		2.5	
Dynamic current consumption	I_{DynVCC}	EN=1, PWM frequency 100kHz, C_{LOAD}=1nF	3		5	mA
	I_{DynVDD}		2		5	
Driver						
Propagation delay t_{pd}		From digital inputs to driver outputs	100		260	ns
Rise time[1] t_r		1nF output capacitor		26		ns
Fall time[1] t_f		1nF output capacitor		23		
Minimum ON time t_{ON_min}			0.5			µs
Minimum OFF time t_{OFF_min}			0.5			
Peak output current of PU_DR1 or PU_DR2 driver I_{Peak_PU}		100nF output capacitor T_C=-60°C T_C=85°C T_C=230°C		6 5 4		A
Continuous output current of PU_DR2 or PU_DR1 I_{DC_PU}		VCC-VSS=7V		1		
Peak output current of PD_DR or PD_MC driver I_{Peak_PD}		100nF output capacitor T_C=-60°C T_C=85°C T_C=230°C		5 3.7 3		
Output drivers ON resistance R_{ON_DR}		PU_DR1, PU_DR2, PD_DR, PD_MC I_{LOAD}=200mA	0.8		2.5	Ω
ON resistance of soft-shutdown transistor R_{ON_SSD}		I_{LOAD}=2mA	400		800	
Schmidt triggered inputs (IN_DR1, IN_DR2, IN_MC, IN_SSD, IN_PD, EN)						
High level input voltage V_{IH}			3.6			V
Low level input voltage V_{IL}					1.2	
Pull-up strength (pull-up inputs) R_{PU}				100		kΩ
Pull-down strength (pull-down inputs) R_{PD}				100		

[1] *The rise/fall time measurement strongly depends on parasitic capacitance at the output of the driver. This measurement has been performed with all driver outputs shorted (PU_DRx, PD_DR_x, PD_MC_x), which adds a significant parasitic capacitance (estimated to 400pF) to the 1nF capacitance connected at the output.*

TYPICAL PERFORMANCE

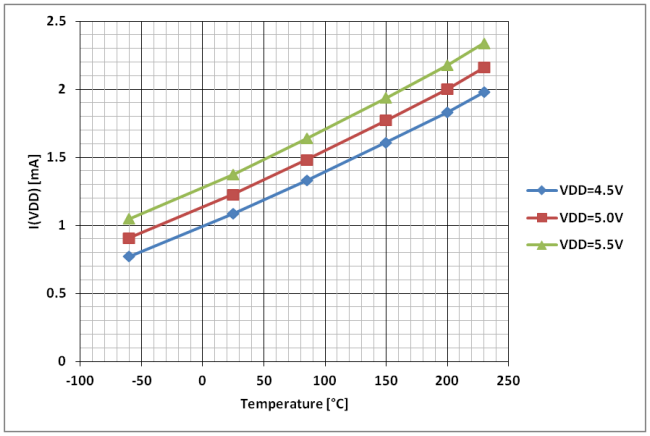


Figure 1. Quiescent current consumption on VDD versus temperature (EN=IN_SSD=1, IN_DR1=IN_DR2=IN_PD=IN_MC=0, VCC=25V).

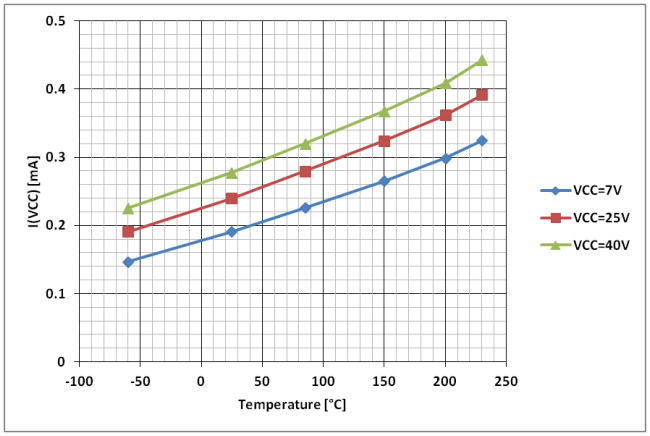


Figure 2. Quiescent current consumption on VCC versus temperature (EN=IN_SSD=1, IN_DR1=IN_DR2=IN_PD=IN_MC=0).

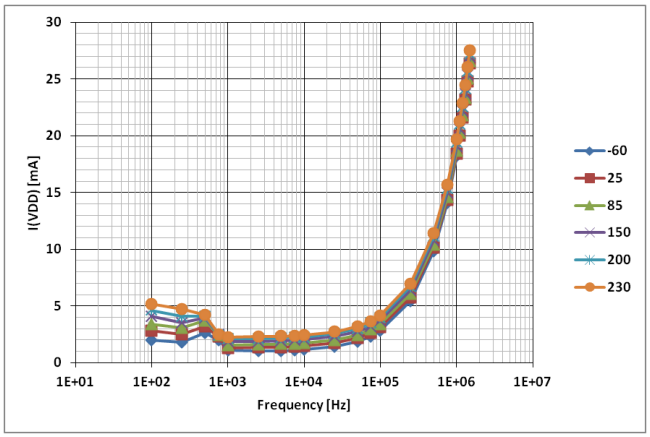


Figure 3. Dynamic current consumption on VDD versus frequency for several case temperatures (C_{LOAD}=1nF, V_{CC}=25V, V_{DD}=5V).[1]

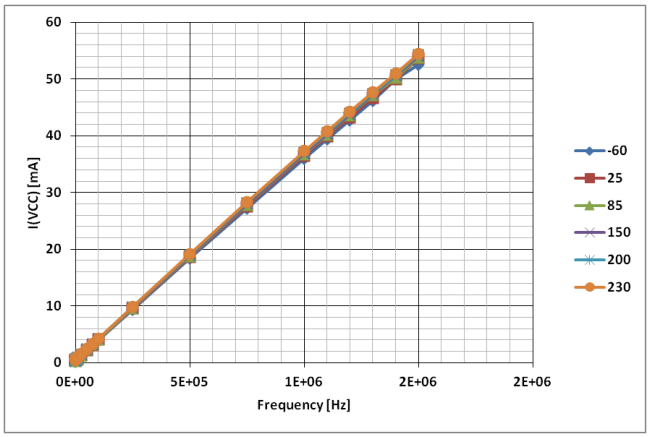


Figure 4. Dynamic current consumption on VCC versus frequency for several case temperatures (C_{LOAD}=1nF, V_{CC}=25V, V_{DD}=5V).

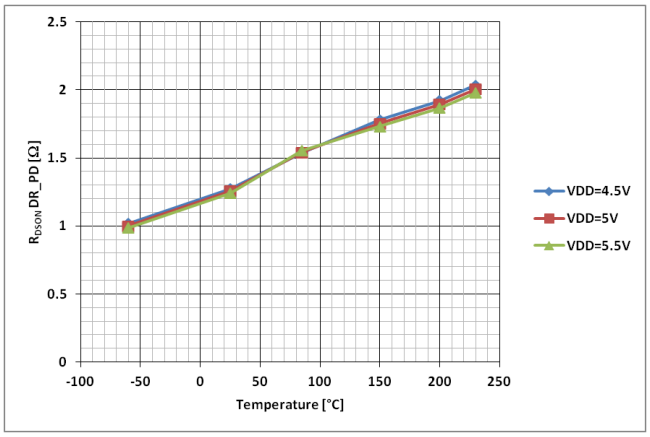


Figure 5. R_{ON} of pull-down driver (DR_PD) versus case temperature for several V_{DD} (I_{LOAD}=200mA, V_{CC}=25V).

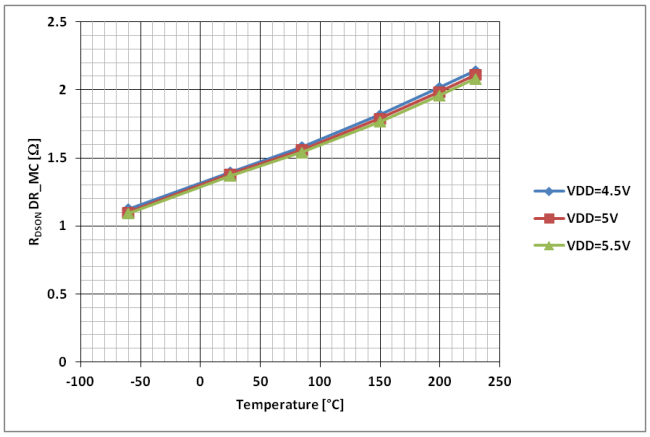


Figure 6. R_{ON} of Miller Clamp driver (DR_MC) versus case temperature for several V_{DD} (I_{LOAD}=200mA, V_{CC}=25V).

[1] *The dynamic current consumption on VDD supply significantly increases below 1kHz PWM frequency due to charge pump turn-on.*

TYPICAL PERFORMANCE (CONTINUED)

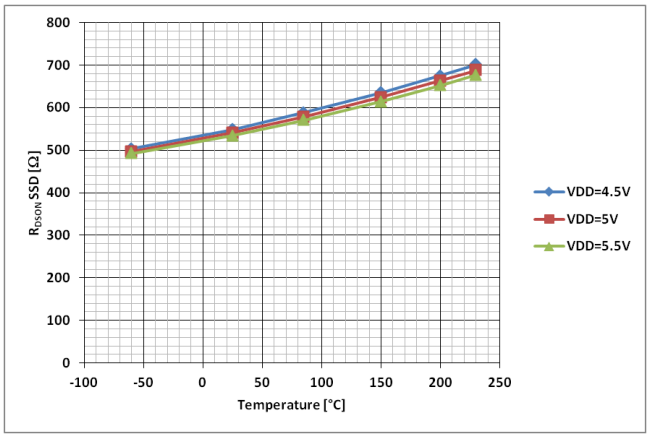


Figure 7. R_{ON} of soft-shut-down driver (SSD) versus case temperature for several V_{DD} (I_{LOAD}=2mA, V_{CC}=25V).

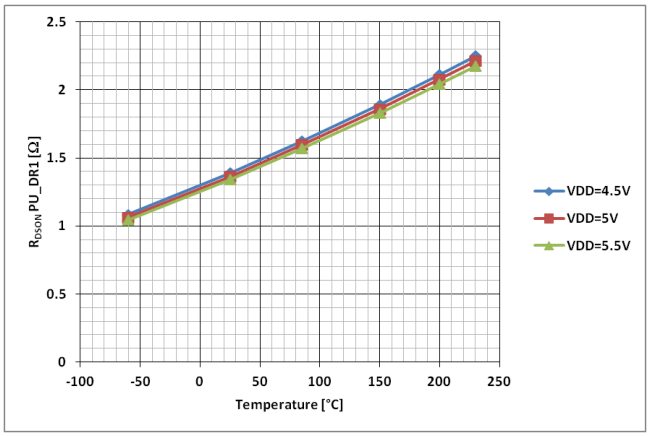


Figure 8. R_{ON} of pull-up driver (DR1_PU) versus case temperature for several V_{DD} (I_{LOAD}=200mA, V_{CC}=25V).

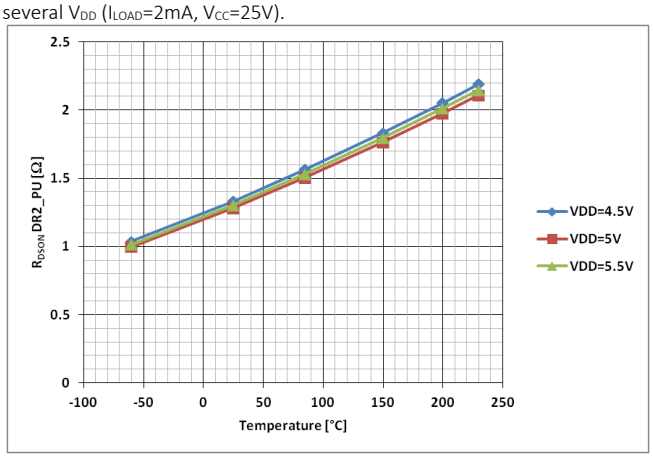


Figure 9. R_{ON} of pull-up driver (DR2_PU) versus case temperature for several V_{DD} (I_{LOAD}=200mA, V_{CC}=25V).

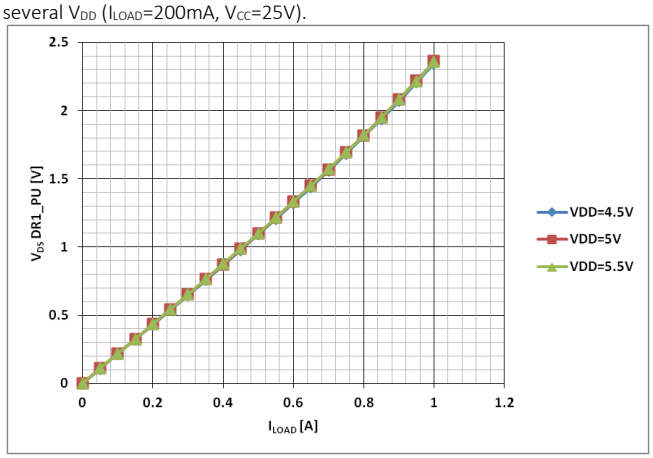


Figure 10. V_{DS} versus continuous output current of pull-up driver (DR1_PU) for different V_{DD} (T_C=230°C, V_{CC}=25V).

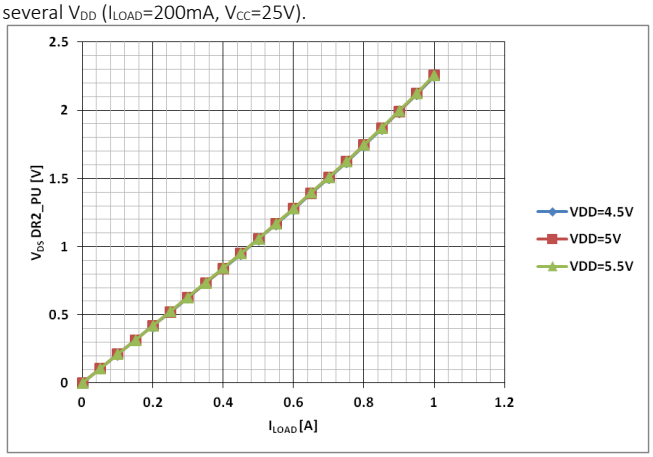


Figure 11. V_{DS} versus continuous output current of pull-up driver (DR2_PU) for different V_{DD} (T_C=230°C, V_{CC}=25V).

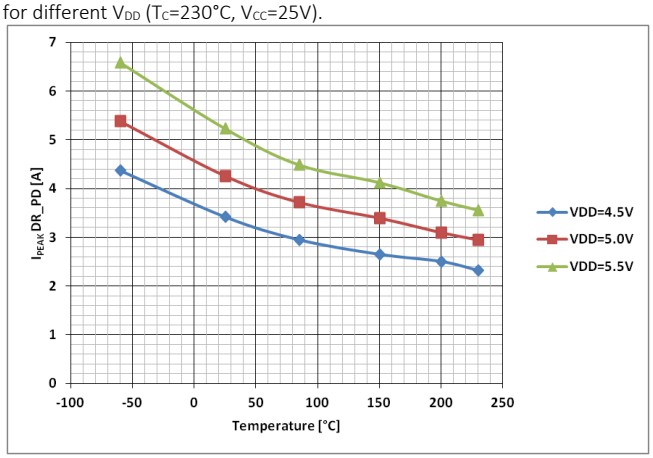


Figure 12. Peak output current of pull-down driver (DR_PD) versus case temperature for several V_{DD} (C_{LOAD}=100nF, V_{CC}=25V).

TYPICAL PERFORMANCE (CONTINUED)

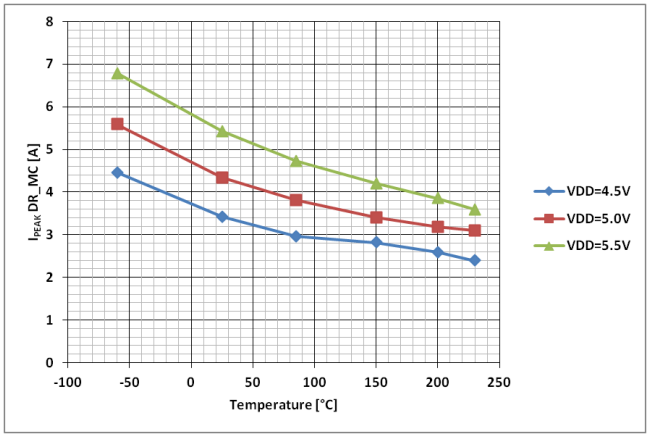


Figure 13. Peak output current of Miller Clamp driver (DR_MC) versus case temperature for several V_{DD} (C_{LOAD}=100nF, V_{CC}=25V).

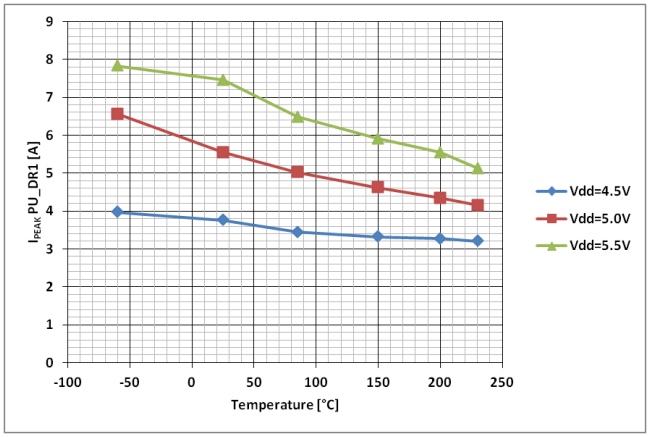


Figure 14. Peak output current of pull-up driver (DR_PD1) versus case temperature for several V_{DD} (C_{LOAD}=100nF, V_{CC}=25V).

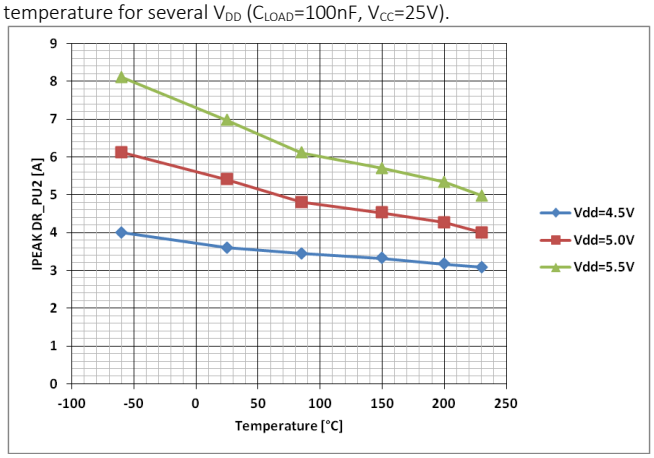


Figure 15. Peak output current of pull-up driver (DR_PU2) versus case temperature for several V_{DD} (V_{CC}=25V).

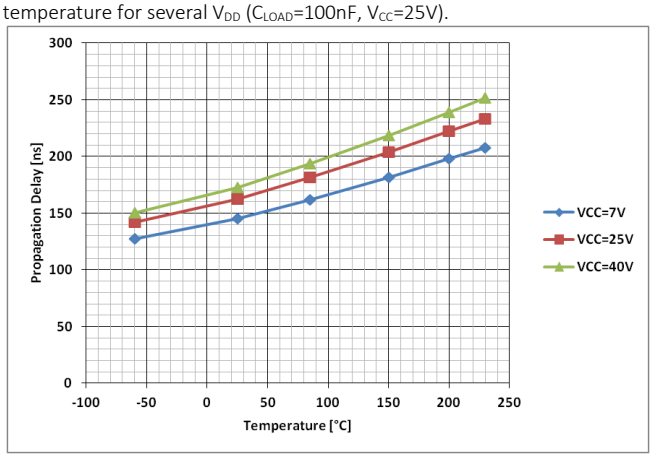


Figure 16. Propagation delay from IN_DR1 to PU_DR1 versus case temperature for several V_{CC} (CLOAD=1nF, V_{DD}=5V).

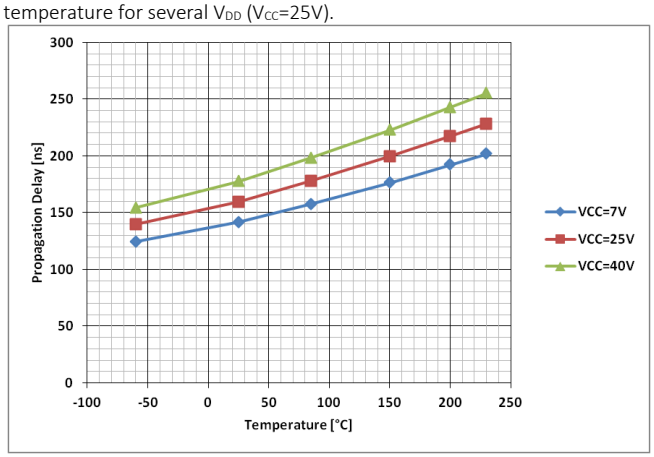


Figure 17. Propagation delay from IN_DR2 to PU_DR2 versus case temperature for several V_{CC} (C_{LOAD}=1nF, V_{DD}=5V).

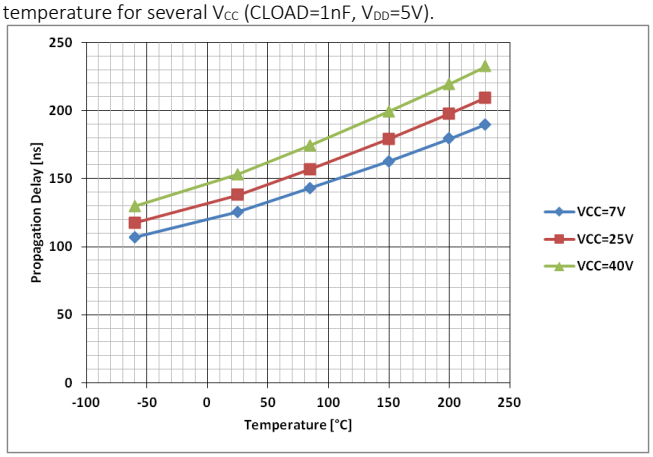


Figure 18. Propagation delay from IN_DR1 to PD_DR versus case temperature for several V_{CC} (C_{LOAD}=1nF, V_{DD}=5V).

TYPICAL PERFORMANCE (CONTINUED)

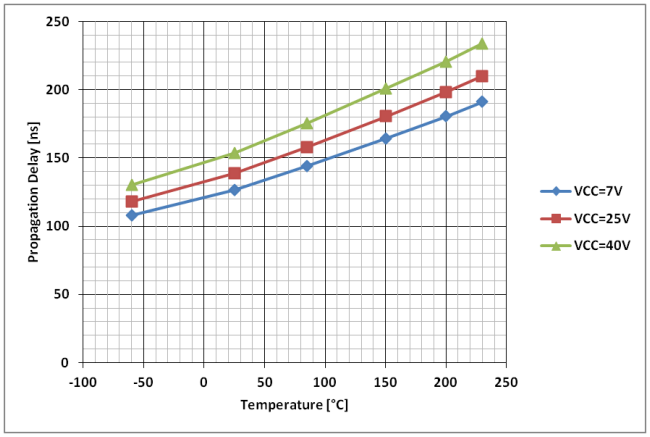


Figure 19. Propagation delay from IN_DR1 to PD_MC versus case temperature for several V_{CC} (C_{LOAD}=1nF, V_{DD}=5V).

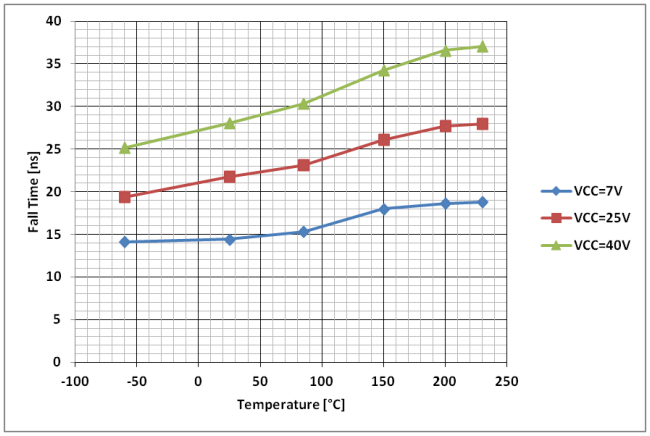


Figure 20. Fall time of PD_DR output versus case temperature for several V_{CC} (V_{DD}=5V).

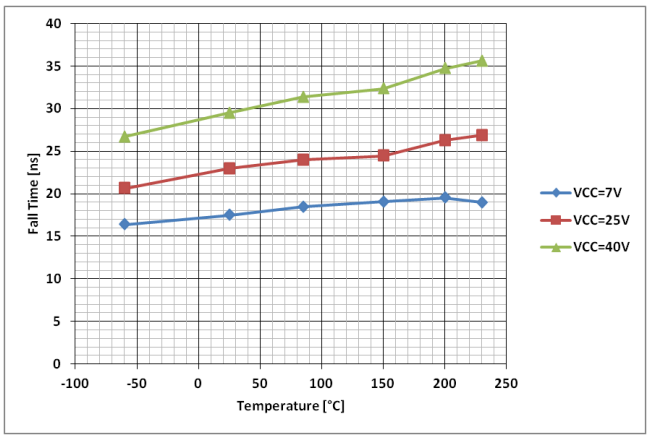


Figure 21. Fall time of PD_MC output versus case temperature for several V_{CC} (V_{DD}=5V).

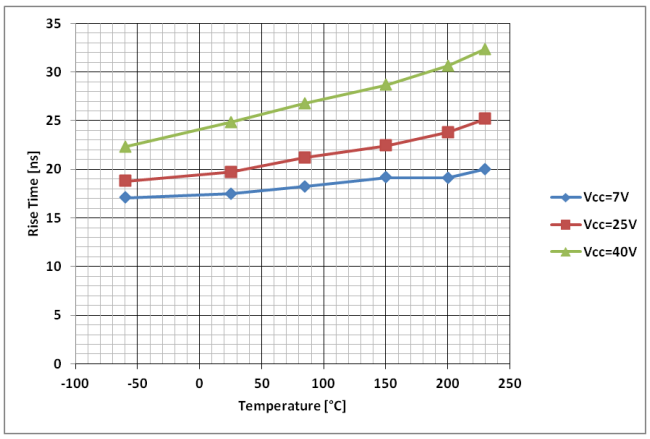


Figure 22. Rise time of PU_DR1 output versus case temperature for several V_{CC} (V_{DD}=5V).

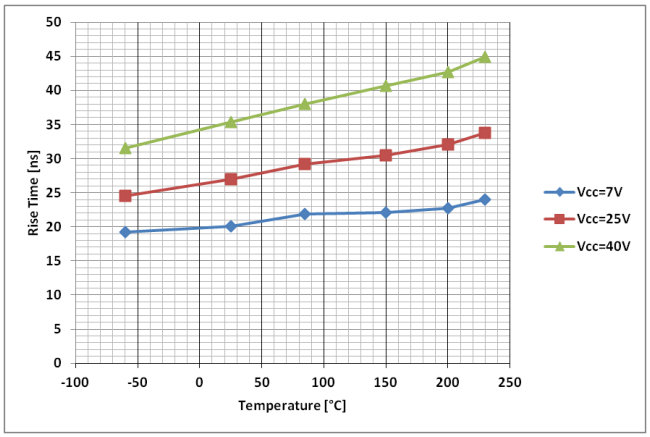


Figure 23. Rise time of PU_DR2 output versus case temperature for several V_{CC} (V_{DD}=5V).

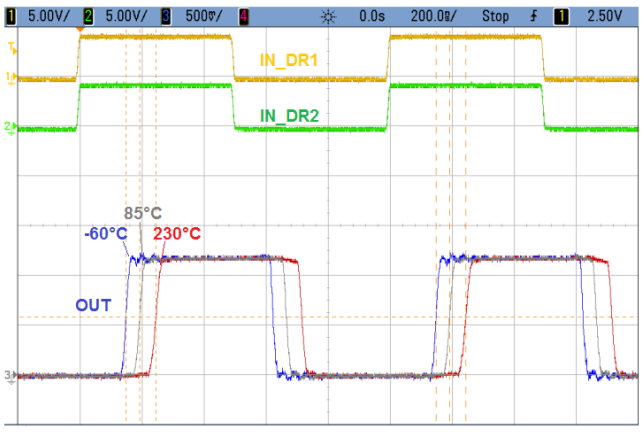


Figure 24. Oscilloscope snap shot showing operation at 1MHz input frequency versus case temperature (PU_DR1, PU_DR2, PD_DR, PD_MC connected, C_{LOAD}=1nF, V_{DD}=5V, V_{CC}=25V).

THEORY OF OPERATION

Introduction

XTR25010 is a high-temperature, high reliability power transistor driver and controller integrated circuit specifically designed to drive wide bandgap (WBG) power transistors, such as Silicon Carbide (SiC) as well as Gallium Nitride (GaN) transistors including normally-On and normally-Off JFETs, MOSFETs, SJTs, BJTs and HEMTs. For the turn-on of power transistors, the XTR25010 includes two independent pull-up gate-drive-channels (PU_DR1 and PU_DR2) each capable of sourcing 4A at T_C=230°C. For the turn-off of power transistors, the XTR25010 includes two pull-down gate-drive-channels (PD_DR and PD_MC) each capable of sinking 3A peak current at T_C=230°C. The PD_DR channel is used for the effective turn-off, while PD_MC channel is used for Active Miller Clamping (AMC).
For driving wide bandgap transistors, it is recommended to use XTR25010 as a power stage extension for the XTR26010, which generates the needed control signals and additional protection functions (see XTR26010 for more details).
For DC/DC converters and motor drive, the XTR25010 can be driven directly with suitable signals from PWM controllers such as XTR30010.

Truth table

- The EN input is master over all other inputs.
- IN_SSD is active low.
- The outputs can be set to high impedance with a logic 1 on EN and IN_SSD, and logic 0 on all other inputs.

INPUTS						OUTPUTS			
EN	IN_SSD	IN_DR1	IN_DR2	IN_PD	IN_MC	PU_DR1	PU_DR2	PD_DR	PD_MC
0	X	X	X	X	X	Z	Z	VSS	VSS
1	0	X	X	X	X	Z	Z	VSS (SSD)	Z
1	1	1	0	X	X	PVCC_DR1	Z	Z	Z
1	1	0	1	X	X	Z	PVCC_DR2	Z	Z
1	1	1	1	X	X	PVCC_DR1	PVCC_DR2	Z	Z
1	1	0	0	0	0	Z	Z	Z	Z
1	1	0	0	0	1	Z	Z	Z	VSS
1	1	0	0	1	0	Z	Z	VSS	Z
1	1	0	0	1	1	Z	Z	VSS	VSS

Bootstrap capacitors

The bootstrap capacitor value can be selected taking into account conditions 1, 2 and 3 described hereafter.

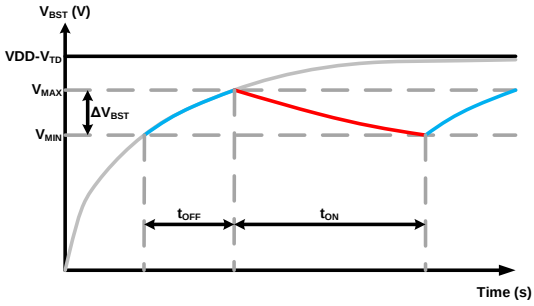


Figure 25. Bootstrap capacitor charging (shown in blue) and discharging (shown in red) curves.

- The bootstrap capacitor C_{BST} is charged for the first time during the startup time given by the rise time of the power supply. It is recommended to wait for at least a 50µs, after power supply startup, before sending any PWM signal to ensure correct first charge of the C_{BST}. The charging path is, as described in Figure 26 with the blue arrows, going from the 5V versus VSS power supply PVDD via the integrated bootstrap diode, then the external R_{PU}, and finally the PD_MC driver in parallel with the R_{PD} and the PD_DR driver. Hence, C_{BST} must fulfill the following condition to guarantee its total charge during the startup, which gives an upper limit:

Cond. 1: $C_{BST}<50\mu s/(3*R_{PU})$

As the on resistances of the PU, PD, MC transistors are in the range of 1…2Ω, they are neglected compared to R_{PU} and R_{PD}. As an example, for R_{PU}=20Ω, C_{BST} must be smaller than 833nF.

- The bootstrap capacitor C_{BST} is discharged into the PU_DR driver during the ON time t_{ON} as shown by the red arrows in Figure 26.

As shown in Figure 25, in steady state, the voltage decreases ΔV_{BST} on C_{BST} during discharge (red curve, ON time t_{ON}) is given by:

$$\Delta V_{BST}=(I_Q*t_{ON}+C_{eq}*V_{MAX})/C_{BST}$$

Where I_Q=250µA is the quiescent current delivered from BST_DRx_P to the pull-up driver, C_{eq}≈500pF is the equivalent capacitor that must be charged by BST_DRx_P up to the voltage V_{MAX}, $t_{ON}=(1/f_R)-t_{OFF}$, and fr is the PWM frequency.

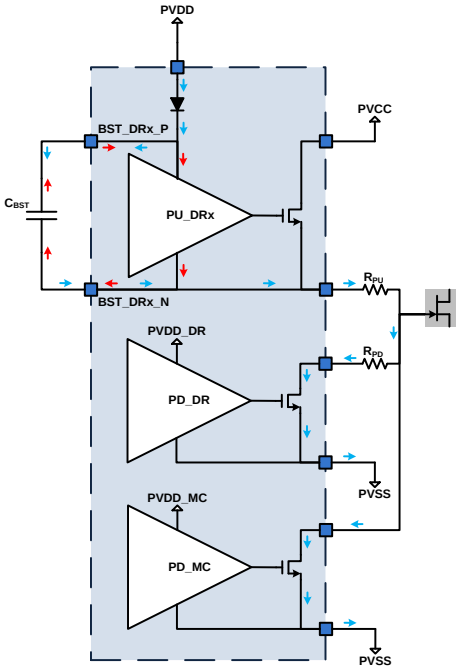


Figure 26. Bootstrap capacitor charging and discharging paths.

To have a first guess for minimum value of C_{BST}, we consider the extreme values for $V_{MAX}=V_{DD}-V_{TD}$ (V_{TD}~0.7V is the forward voltage of the bootstrap diode), and ΔV_{BST}=500mV to ensure V_{MIN} > 3.75V, which is the threshold to turn-on the integrated charge pump. Indeed, the integrated charge pump has been designed to be able to maintain the on state permanently (PWM DTC 100%). However, the charge pump is not able to provide enough charge to the bootstrap capacitor when the PWM signal is switching. Therefore, the following condition on C_{BST}, which gives a lower limit, is obtained:

Cond. 2: $C_{BST}>[I_Q*t_{ON}+C_{eq}*(V_{DD}-V_{TD})]/\Delta V_{BST}$

For $V_{DD}-V_{TD}$=4.3V, f_R=50kHz, t_{ON}=19µs (t_{OFF}=1µs), and ΔV_{BST}=500mV, C_{BST} must be higher than 13.8nF. As this is an extreme value, we recommend taking at least three times this value to reduce the voltage ripple ΔV_{BST}.

- In steady state, as shown in Figure 25, the voltage difference ΔV_{BST} on C_{BST} during the charge period (blue curve, OFF time t_{OFF}) is given by:

$$\Delta V_{BST}=(V_{DD}-V_{TD}-V_{MIN})*(1-\exp[-t_{OFF}/(R_{eq}*C_{BST})])$$

Where R_{eq} is the total resistance in the charge path of the bootstrap capacitor. When the XTR25010 is used together with XTR26010 for gate drive applications, R_{eq} is given by:

$$R_{eq}^{-1}=(R_{PU}+R_{PD})^{-1}*t_{MC}/t_{OFF}+R_{PU}^{-1}*(t_{OFF}-t_{MC})/t_{OFF}$$

Where t_{MC} is the Miller Clamp delay.

From the equation of ΔV_{BST} during the charge, and considering a given R_{eq}, the following condition on C_{BST} is obtained:

Cond. 3: $C_{BST}<-t_{OFF}/(R_{eq}*\ln[1-\Delta V_{BST}/(V_{DD}-V_{TD}-V_{MIN})])$

For V_{MIN}=4V, ΔV_{BST}=150mV, t_{MC}=100ns, t_{OFF}=1µs, and R_{eq}=21Ω (R_{PU}=R_{PD}=20Ω), C_{BST} must be smaller than 68.5nF.

With C_{BST}=47nF, R_{eq}=21Ω, fr=50kHz, t_{OFF}=1µs, the following ripple characteristics are obtained:

ΔV_{BST} = 146mV, V_{MAX} = 4.21V, V_{MIN} = 4.07V

Application considerations

Forcing a voltage V_{BST} above 6V across the bootstrap capacitor could damage the part. Indeed, during the normal switched operation, as shown in Figure 27, a parasitic charge pump effect can be created that tends to increase the voltage across the bootstrap capacitor. When the PU_DRx driver is on, the internal charge pump capacitor C_{CP} (~100pF) is charged to PVCC voltage following the charge path shown by the blue arrows in Figure 27. Then, when the PD_DR driver is on, C_{BST} is charged via C_{CP} following the charge path shown by the red arrows in Figure 27.

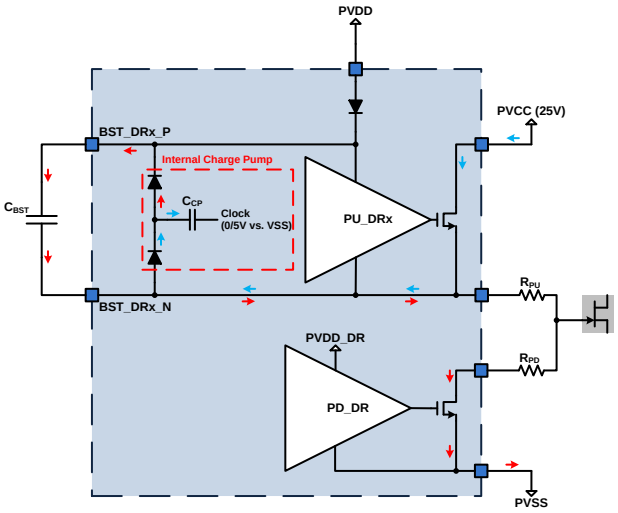


Figure 27. Parasitic charge pump charging (blue arrows) and discharging (red arrows) paths.

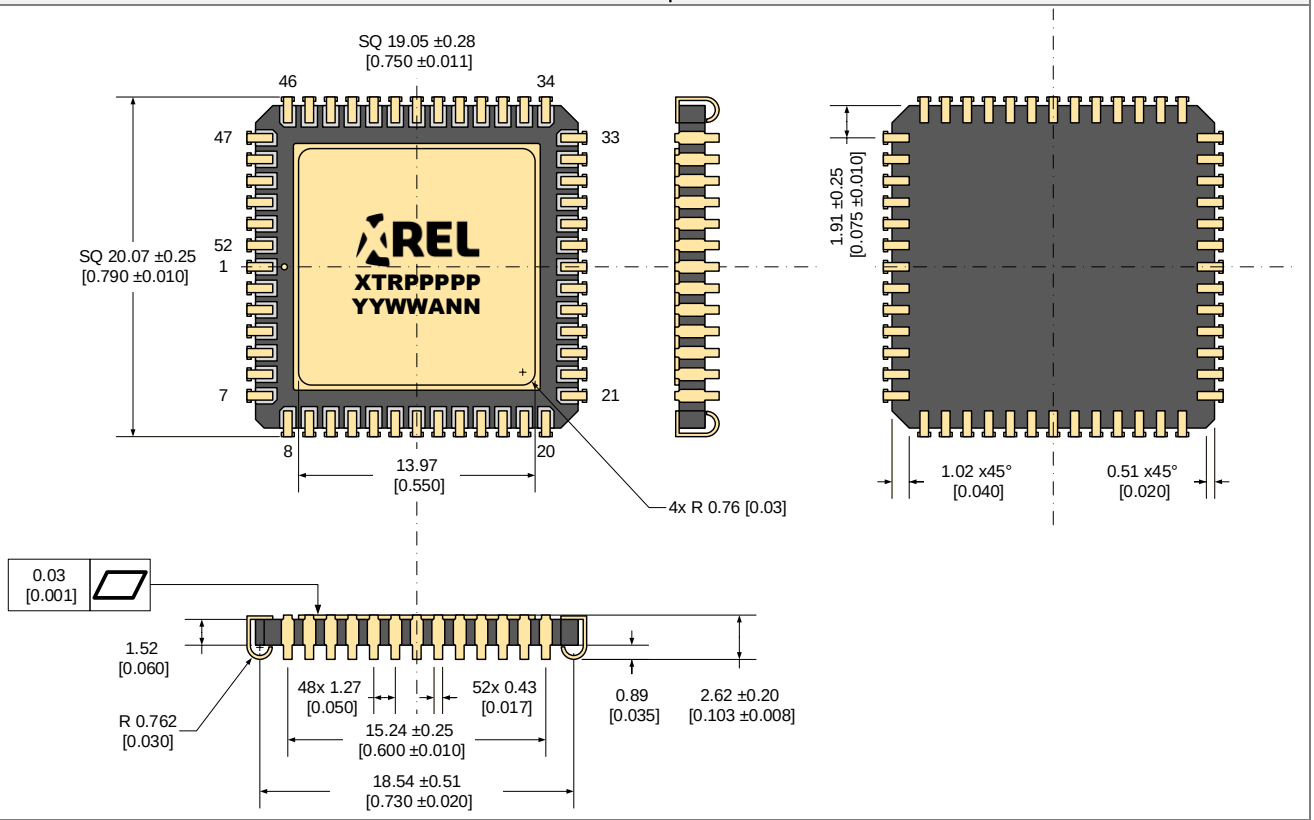
To remove the extra charge due to this parasitic charge pump effect, the XTR25010 has an internal protection that monitors V_{BST} and enables a discharge path from the bootstrap capacitor top plate (BST_DRx_P) to VSS if V_{BST} exceeds 6V. This discharge path is made of an internal resistor of about 10kΩ connected between BST_DRx_P and VSS. This protection is blanked for 2µs after each PWM rising/falling edge to avoid any spurious activation due to switching noise. Hence, considering a margin of 3µs, for t_{ON} or t_{OFF} above 5µs no additional external protection is needed.

For supply voltages (VCC-VSS) above 10V, if the PWM frequency is around or higher than 100kHz and t_{ON} or t_{OFF} are below 5µs, it is recommended to add a 6V clamping diode to avoid damaging the part.

If one of the pull-up drivers DR1_PU/DR2_PU is not used, the corresponding output PU_DR1/PU_DR2 shall be connected to PVSS. Otherwise the unused driver could be damaged due to an excessive charge of the bootstrap capacitor caused by the parasitic charge pump effect.

PACKAGE OUTLINES

J-Formed Leaded Chip Carrier LJCC52



Part Marking Convention	
Part Reference: XTRPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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