HARRIS

82C59A

CMOS Priority Interrupt Controller

REFERENCE PAGE 4-156 FOR APPLICATION NOTE 109

Features

- Pin Compatible with NMOS 8259A
- 8MHz and 5MHz Versions Available
- Eight Level Priority Controller, Expandable to 64 Levels
- Fully TTL Compatible
- High Speed, No "Wait State" Operation with 8MHz 80C86 and 80C88
- Programmable Interrupt Modes
- 8080/8085 and 8086/80C86/80C88 Compatible Operation
- Individual Request Mask Capability
- Fully Static Design
- Scaled SAJI IV CMOS Process
- Single 5V Power Supply
- Low Standby Power — 10μA Maximum
- Wide Operating Temperature Ranges:
  - C82C59A ..... 0°C to +70°C
  - I82C59A ..... -40°C to +85°C
  - M82C59A ..... -55°C to +125°C

Description

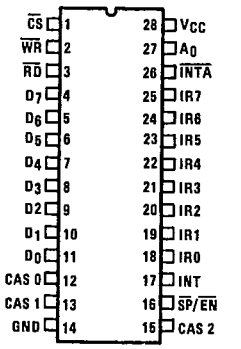
The Harris 82C59A is a high performance CMOS Priority Interrupt controller manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C59A is designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system. The high speed and industry standard configuration of the 82C59A make it compatible with microprocessors such as the 80C86, 80C88, 8086, 8080/85 and NSC800.

The 82C59A can handle up to eight vectored priority interrupting sources and is cascadable to 64 without additional circuitry. Individual interrupting sources can be masked or prioritized to allow custom system configuration. Two modes of operation make the 82C59A compatible with both 8080/85 and 80C86/88 formats.

Static CMOS circuit design insures low operaing power. Harris advanced SAJI process results in performance equal to or greater than existing equivalent products at a fraction of the power.

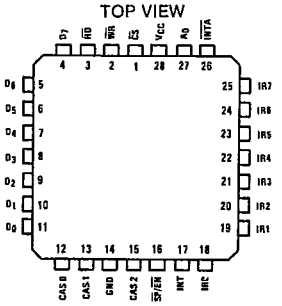
Pinouts

TOP VIEW

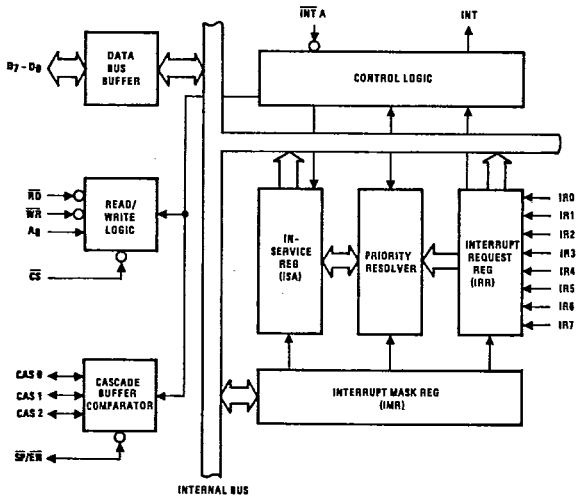


LCC/PLCC

TOP VIEW



Functional Diagram



D_7-D_0	DATA BUS (BI-DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS 2 - CAS 0	CASCADE LINES
$\overline{SP/EN}$	SLAVE PROGRAM INPUT ENABLE
INT	INTERRUPT OUTPUT
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE INPUT
IR0 - IR7	INTERRUPT REQUEST INPUTS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	28	I	V_{CC}: The +5V power supply pin. A 0.1μF capacitor between pins 14 and 28 is recommended for decoupling.
GND	14	I	GROUND
$\overline{CS}$	1	I	CHIP SELECT: A low on this pins enables $\overline{RD}$ and $\overline{WR}$ communications between the CPU and the 82C59A. INTA functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	WRITE: A low on this pin when $\overline{CS}$ is low enables the 82C59A to accept command words from the CPU.
$\overline{RD}$	3	I	READ: A low on this pin when $\overline{CS}$ is low enables the 82C59A to release status onto the data bus for the CPU.
D_7-D_0	4-11	I/O	BIDIRECTIONAL DATA BUS: Control status and interrupt-vector information is transferred via this bus.
CAS 0 - CAS 2	12, 13, 15	I/O	CASCADE LINES: the CAS lines form a private 82C59A bus to control a multiple 82C59A structure. These pins are outputs for a master 82C59A and inputs for a slave 82C59A.
$\overline{SP}/\overline{EN}$	16	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. when in the Buffered Mode it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it is used as an input to designate a master ($\overline{SP}$ = 1) or slave ($\overline{SP}$ = 0).
INT	17	O	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IRO-IR7	18-25	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high fevel on an IR input (Level Triggered Mode).
INTA	26	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable 82C59A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	27	I	ADDRESS LINE: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 82C59A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to CPU A0 address line (A for 80C86/88).

Functional Description

INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

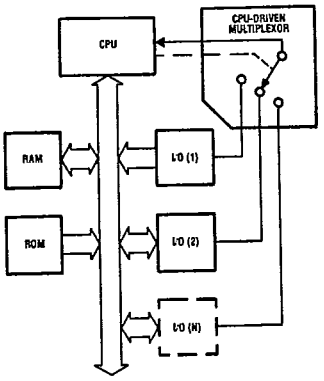
The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system through-put, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

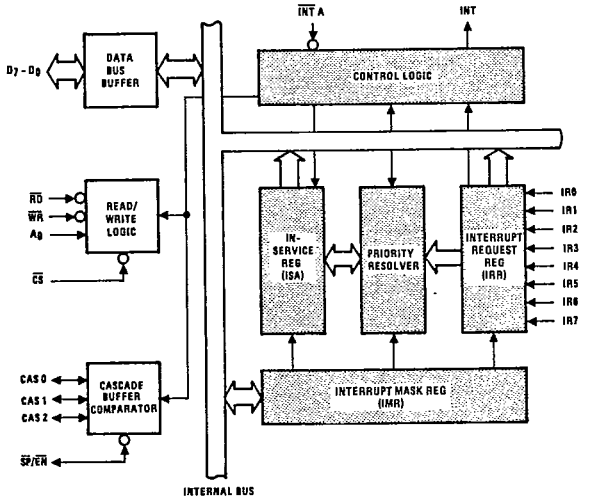
This is the interrupt-driven method. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

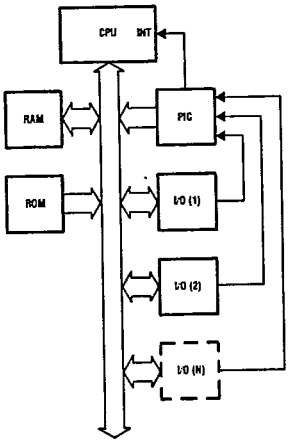
Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.



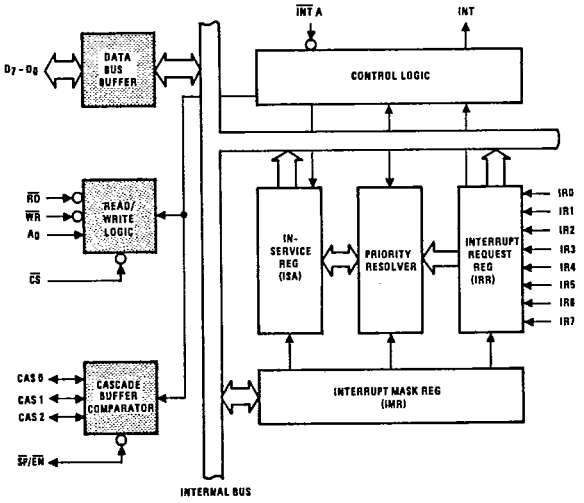
POLLED METHOD



82C59A INTERRUPT LOGIC



INTERRUPT METHOD



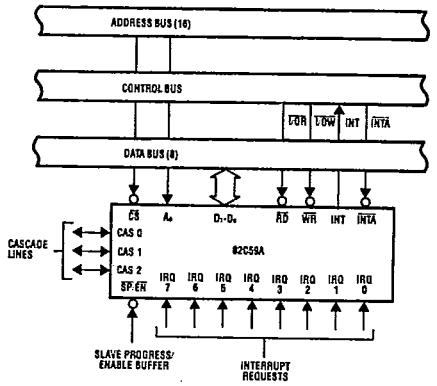
82C59A DATA AND CONTROL LOGIC

82C59A FUNCTIONAL DESCRIPTION

The 82C59A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels of requests and has built-in features for expandability to other 82C59As (up to 64 levels). It is programmed by system software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 82C59A can be configured to match system requirements. The priority modes can be changed or reconfigured dynamically at any time during main program operation. This means that the complete interrupt structure can be defined as required, based on the total system environment.

INTERRUPT REQUEST REGISTER (IRR) and IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are currently being serviced.



PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during the INTA sequence.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which disable the interrupt lines to be masked. The IMR operates on the output of the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INTERRUPT (INT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A, 8086, 8088 and 80C86, 80C88 input levels.

INTERRUPT ACKNOWLEDGE ($\overline{INTA}$)

$\overline{INTA}$ pulses will cause the 82C59A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 82C59A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 82C59A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 82C59A to be transferred onto the Data Bus.

CHIP SELECT ($\overline{CS}$)

A LOW on this input enables the 82C59A. No reading or writing of the device will occur unless the device is selected.

WRITE ($\overline{WR}$)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 82C59A.

READ ($\overline{RD}$)

A LOW on this input enables the 82C59A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level (in the poll mode.) onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 82C59As used in the system. The associated three I/O pins (CAS0-2) are outputs when the 82C59A is used as a master and are inputs when the 82C59A is used as a slave. As a master, the 82C59A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive INTA pulses. (See section "Cascading the 82C59A".)

INTERRUPT SEQUENCE

The powerful features of the 82C59A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specified interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

These events occur in an 8080A/8085 system:

1. One or more of the INTERRUPT REQUEST lines (I0-I7) are raised high, setting the corresponding IRR bit(s).
2. The 82C59A evaluates these requests in the priority resolver and sends an interrupt (INT) to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 82C59A will also release a CALL instruction code (11001101) onto the 8-bit data bus through D_0-D_7.
5. This CALL instruction will initiate two additional $\overline{INTA}$ pulses to be sent to the 82C59A from the CPU group.
6. These two INTA pulses allow the 82C59A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first INTA pulse and the higher 8-bit address is released at the second INTA pulse.
7. This completes the 3-byte CALL instruction released by the 82C59A. In the AEOI mode, the ISR bit is reset at the end of the third INTA pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an 80C86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 82C59A does not drive the data bus during this cycle.
5. The 80C86 will initiate a second $\overline{INTA}$ pulse. During this pulse, the 82C59A releases an 8-bit pointer onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode, the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request was too short in duration), the 82C59A will issue an interrupt level 7. If a slave is programmed on IR bit 7, the CAS lines remain inactive and vector addresses are output from the master 82C59A.

Interrupt Sequence Outputs

8080, 8085

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse, the CALL opcode is enabled onto the data bus.

First Interrupt Vector Byte Data: Hex CD

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse, the lower address of the appropriate service routine is enabled onto the data bus. When interval = 4 bits, A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the 82C59A. When interval = 8, only A_6 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR					Interval = 4			
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR					Interval = 8			
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third $\overline{INTA}$ pulse, the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8-A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

80C86, 80C88 INTERRUPT RESPONSE MODE

80C86 mode is similar to 8080/85 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of 8080/85 systems in that the 82C59A uses it to internally freeze the state of the interrupts for priority resolution and, as a master, it issues the interrupt code on the cascade lines. On this first cycle, it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in 80C86 mode, the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in 80C86 mode.)

Content of Interrupt Vector Byte for 80C86 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 82C59A

The 82C59A accepts two types of command words generated by the CPU;

1. Initialization Command Words (ICWs): Before normal operation can begin, each 82C59A in the system must be brought to a starting point—by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. Operation Command Words (OCWs): These are the command words which command the 82C59A to operate in various interrupt modes. Among these modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 82C59A anytime after initialization.

Initialization Command Words (ICWS)

GENERAL

Whenever a command is issued with A0=0 and D4=1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR7 input is assigned priority 7.
d. Special Mask Mode is cleared and Status Read is set to IRR.
e. If IC4=0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, 8080/85 system).

*NOTE: Master/Slave in ICW4 is only used in the buffered mode.

INITIALIZATION COMMAND WORDS 1 and 2 (ICW1, ICW2)

A_5-A_{15}: Page starting address of service routines. In an 8080/85 system, the 8 request levels will generate CALLS to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the 82C59A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the 82C59A while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

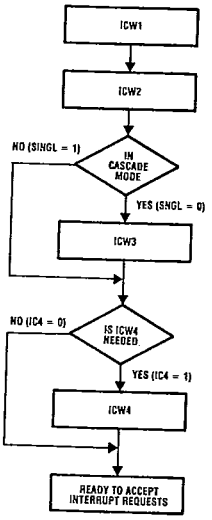
In an 80C86 system, A_{15}-A_{11} are inserted in the five most significant bits of the vectoring byte and the 82C59A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 82C59A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

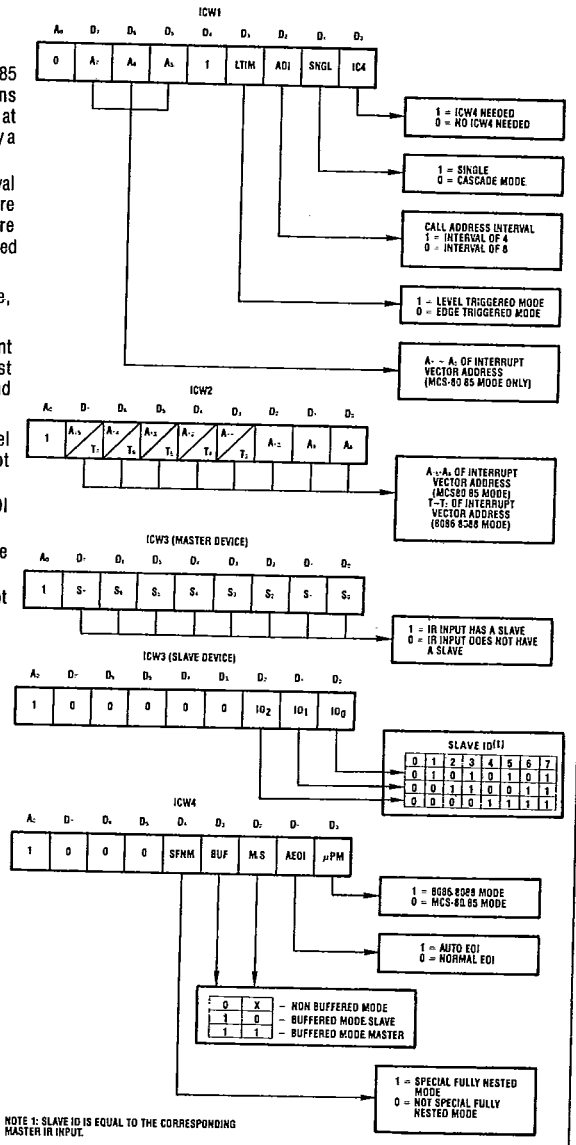
ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 82C59A in the system. If SNGL=1, no ICW3 will be issued.

IC4: If this bit is set—ICW4 has to be issued. If ICW4 is not needed, set IC4 = 0.



82C59A INITIALIZATION SEQUENCE



82C59A INITIALIZATION COMMAND WORD FORMAT

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 82C59A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP=1, or in buffered mode when M/S=1 in ICW4), a "1" is set for each slave in the bit corresponding to the appropriate IR line for the slave. The master then will release byte 1 of the call sequence (for 8080/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 80C86, only byte 2) through the cascade lines.

b. In the slave mode (either when SP=0, or if BUF=1 and M/S=0 in ICW4), bits 2-0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 80C86) are released by it on the Data Bus (Note: the slave address must correspond to the IR line it is connected to in the master ID).

INITIALIZATION COMMAND WORD 4 (ICW4)

SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, the buffered mode is programmed. In buffered mode, SP/EN becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 82C59A is programmed to be a master, M/S = 0 means the 82C59A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1, the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 82C59A for 8080/85 system operation, μPM = 1 sets the 82C59A for 80C86 system operation.

OPERATION COMMAND WORDS (OCWs)

After the initialization Command Words (ICWs) are programmed into the 82C59A, the device is ready to accept interrupt requests at its input lines. However, during the 82C59A operation, a selection of algorithms can command the 82C59A to operate in various modes through the Operation Command Words (OCWs).

OPERATION CONTROL WORDS (OCWs)

A0	D7	D6	D5	D4	D3	D2	D1	D0
				OCW1				
1	M7	M6	M5	M4	M3	M2	M1	M0
				OCW2				
0	R	SL	EOI	0	0	L2	L1	L0
				OCW3				
0	0	ESMM	SMM	0	1	P	RR	RIS

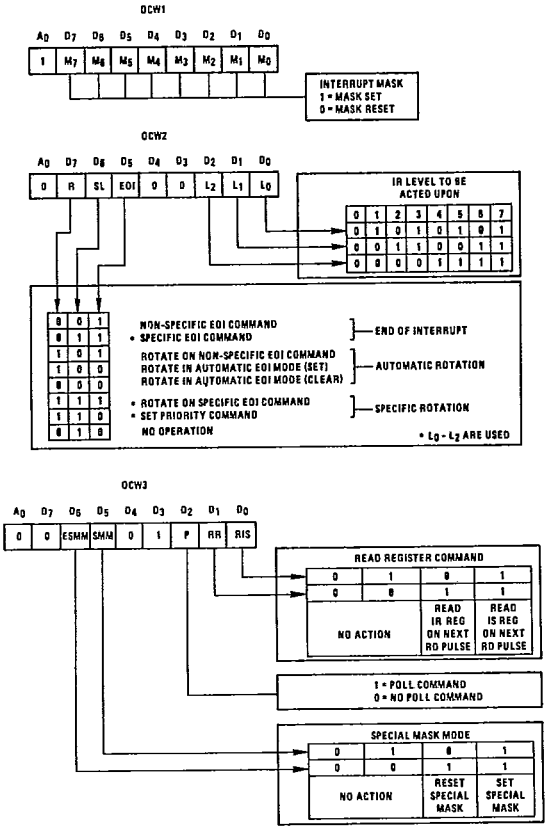
OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the Interrupt Mask Register (IMR). M_7-M_0 represent the eight mask bits. M=1 indicates the channel is masked (inhibited), M=0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

R, SL, EOI—These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0—These bits determine the interrupt level acted upon when the SL bit is active.



82C59A OPERATION COMMAND WORD FORMAT

OPERATION CONTROL WORD 3 (OCW3)

ESMM – Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM=0,the SMM bit becomes a "don't care".

SMM – Special Mask Mode. If ESMM=1 and SMM=1,the 82C59A will enter Special Mask Mode. If ESMM=1 and SMM=0,the 82C59A will revert to normal mask mode. When ESMM=0, SMM has no effect.

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (IS0-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last $\overline{INTA}$. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode or via the set priority command.

END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{INTA}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 82C59A before returning from a service routine (EOI Command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 82C59A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 82C59A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI=1, SL=0, R=0).

When a mode is used which may disturb the fully nested structure, the 82C59A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI=1, SL=1, R=0, and L0-L2 is the binary level of the IS bit to be reset).

An IRR bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 82C59A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

If AEOI=1 in ICW4, then the 82C59A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 82C59A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in 8080/85, second in 80C86). Note that from a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single 82C59A.

AUTOMATIC ROTATION (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most once. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	1	0	0	0	0
PRIORITY STATUS	7	6	5	4	3	2	1	0
	lowest							highest

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	0	0	0	0	0
PRIORITY STATUS	2	1	0	7	6	5	4	3
	highest							lowest

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the Rotate in Automatic EOI Mode which is set by (R=1, SL=0, EOI=0) and cleared by (R=0, SL=0, EOI=0).

SPECIFIC ROTATION (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R=1, SL=1; L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R=1, SL=1, EOI=1 and L0-12=IR level to receive bottom priority).

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 82C59A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: ESMM=1, SMM=1, and cleared where ESMM=1, SMM=0.

POLL COMMAND

In this mode, the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P=1 in OCW3. The 82C59A treats the next $\overline{RD}$ pulse to the 82C59A (i.e. $\overline{RD}$=0, $\overline{CS}$=0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

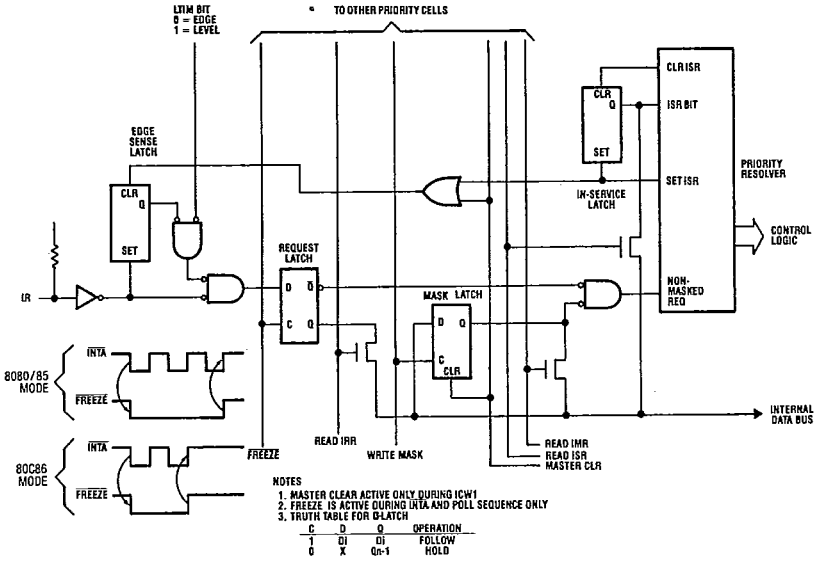
The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	—	—	—	—	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the INTA sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.



PRIORITY CELL – SIMPLIFIED LOGIC DIAGRAM

READING THE 82C59A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 (IMR)).

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0).

The ISR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corrersponds with the previous one; i.e., the 82C59A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used. In the poll mode, the 82C59A treats the $\overline{RD}$ following a "poll write" operation as an INTA. After initialization, the 82C59A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0 = 1 (OCW1). Polling overrides status read when P = 1, RR = 1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

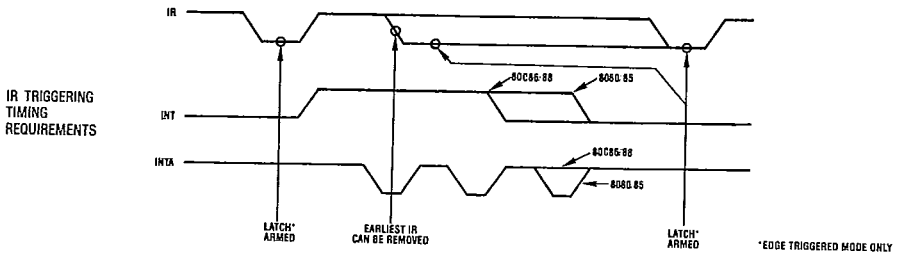
If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occuring.

The priority cell diagram showns a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 82C59A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowleges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

In power sensitive applications, it is advisable to place the 82C59A in the edge-triggered mode with the IR lines normally high. This will minimize the current through the pull-up resistors on the IR pins.



THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the special fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IRs within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specified EOI can be sent to the master,too. If not, no EOI should be sent.

BUFFERED MODE

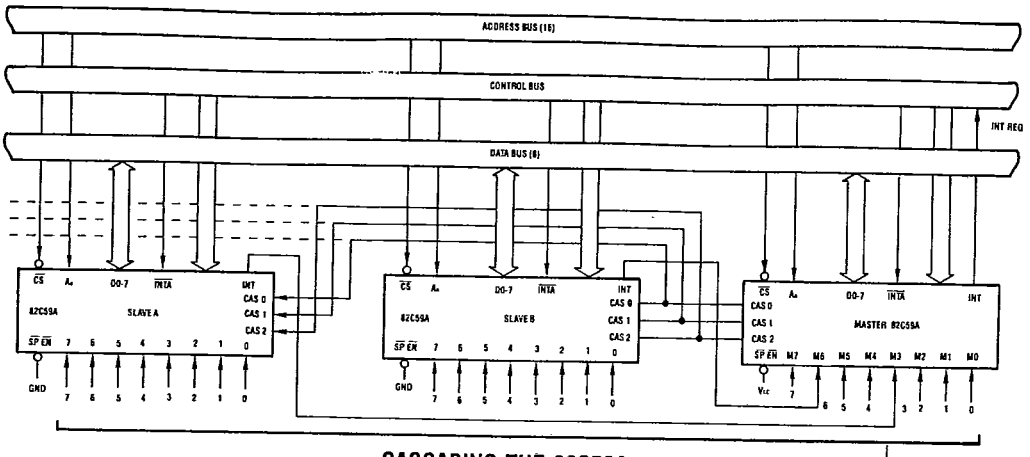
When the 82C59A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 82C59A to send an enable signal of SP/EN to enable the buffers. In this mode, whenever the 82C59A's data bus outputs are enabled, the SP/EN output becomes active.

This modification forces the use of software programming to determine whether the 82C59A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 82C59A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.



CASCADING THE 82C59A

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 80C86/80C88).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 82C59A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. Chip select decoding is required to activate each 82C59A.

Note: Auto EOI is supported in the slave mode for the 82C59A.

The cascade lines of the Master 82C59A are activated only for slave inputs, non-slave inputs leave the cascade line inactive (low). Therefore, it is necessary to use a slave address of 0 (zero) only after all other addresses are used.

Specifications 82C59A

Absolute Maximum Ratings

Supply Voltage ..... +8.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.5V to VCC +0.5V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 20°C/W (CERDIP package), 25°C/W (LCC package)
θ_{ja} ..... 58°C/W (CERDIP package), 63°C/W (LCC package)
Gate Count ..... 1250 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
C82C59A ..... 0°C to +70°C
I82C59A ..... -40°C to +85°C
M82C59A ..... -55°C to +125°C

D. C. Electrical Specifications

VCC = 5.0V ± 10%; T_A = 0°C to +70°C (C82C59A); T_A = -40°C to +85°C (I82C59A); T_A = -55°C to +125°C (M82C59A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	I82C59A, C82C59A, M82C59A
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Output High Voltage	3.0 VCC -0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	+1.0	μA	VIN = GND or VCC DIP Pins: 1-3, 26-27
IO	I/O Leakage Current	-10.0	+10.0	μA	VO = GND or VCC DIP Pins: 4-13, 15-16
ILIR	IR Input Load Current		-500 10	μA μA	VIN = 0V VIN = VCC
ICCSB	Standby Power Supply Current		10	μA	VCC = 5.5V, VIN = VCC or GND (Note 1) Outputs Open
ICCOP	Operating Power Supply Current		1	mA/MHz	T_A = +25°C, VCC = 5V, Typical (Note 2)

NOTES: 1. Except for IR0-IR7 where VIN = VCC or open.
2. ICCOP = 1mA/MHz of peripheral read/write cycle time. (Example: 1.0μs I/O read/write cycle time = 1mA).

Capacitance T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	5	pF	FREQ = 1MHz, all measurements are referenced to device GND
C_{OUT}	Output Capacitance	15	pF	
$C_{I/O}$	I/O Capacitance	20	pF	

Specifications 82C59A

A. C. Electrical Specifications

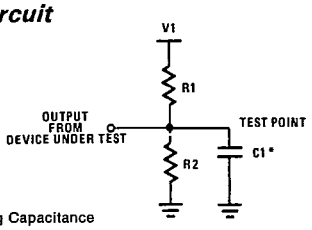
V_{CC} = 5V ± 10%, GND = 0V; T_A = 0°C to +70°C (C82C59A) (C82C59A-5)
T_A = -40°C to +85°C (I82C59A) (I82C59A-5)
T_A = -55°C to +125°C (M82C59A) (M82C59A-5)

SYMBOL	PARAMETER	82C59A-5 MIN	82C59A-5 MAX	82C59A MIN	82C59A MAX	UNITS	TEST CONDITIONS
TIMING REQUIREMENTS							
(1) TAHRL	AO/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$	10		10		ns	
(2) TRHAX	AO/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$	5		5		ns	
(3) TRLRH	$\overline{RD}$/$\overline{INTA}$ Pulse Width	235		160		ns	
(4) TAHWL	AO/$\overline{CS}$ Setup to $\overline{WR}$	0		0		ns	
(5) TWHAX	AO/$\overline{CS}$ Hold after $\overline{WR}$	5		5		ns	
(6) TWLWH	$\overline{WR}$ Pulse Width	165		95		ns	
(7) TDVWH	Data Setup to $\overline{WR}$	240		160		ns	
(8) TWHDX	Data Hold after $\overline{WR}$	5		5		ns	
(9) TJLJH	Interrupt Request Width (Low)	100		100		ns	See Note 1
(10) TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$ (Slave Only)	55		40		ns	
(11) TRHRL	End of $\overline{RD}$ to next $\overline{RD}$; End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		160		ns	
(12) TWHWL	End of $\overline{WR}$ to next $\overline{WR}$	190		190		ns	
(13) TCHCL	End of Command to next Command (Not same command type) End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	500		400		ns	

*Worst case timinng for TCHCL in an actual microprocessor system is typically much greater than 400ns (i.e. 8085A = 1.6μs, 8085A-2 = 1μs, 80C86 = 1μs).
NOTE 1. This is the low time required to clear the input latch in the edge triggered mode.

SYMBOL	PARAMETER	82C59A-5 MIN	82C59A-5 MAX	82C59A MIN	82C59A MAX	UNITS	TEST CONDITIONS
TIMING RESPONSES							
(14) TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$		160		120	ns	1
(15) TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$	10	100	10	85	ns	2
(16) TJHIH	Interrupt Output Delay		350		300	ns	1
(17) TIALCV	Cascade Valid from First $\overline{INTA}$ (Master Only)		565		360	ns	1
(18) TRLEL	Enable Active from $\overline{RD}$ or $\overline{INTA}$		125		100	ns	1
(19) TRHEH	Enable Inactive from $\overline{RD}$ or $\overline{INTA}$		60		50	ns	1
(20) TAHDV	Data Valid from Stable Address		210		200	ns	1
(21) TCVDV	Cascade Valid to Valid Data		300		200	ns	1

A. C. Test Circuit

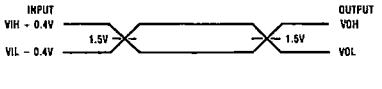


*Includes Stray and Jig Capacitance

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	Open	100pF
2	4.5V	1.8kΩ	1.8kΩ	30pF

TEST CONDITION DEFINITION TABLE

A. C. Testing Input, Output Waveforms

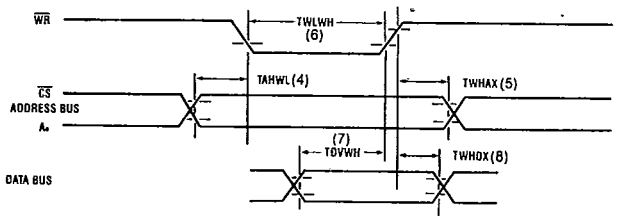


A.C. Testing: All input signals must switch between VIL - 0.4V and VIH + 0.4V. Input rise and fall times are driven at 1ns/V.

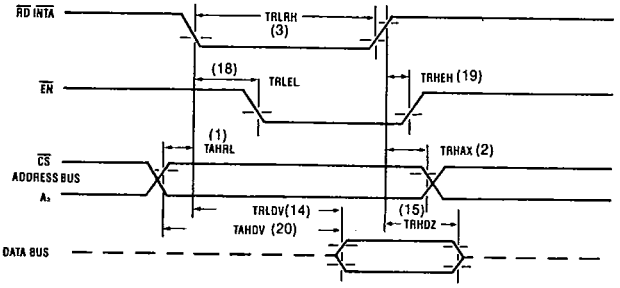
T-52-33-13

Waveforms

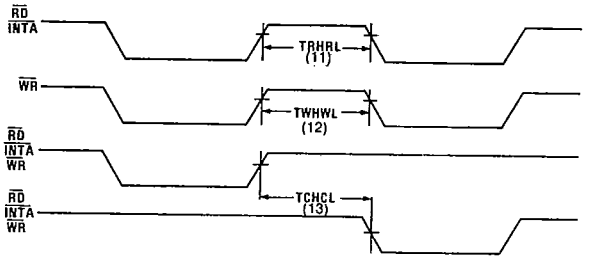
WRITE



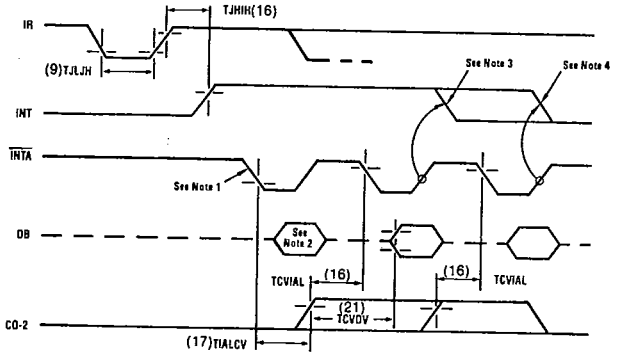
READ/INTA



OTHER TIMING



INTA SEQUENCE



Note 1: Interrupt Request (IR) must remain HIGH until leading edge of first $\overline{\text{INTA}}$.
Note 2: During first $\overline{\text{INTA}}$ the Data Bus is not active in 80C86/88 mode.
Note 3: 80C86/88 mode.
Note 4: 8080/8085 mode.