SILICON P-N-P-N PLANAR TETRODE THYRISTOR

Planar p-n-p-n trigger device in a microminiature plastic envelope. It is intended for use as a programmable trigger device (SCS = silicon controlled switch).

QUICK REFERENCE DATA

Anode gate – cathode voltage	$V_{ga\text{-}kR}$	max.	70 V
Anode gate – anode voltage (open cathode)	$V_{ga\text{-}aO}$	max.	70 V
Average anode current	$I_{A(AV)}$	max.	175 mA
Total power dissipation at T_{amb} = 25 °C	P_{tot}	max.	250 mW
Junction temperature	T_j	max.	150 °C
Gate-controlled turn-on time $R_{gk\text{-}k}$ = 1 kΩ	t_{gt}	<	0,25 μs
Circuit-commutated turn-off time $R_{gk\text{-}k}$ = 1 kΩ	t_q	<	5 μs

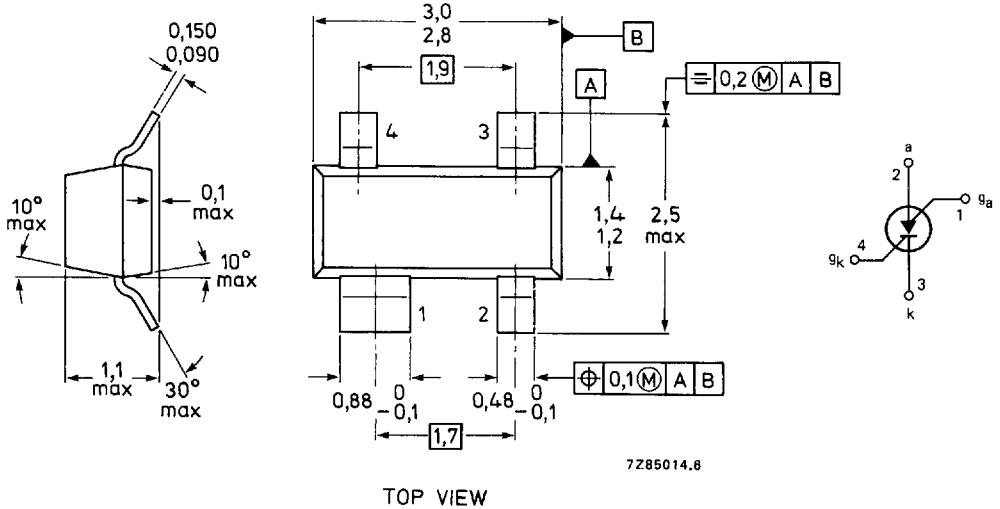
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-143.

Marking code

BRY62 = A51



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Transistor 1 (T1)			
Collector-base voltage (open emitter)	V_{CBO}	max.	70 V
Collector-emitter voltage (R_{BE} = 10 kΩ)	V_{CEO}	max.	70 V
Emitter-collector voltage (I_{C1} = 0)	V_{EBO}	max.	5 V
Average collector current	$I_{C(AV)}$	max.	175 mA▲
Collector current (peak value)	I_{CM}	max.	175 mA**
Average emitter current	$I_{E(AV)}$	max.	175 mA
Emitter current (peak value) t_p = 10 μs; δ = 1%	I_{EM}	max.	2,5 A
Transistor 2 (T2)			
Collector-base voltage (I_{E2} = 0)	$-V_{CBO}$	max.	70 V
Collector-emitter voltage (I_{B2} = 0)	$-V_{CEO}$	max.	70 V
Emitter-base voltage (I_{C2} = 0)	$-V_{EBO}$	max.	70 V
Emitter current (average)	$I_{E(AV)}$	max.	175 mA
Emitter current (peak value) t_p = 10 μs; δ = 1%	I_{EM}	max.	2,5 A
Reverse gate to cathode voltage	$V_{ga\text{-}kR}$	max.	70 V
Gate to anode voltage (open cathode)	$V_{ga\text{-}aO}$	max.	70 V
Gate to cathode voltage (open anode)	$V_{gk\text{-}kO}$	max.	5 V
Average anode current	$I_{A(AV)}$	max.	175 mA
Anode current (peak value) t_p = 10 μs; δ = 1%	I_{AM}	max.	2,5 A
Anode gate current (average)	$I_{GA(AV)}$	max.	175 mA
Anode gate current (peak value)	I_{GAM}	max.	**
Total power dissipation at T_{amb} = 25 °C*	P_{tot}	max.	250 mW
Junction temperature	T_j	max.	150 °C
Storage temperature	T_{stg}	−65 to +	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	500 K/W

* Device mounted on a ceramic substrate of 15 mm x 15 mm x 0,5 mm.

** During switching on, the device can withstand the discharge of a capacitor of maximum value of 500 pF. This capacitor is charged when the transistor is in cut-off condition, with a collector supply voltage of 160 V and a series resistance of 100 kΩ.

▲ Provided the I_E rating is not exceeded.

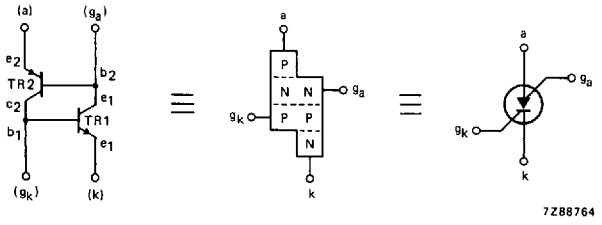


Fig. 2 Circuit diagram.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

Transistor 1 (TR1)

Collector-emitter cut-off current			
V_{CE} = 60 V; R_{BE} = 10 kΩ	I_{CER}	<	100 nA
V_{CE} = 70 V; R_{BE} = 10 kΩ; T_j = 150 °C	I_{CER}	<	10 μA
Emitter cut-off current			
V_{EB} = 5 V; I_C = 0; T_j = 150 °C	I_{EBO}	<	10 μA
Saturation voltages			
I_C = 10 mA; I_B = 1 mA	V_{CEsat}	<	0,5 V
	V_{BEsat}	<	0,9 V
D.C. current gain			
V_{CE} = 2 V; I_C = 10 mA	h_{FE}	>	50
Collector capacitance			
V_{CB} = 20 V; I_E = I_e = 0	C_c	<	5 pF
Emitter capacitance			
V_{EB} = 1 V; I_C = i_c = 0	C_e	<	25 pF
Transition frequency at f = 100 MHz			
V_{CE} = 2 V; I_C = 10 mA	f_T	=	300 MHz

Transistor 2 (TR2)

Collector-emitter cut-off current			
$-V_{CE}$ = 70 V; I_B = 0; T_j = 150 °C	$-I_{CEO}$	<	10 μA
Emitter cut-off current			
$-V_{EB}$ = 70 V; I_C = i_c = 0; T_j = 150 °C	$-I_{EBO}$	<	10 μA
D.C. current gain			
V_{CB} = 0 V; I_E = 1 mA	h_{FE}	0,25 to 2,5	

THYRISTOR

Anode to cathode

On-state voltage

I_A = 50 mA; I_{ga} = 0; R_{gk-k} = 10 kΩ	V_T	<	1,4 V
I_A = 1 mA; I_{ga} = 10 mA; R_{gk-k} = 10 kΩ	V_T	<	1,2 V

Holding current

I_{ga} = 10 mA; $-V_{gk}$ = 2 V; R_{gk-k} = 10 Ω	I_H	<	1 mA

Switching characteristics

Gate-controlled turn-on time ($t_{gt} = t_d + t_r$) when switched from V_{gk} = −0,5 V to 4,5 V

at R_{gk-k} = 1 kΩ	t_{gt}	<	0,25 μs
at R_{gk-k} = 10 kΩ	t_{gt}	<	1,5 μs

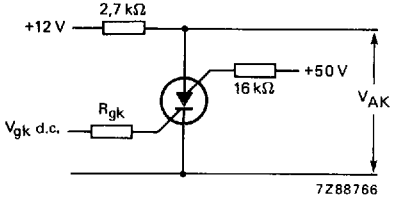


Fig. 3 Switching times test circuit. The pulse time of V_{gk} can be adjusted in such a way that the broken line in Fig. 4 disappears, which means that the thyristor starts triggering.

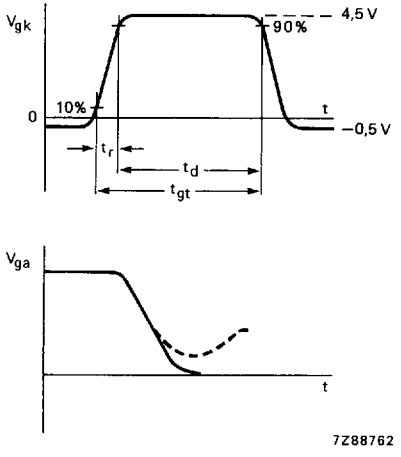


Fig. 4 Switching times waveforms.

Turn-off time (Figs 5 and 6)

R_{gk} = 1 kΩ	t_q	<	5 μs
R_{gk} = 10 kΩ	t_q	<	8 μs
R_{gk} = 10 kΩ; T_j = 125 °C	t_q	<	15 μs

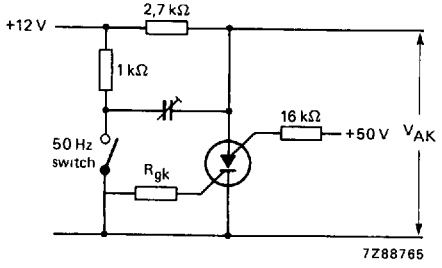


Fig. 5 Switching times test circuit.

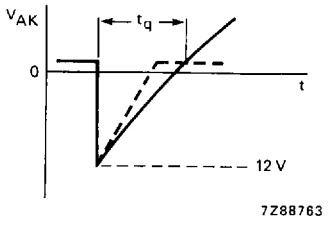


Fig. 6 Switching times waveforms.

The capacitor can be adjusted in such a way that the broken line disappears, which means that the thyristor will not trigger any more.