1.1 Overview

1.1.1 Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for automotive power window, camera, TV, CD, printer, telephone, home appliance, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. MN101EFA7G/A8G/A2G/A3G/G0G have an internal 128 KB of ROM and 6 KB of RAM. MN101EFA7D/A8D/A2D/A3D/G0D have an internal 64 KB of ROM and 4 KB of RAM. Peripheral functions include 5 external interrupts (3 external interrupts in MN101EFAG0G(D)), including NMI, 10 timer counters, 4 types of serial interfaces, A/D converter, watchdog timer and buzzer output. The system configuration is suitable for system control microcontroller.

With 3 oscillation systems (internal frequency: 16 MHz, high-speed crystal/ceramic frequency: max. 10 MHz, low-speed crystal/ceramic frequency: 32.768 kHz) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode) or PLL input (PLL mode), or low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has NORMAL mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in NORMAL mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).

1.1.2 Product Summary

This manual describes the following model.

Table:1.1.1 Product Summary

Model	ROM Size	RAM Size	Classification	Capacitive Touch Detection Circuit	Package
MN101EFA8G	128 KB	6 KB	Flash EEPROM version	√	80 Pin TQFP 80 Pin LQFP
MN101EFA8D	64 KB	4 KB			
MN101EFA3G	128 KB	6 KB	Flash EEPROM version	-	
MN101EFA3D	64 KB	4 KB			
MN101EFA7G	128 KB	6 KB	Flash EEPROM version	√	64 Pin TQFP 64 Pin LQFP
MN101EFA7D	64 KB	4 KB			
MN101EFA2G	128 KB	6 KB	Flash EEPROM version	-	
MN101EFA2D	64 KB	4 KB			
MN101EFG0G	128 KB	6 KB	Flash EEPROM version	-	56 Pin TQFP
MN101EFG0D	64 KB	4 KB			

1.2 Hardware Functions

■ Feature

- Memory Capacity:
  ROM 128 KB / 64 KB
  RAM 6 KB / 4 KB

- Package:
  MN101EFA8/A3 Series
    80-Pin TQFP (12 mm × 12 mm / 0.50 mm pitch, halogen free)
    80-Pin LQFP (14 mm × 14 mm / 0.65 mm pitch, halogen free)

  MN101EFA7/A2 Series
    64-Pin TQFP (10 mm × 10 mm / 0.50 mm pitch, halogen free)
    64-Pin LQFP (14 mm × 14 mm / 0.80 mm pitch)

  MN101EFG0 Series
    56-Pin TQFP (10 mm × 10 mm / 0.65 mm pitch, halogen free)

  Panasonic "halogen free" semiconductor products refer to the products made of molding resin and interposer which conform to the following standards.
    - Bromine : 900 ppm (Maximum Concentration Value)
    - Chlorine : 900 ppm (Maximum Concentration Value)
    - Bromine + Chlorine : 1500 ppm (Maximum Concentration Value)

  The above-mentioned standards are based on the numerical value described in IEC61249-2-21.
  Antimony and its compounds are not added intentionally.

- Machine Cycle:
  High-speed mode 0.05 µs / 20 MHz (4.0 V to 5.5 V)
  Low-speed mode 62.5 µs / 32 kHz (4.0 V to 5.5 V)

- Oscillation circuit: 3 channel oscillation circuit
  Internal oscillation (frc): 16 MHz
  Crystal/ceramic (fosc): Maximum 10 MHz
  Crystal/ceramic (fx): Maximum 32.768 kHz

-Clock Multiplication circuit (PLL Circuit)
  PLL circuit output clock (fpll): fosc multiplied by 2, 3, 4, 5, 6, 8, 10,
  1/2 × frc multiplication by 4, 5 enable

-Clock Gear for System Clock
  System Clock (fs): fpll divided by 1, 2, 4, 16, 32, 64, 128

-Clock Gear for control clock of peripheral function
  Control clock of peripheral function (fpll-div): stop or fpll divided by 1, 2, 4, 8, 16

- Memory Bank:
Expands data memory space by the bank system (by 64 KB, 16 banks)
Source address bank / Destination address bank

- Operation Mode:
NORMAL mode (High-speed mode)
SLOW mode (Low-speed mode)
HALT mode
STOP mode
(The operation clock can be switched in each mode.)

- Operating Voltage: 4.0 V to 5.5 V

- Operation ambient temperature: -40 °C to +85 °C

- Interrupt:
MN101EFA8 Series: 36 interrupts
MN101EFA3 Series: 28 interrupts
MN101EFA7 Series: 32 interrupts
MN101EFA2 Series: 28 interrupts
MN101EFG0 Series: 26 interrupts

<Non-maskable interrupt>
- Non-maskable interrupt and Watchdog timer overflow interrupt

<Timer interrupts>
- Timer 0 interrupt
- Timer 1 interrupt
- Timer 2 interrupt
- Timer 3 interrupt
- Timer 6 interrupt
- Time base timer interrupt
- Timer 7 interrupt
- Timer 7 compare register 2 match interrupt
- Timer 8 interrupt
- Timer 8 compare register 2 match interrupt
- Timer 9 overflow interrupt
- Timer 9 underflow interrupt
- Timer 9 compare register 2 match interrupt

<Serial Interface interrupts>
- Serial interface 0 interrupt
- Serial interface 0 UART reception interrupt
- Serial interface 1 interrupt
- Serial interface 1 UART reception interrupt
- Serial interface 2 interrupt
- Serial interface 2 UART reception interrupt
- Serial interface 4 interrupt
- Serial interface 4 stop condition interrupt

<A/D interrupt>
- A/D conversion interrupt

<External interrupts>
- IRQ0: Edge selectable, noise filter connection available
- IRQ1: Edge selectable, noise filter connection available
- IRQ2: Edge selectable, noise filter connection available, both edges interrupt
- IRQ3: Edge selectable, noise filter connection available, both edges interrupt
- IRQ4: Edge selectable, noise filter connection available, both edges interrupt, Key scan interrupt

<Touch Detect interrupts>
- Touch 0 detect interrupt
- Touch 0 detect error interrupt
- Touch 0 round interrupt
- Touch 0 data transmission interrupt
  (MN101EFA3/A2/G0 Series don't have this function)

- Touch 1 detect interrupt
- Touch 1 detect error interrupt
- Touch 1 round interrupt
- Touch 1 data transmission interrupt
  (MN101EFA7/A3/A2/G0 Series don't have this function)

- Timer Counter: 10 timers
  - 8-bit timer for general use × 4 sets
  - 16-bit timer for general use × 2 sets
  - Motor control 16-bit timer × 1 set
  - 8-bit free-run timer × 1 set
  - Time base timer × 1 set
  - Baud rate timer × 1 set

  Timer 0 (8-bit timer for general use)
  - Square wave output (Timer pulse output)
  - Added pulse (2-bit) type PWM output can be output to large current pin TM0IOA
  - Event count
  - Simple pulse measurement
  - Clock source
    fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fx, External clock, Timer A output

  Timer 1 (8-bit timer for general use)
  - Square wave output (Timer pulse output) can be output to large current pin TM1IOA
  - Event count
  - 16-bit cascade connected (with Timer 0)
  - Clock source
    fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fx, External clock, Timer A output

Timer 2 (8-bit timer for general use)
- Square wave output (Timer pulse output)
- Added pulse (2-bit) type PWM output can be output to large current pin TM2IOA
- Event count
- Simple pulse measurement
- 24-bit cascade connected (with Timer 0 and Timer 1)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fx,
  External clock, Timer A output

Timer 3 (8-bit timer for general use)
- Square wave output (Timer pulse output) can be output to large current pin TM3IOA
- Event count
- 16-bit cascade connected (with Timer 2)
- 32-bit cascade connected (with Timer 0 and Timer 1 and Timer 2)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/128, fs/2, fs/4, fs/8, fx,
  External clock, Timer A output

Timer 6 (8-bit free-run timer, Time base timer)
8-bit free-run timer
- Clock source
  fpll-div, fpll-div/2^{12}, fpll-div/2^{13}, fs, fx, fx/2^{2}, fx/2^{3}, fx/2^{12}, fx/2^{13}

Time base timer
- Interrupt generation cycle
  fpll-div/2^{7}, fpll-div/2^{8}, fpll-div/2^{9}, fpll-div/2^{10}, fpll-div/2^{13}, fpll-div/2^{15}, fx/2^{7}, fx/2^{8}, fx/2^{9}, fx/2^{10}, fx/2^{13}, fx/2^{15}

Timer 7 (16-bit timer for general use)
- Square wave output (Timer pulse output)
- High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM7IOA
- Event count
- Input capture function (Both edges can be operated)
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,
  Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer 8 (16-bit timer for general use)
- Square wave output (Timer pulse output)
- High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM8IOA
- Event count
- Input capture function (Both edges can be operated)
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,
  Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer 9 (Motor control 16-bit timer)
- Square wave output (Timer pulse output) can be output to large current pin TM9IOA
- Event count
- Complementary 3-phase PWM output can be output to large current pin TM9OD0 to TM9OD5
  (Triangle wave and saw tooth wave are supported, dead time insertion available)
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,
  Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer A (Baud rate timer)
- Clock output for peripheral functions
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/16, fpll-div/32, fs/2, fs/4

- Watchdog timer

Time-out cycle can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
On detection of 2 errors, forcibly hard reset inside LSI.
Operation start timing is selectable. (At reset release or write to register)

- Buzzer Output/ Reverse Buzzer Output

Output frequency can be selected from $fpll\text{-}div/2^{9}$, $fpll\text{-}div/2^{10}$, $fpll\text{-}div/2^{11}$, $fpll\text{-}div/2^{12}$, $fpll\text{-}div/2^{13}$, $fpll\text{-}div/2^{14}$, $fx/2^{3}$, $fx/2^{4}$

- A/D Converter: 10-bit × 16 channels (MN101EFA8/A3 Series)
  10-bit × 12 channels (MN101EFA7/A2/G0 Series)

- Serial Interface: 4 channels

Serial 0: UART (full duplex)/ Clock synchronous
Clock synchronous serial interface
- Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
  Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB can be selected as the first bit to be transferred,
  arbitrary sizes of 2 to 8 bits are selectable.
- Sequence transmission, reception or both are available

Full duplex UART
- Baud rate timer, selected from Timer 0 to 3 or Timer A
- Parity check, overrun error/ framing error detection
- Transfer size 7 to 8 bits can be selected

Serial 1: UART (full duplex)/ Clock synchronous
Clock synchronous serial interface
- Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
  Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB can be selected as the first bit to be transferred,
  arbitrary sizes of 2 to 8 bits are selectable.
- Sequence transmission, reception or both are available.

Full duplex UART
- Baud rate timer, selected from Timer 0 to 3 or Timer A
- Parity check, overrun error/ framing error detection
- Transfer size 7 to 8 bits can be selected

Serial 2: UART (full duplex)/ Clock synchronous
Clock synchronous serial interface
- Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 2 to 8 bits are selectable.
- Sequence transmission, reception or both are available.

Full duplex UART
- Baud rate timer, selected from Timer 0 to 3 or Timer A
- Parity check, overrun error/ framing error detection
- Transfer size 7 to 8 bits can be selected

Serial 4: Multi master IIC/ Clock synchronous
Clock synchronous serial interface
- Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/32, fs/2, fs/4, Timer 0 to 3 or Timer A divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 2 to 8 bits are selectable.
- Sequence transmission, reception or both are available.

Multi master IIC
- 7-bit slave address is settable.
- General call communication mode is supported.

- Automatic Reset:
  Power detection level: 4.3 V (at rising), 4.2 V (at falling)

- LED Driver: 8 pins (Port A)

- Touch Sensor Timer: 2 unit/ 12 channels (MN101EFA8 Series only)
  1 unit/ 8 channels (MN101EFA7 Series only)

- Ports (MN101EFA8/A3 Series)

I/O ports	70 pins
Serial Interface pins	21 pins
Timer I/O	19 pins
Buzzer output pins	4 pins
A/D input pins	16 pins
External Interrupt pins	5 pins
LED (large current) driver	8 pins
Touch sensor input pins	12 pins (MN101EFA3 Series does not have this function)
Touch sensor resistor connect pins	4 pins (MN101EFA3 Series does not have this function)
High-speed oscillation	2 pins
Low-speed oscillation	2 pins
Special pins	9 pins
Operation mode input pins	3 pins
Reset input pin	1 pin
Analog reference voltage input pin	1 pin
Power pins	4 pins

- Ports (MN101EFA7/A2 Series)

I/O ports	55 pins
Serial Interface pins	15 pins
Timer I/O	19 pins
Buzzer output	4 pins
A/D input pins	12 pins
External Interrupt pins	5 pins
LED (large current) driver	8 pins
Touch sensor input pins	8 pins (MN101EFA2 Series does not have this function)
Touch sensor resistor connect pins	2 pins (MN101EFA2 Series does not have this function)
High-speed oscillation	2 pins
Low-speed oscillation	2 pins
Special pins	8 pins
Operation mode input pins	3 pins
Reset input pin	1 pin
Analog reference voltage input pin	1 pin
Power pins	3 pins

- Ports (MN101EFG0 Series)

I/O ports	48 pins
Serial Interface pins	12 pins
Timer I/O	15 pins
Buzzer output	4 pins
A/D input pins	12 pins
External Interrupt pins	3 pins
LED (large current) driver	8 pins
High-speed oscillation	2 pins
Low-speed oscillation	2 pins
Special pins	8 pins
Operation mode input pins	3 pins
Reset input pin	1 pin
Analog reference voltage input pin	1 pin
Power pins	3 pins

1.3 Pin Description

1.3.1 Pin configuration

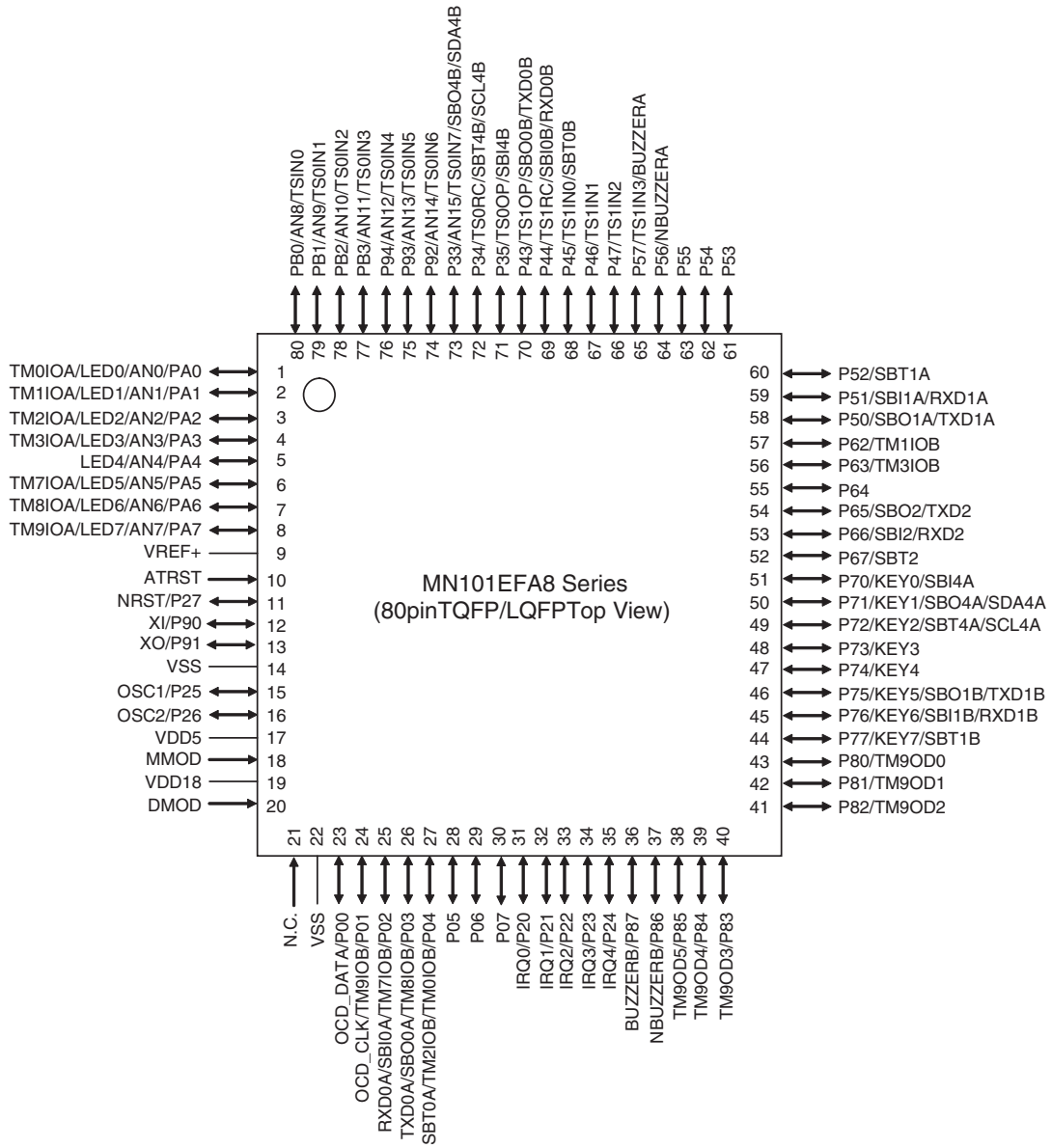

Figure:1.3.1 Pin Configuration (MN101EFA8 Series 80-pin TQFP/LQFP)

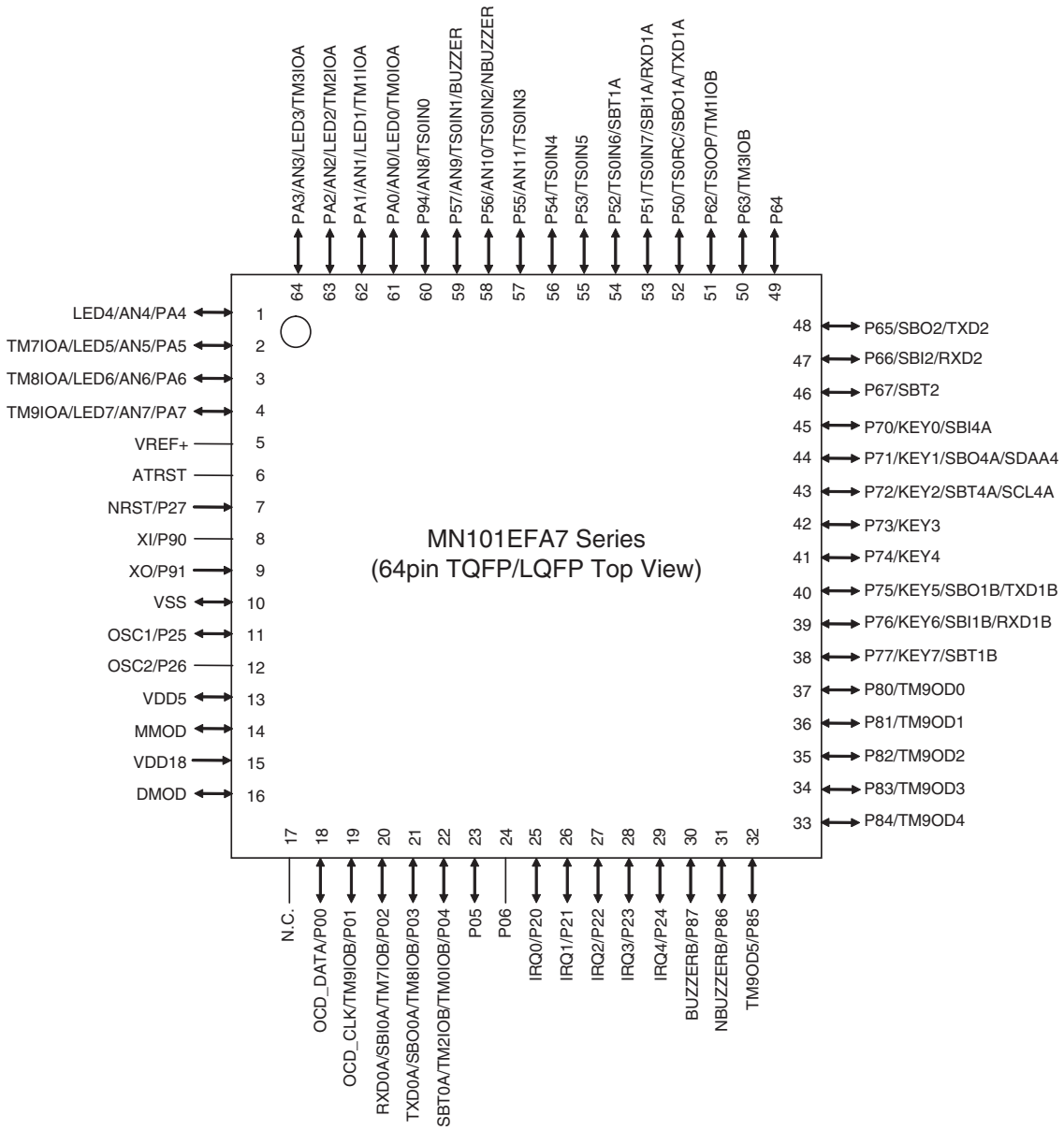

Figure:1.3.2 Pin Configuration (MN101EFA7 Series 64-pin TQFP/LQFP)

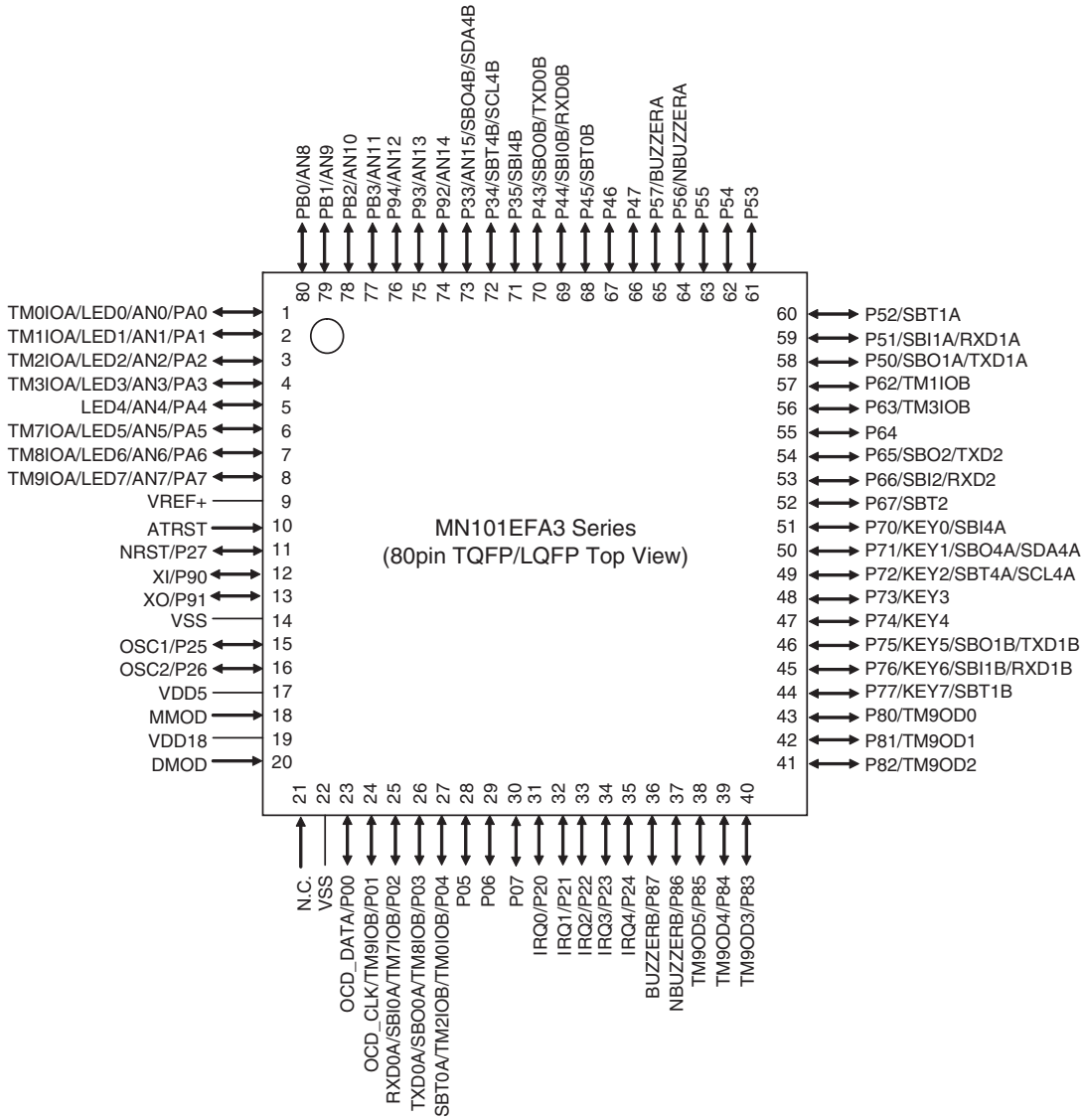

Figure:1.3.3 Pin Configuration (MN101EFA3 Series 80-pin TQFP/LQFP)

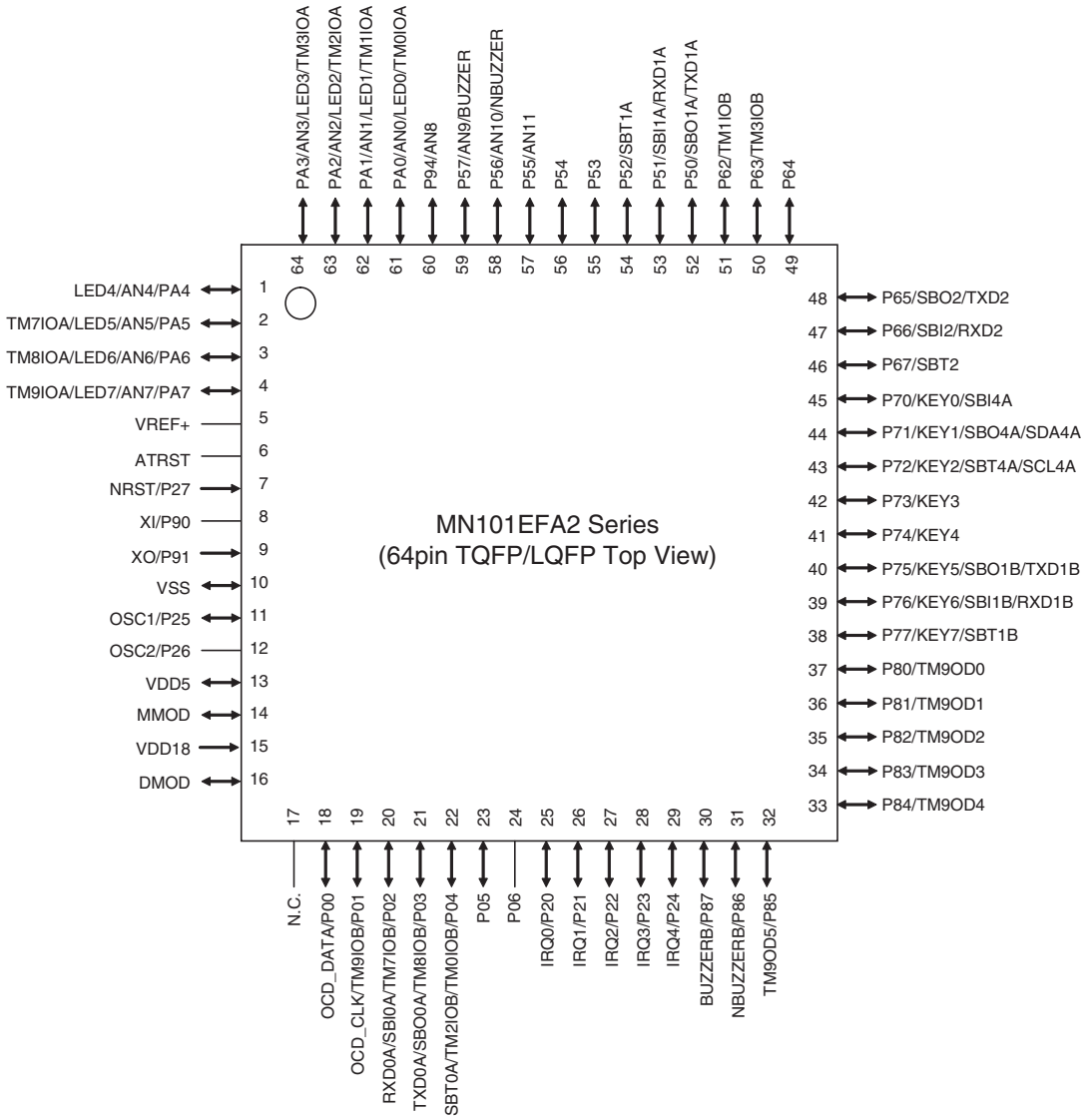

Figure:1.3.4 Pin Configuration (MN101EFA2 Series 64-pin TQFP/LQFP)

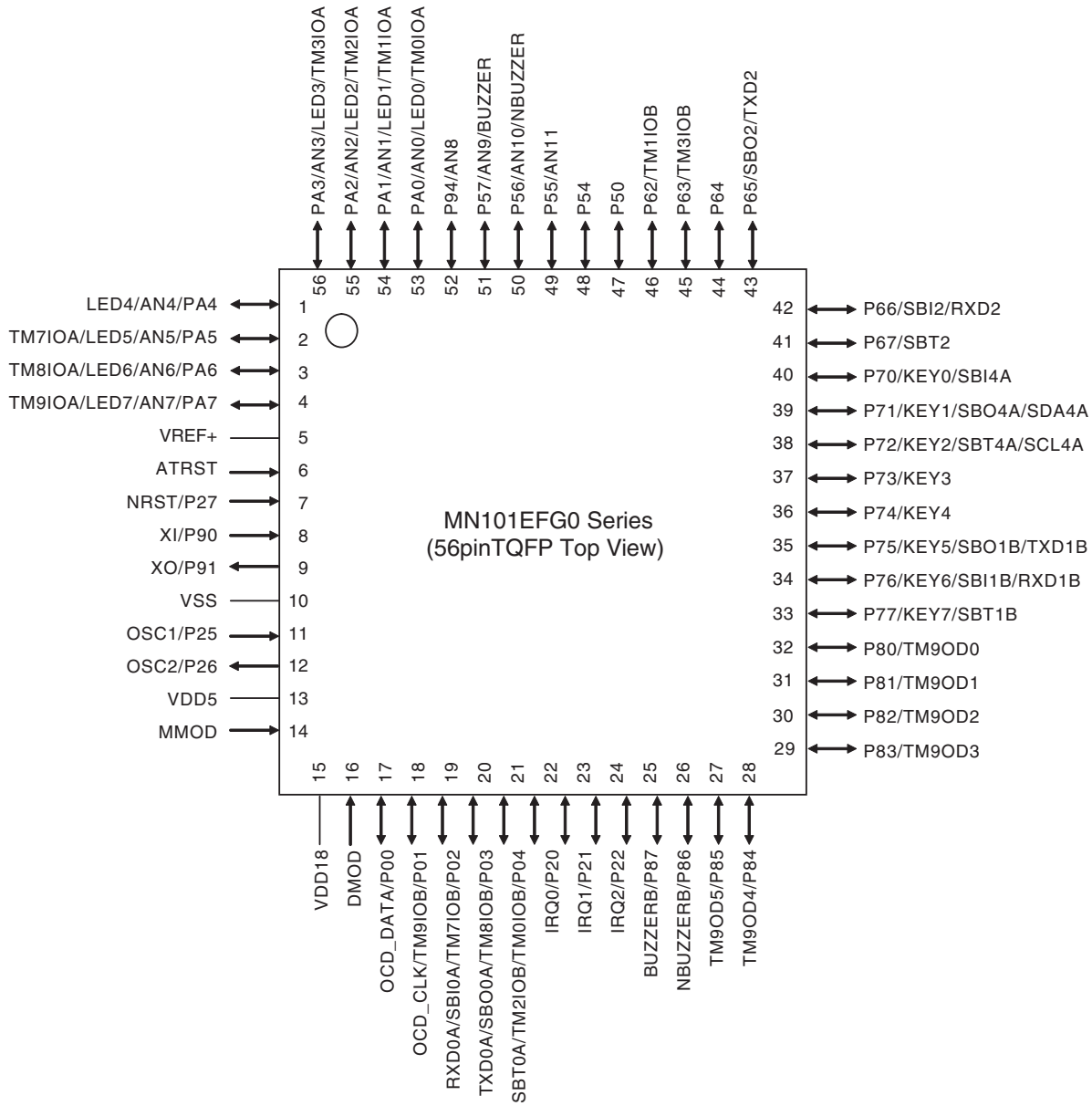

Figure:1.3.5 Pin Configuration (MN101EFG0 Series 56-pin TQFP

1.3.2 Pin Specification

Table remarks √: With function -: Without function

Pins	I/O	Direction Control	Pin Control	Special Functions	Functions Description	MN101EFA8 Series	MN101EFA3 Series	MN101EFA7 Series	MN101EFA2 Series	MN101EFG0 Series
P00	in/out	P0DIR0	P0PLU0	OCD_DATA	On-boad programmer data pin	√	√	√	√	√
P01	in/out	P0DIR1	P0PLU1	TM9IOB	Timer 9 input/output	√	√	√	√	√
				OCD_CLK	On-boad programmer clock supply pin					
P02	in/out	P0DIR2	P0PLU2	TM7IOB	Timer 7 input/output	√	√	√	√	√
				SBI0A	Serial 0 data input					
				RXD0A	UART 0 data input					
P03	in/out	P0DIR3	P0PLU3	TM8IOB	Timer 8 input/output	√	√	√	√	√
				SBO0A	Serial 0 data input/output					
				TXD0A	UART 0 data input/output					
P04	in/out	P0DIR4	P0PLU4	TM0IOB	Timer 0 input/output	√	√	√	√	√
				TM2IOB	Timer 2 input/output					
				SBT0A	Serial 0 clock input/output					
P05	in/out	P0DIR5	P0PLU5	-	-	√	√	√	√	-
P06	in/out	P0DIR6	P0PLU6	-	-	√	√	√	√	-
P07	in/out	P0DIR7	P0PLU7	-	-	√	√	-	-	-
P20	in/out	P2DIR0	P2PLU0	IRQ0	External Interrupt 0	√	√	√	√	√
P21	in/out	P2DIR1	P2PLU1	IRQ1	External Interrupt 1	√	√	√	√	√
P22	in/out	P2DIR2	P2PLU2	IRQ2	External Interrupt 2	√	√	√	√	√
P23	in/out	P2DIR3	P2PLU3	IRQ3	External Interrupt3	√	√	√	√	-
P24	in/out	P2DIR4	P2PLU4	IRQ4	External Interrupt4	√	√	√	√	-
P25	in/out	P2DIR5	P2PLU5	OSC1	Seramic/crystal high-speed clock input	√	√	√	√	√
P26	in/out	P2DIR6	P2PLU6	OSC2	Seramic/crystal high-speed clock output	√	√	√	√	√
P27	in/out	-	-	NRST	Reset	√	√	√	√	√
P33	in/out	P3DIR3	P3PLUD3	SB04B	Serial 4 data input/output	√	√	-	-	-
				SDA4B	Multi-master IIC 4 data input/output					
				AN15	Analog 15 input					
				TS0IN7	Touch sensor 0 input 7		-			
P34	in/out	P3DIR4	P3PLUD4	SBT4B	Serial 4 clock input/output	√	√	-	-	-
				SCL4B	Multi-master IIC 4 clock input/output					
				TS0RC	Touch sensor 0 RC connect		-			
P35	in/out	P3DIR5	P3PLUD5	SBI4B	Serial 4 data input	√	√	-	-	-
				TS0OP	Touch sensor 0 output		-			
P43	in/out	P4DIR3	P4PLU3	SBO0B	Serial 0 data input/output	√	√	-	-	-
				TXD0B	UART 0 data input/output					
				TS1OP	Touch sensor 1 output		-			
P44	in/out	P4DIR4	P4PLU4	SBI0B	Serial 0 data input	√	√	-	-	-
				RXD0B	UART 0 data input					
				TS1RC	Touch sensor 1 RC connect		-			

Table remarks √: With function -: Without function

Pins	I/O	Direction Control	Pin Control	Special Functions	Functions Description	MN101EFA8 Series	MN101EFA3 Series	MN101EFA7 Series	MN101EFA2 Series	MN101EFG0 Series
P45	in/out	P4DIR5	P4PLU5	SBT0B	Serial 0 clock input/output	√	√	-	-	-
				TS1IN0	Touch sensor 1 input 0		-			
P46	in/out	P4DIR6	P4PLU6	-	-	√	√	-	-	-
				TS1IN1	Touch sensor 1 input 1		-			
P47	in/out	P4DIR7	P4PLU7	-	-	√	√	-	-	-
				TS1IN2	Touch sensor 1 input 2		-			
P50	in/out	P5DIR0	P5PLU0 *1 P5PLUD0 *2	SBO1A	Serial 1 data input/output	√	√	√	√	-
				TXD1A	UART 1 data input/output					
				TS0RC	Touch sensor 0 RC connect	-	-	√	-	
P51	in/out	P5DIR1	P5PLU1 *1 P5PLUD1 *2	SBI1A	Serial 1 data input	√	√	√	√	--
				RXD1A	UART 1 data input					
				TS0IN7	Touch sensor 0 input 7	-	-		-	
P52	in/out	P5DIR2	P5PLU2 *1 P5PLUD2 *2	SBT1A	Serial 1 clock input/output	√	√	√	√	-
				TS0IN6	Touch sensor 0 input 6	-	-		-	
P53	in/out	P5DIR3	P5PLU3 *1 P5PLUD3 *2	-	-	√	√	√	√	--
				TS0IN5	Touch sensor 0 input 5	-	-		-	
P54	in/out	P5DIR4	P5PLU4 *1 P5PLUD4 *2	-	-	√	√	√	√	√
				TS0IN4	Touch sensor 0 input 4	-	-		-	-
P55	in/out	P5DIR5	P5PLU5 *1 P5PLUD5 *2	-	-	√	√	√	√	√
				AN11	Analog 11 input	-	-			
				TS0IN3	Touch sensor 0 input 3				-	-
P56	in/out	P5DIR6	P5PLU6 *1 P5PLUD6 *2	NBUZZERA	Buzzer reverse output	√	√	√	√	√
				AN10	Analog 10 input	-	-			
				TS0IN2	Touch sensor 0 input 2				-	-
P57	in/out	P5DIR7	P5PLU7 *1 P5PLUD7 *2	BUZZERA	Buzzer output	√	√	√	√	√
				AN9	Analog 9 input	-				
				TS1IN3	Touch sensor 1 input 3	√	--	-	-	-
				TS0IN1	Touch sensor 0 input 1	-		√		
P62	in/out	P6DIR2	P6PLU2	TM1IOB	Timer 1 input/output	√	√	√	√	√
				TS0OP	Touch sensor 0 output	-	-		-	-
P63	in/out	P6DIR3	P6PLU3	TM3IOB	Timer 3 input/output	√	√	√	√	√
P64	in/out	P6DIR4	P6PLU4	-	-	√	√	√	√	√
P65	in/out	P6DIR5	P6PLU5	SBO2	Serial 2 data input/output	√	√	√	√	√
				TXD2	UART 2 data input/output					
P66	in/out	P6DIR6	P6PLU6	SBI2	Serial 2 data input	√	√	√	√	√
				RXD2	UART 2 data input					
P67	in/out	P6DIR7	P6PLU7	SBT2	Serial 2 clock input/output	√	√	√	√	√
P70	in/out	P7DIR0	P7PLU0	KEY0	Key interrupt 0	√	√	√	√	√
				SBI4A	Serial 4 data input					

*1 MN101EFA8/A3 Series

*2 MN101EFA7/A2/G0 Series

Table remarks √: With function -: Without function

Pins	I/O	Direction Control	Pin Control	Special Functions	Functions Description	MN101EFA8 Series	MN101EFA3 Series	MN101EFA7 Series	MN101EFA2 Series	MN101EFG0 Series
P71	in/out	P7DIR1	P7PLU1	KEY1	Key interrupt 1	√	√	√	√	√
				SBO4A	Serial 4 data input/output					
				SDA4A	Multi-master IIC 4 data input/output					
P72	in/out	P7DIR2	P7PLU2	KEY2	Key interrupt 2	√	√	√	√	√
				SBT4A	Serial 4 clock input/output					
				SCL4A	Multi-master IIC 4 clock input/output					
P73	in/out	P7DIR3	P7PLU3	KEY3	Key interrupt 3	√	√	√	√	√
P74	in/out	P7DIR4	P7PLU4	KEY4	Key interrupt 4	√	√	√	√	√
P75	in/out	P7DIR5	P7PLU5	KEY5	Key interrupt 5	√	√	√	√	√
				SBO1B	Serial 1 data input/output					
				TXD1B	UART 1 data input/output					
P76	in/out	P7DIR6	P7PLU6	KEY6	Key interrupt 6	√	√	√	√	√
				SBI1B	Serial 1 data input					
				RXD1B	UART 1 data input					
P77	in/out	P7DIR7	P7PLU7	KEY7	Key interrupt 7	√	√	√	√	√
				SBT1B	Serial 1 clock input/output					
P80	in/out	P8DIR0	P8PLU0	TM9OD0	Timer 9 output 0	√	√	√	√	√
P81	in/out	P8DIR1	P8PLU1	TM9OD1	Timer 9 output 1	√	√	√	√	√
P82	in/out	P8DIR2	P8PLU2	TM9OD2	Timer 9 output 2	√	√	√	√	√
P83	in/out	P8DIR3	P8PLU3	TM9OD3	Timer 9 output 3	√	√	√	√	√
P84	in/out	P8DIR4	P8PLU4	TM9OD4	Timer 9 output 4	√	√	√	√	√
P85	in/out	P8DIR5	P8PLU5	TM9OD5	Timer 9 output 5	√	√	√	√	√
P86	in/out	P8DIR6	P8PLU6	NBUZZERB	Buzzer reverse output	√	√	√	√	√
P87	in/out	P8DIR7	P8PLU7	BUZZERB	Buzzer output	√	√	√	√	√
P90	in/out	P9DIR0	P9PLUD0	XI	Seramic/crystal low-speed clock input	√	√	√	√	√
P91	in/out	P9DIR1	P9PLUD1	XO	Seramic/crystal low-speed clock output	√	√	√	√	√
P92	in/out	P9DIR2	P9PLUD2	AN14	Analog 14 input	√	√	-	-	-
				TS0IN6	Touch sensor 0 input 6		-			
P93	in/out	P9DIR3	P9PLUD3	AN13	Analog 13 input	√	√	-	-	-
				TS0IN5	Touch sensor 0 input 5		-			
P94	in/out	P9DIR4	P9PLUD4	AN12	Analog 12 input	√	√	-	-	-
				TS0IN4	Touch sensor 0 input 4		-			
				AN8	Analog 8 input	-		√	√	√
				TS0IN0	Touch sensor 0 input 0				-	-
PA0	in/out	PADIR0	PAPLU0	AN0	Analog 0 input	√	√	√	√	√
				LED0	LED driving pin 0					
				TM0IOA	Timer 0 input/output					

Table remarks √: With function -: Without function

Pins	I/O	Direction Control	Pin Control	Special Functions	Functions Description	MN101EFA8 Series	MN101EFA3 Series	MN101EFA7 Series	MN101EFA2 Series	MN101EFG0 Series
PA1	in/out	PADIR1	PAPLU1	AN1	Analog 1 input	√	√	√	√	√
				LED1	LED driving pin 1					
				TM1IOA	Timer 1 input/output					
PA2	in/out	PADIR2	PAPLU2	AN2	Analog 2 input	√	√	√	√	√
				LED2	LED driving pin 2					
				TM2IOA	Timer 2 input/output					
PA3	in/out	PADIR3	PAPLU3	AN3	Analog 3 input	√	√	√	√	√
				LED3	LED driving pin 3					
				TM3IOA	Timer 3 input/output					
PA4	in/out	PADIR4	PAPLU4	AN4	Analog 4 input	√	√	√	√	√
				LED4	LED driving pin 4					
PA5	in/out	PADIR5	PAPLU5	AN5	Analog 5 input	√	√	√	√	√
				LED5	LED driving pin 5					
				TM7IOA	Timer 7 input/output					
PA6	in/out	PADIR6	PAPLU6	AN6	Analog 6 input	√	√	√	√	√
				LED6	LED driving pin 6					
				TM8IOA	Timer 8 input/output					
PA7	in/out	PADIR7	PAPLU7	AN7	Analog 7 input	√	√	√	√	√
				LED7	LED driving pin 7					
				TM9IOA	Timer 9 input/output					
PB0	in/out	PBDIR0	PBPLUD0	AN8	Analog 8 input	√	√	-	-	-
				TS0IN0	Touch sensor 0 input 0		-			
PB1	in/out	PBDIR1	PBPLUD1	AN9	Analog 9 input	√	√	-	-	-
				TS0IN1	Touch sensor 0 input 1		-			
PB2	in/out	PBDIR2	PBPLUD2	AN10	Analog 10 input	√	√	-	-	-
				TS0IN2	Touch sensor 0 input 2		-			
PB3	in/out	PBDIR3	PBPLUD3	AN11	Analog 11 input	√	√	-	-	-
				TS0IN3	Touch sensor 0 input 3		-			

1.3.3 Pin Functions

Table remarks -: Without function

Pins	MN101EF A8/A3 Series	MN101EF A7/A2 Series	MN101EF G0 Series	I/O	Function	Description
VDD5	17	13	13	-	Power connect pins	Apply 4.0 V to 5.5 V to VDD5 and 0 V connect 0.1 μF + 1 μF or larger bypass capacitor for internal power stabilization.
VSS	14, 22	10	10	-		
VDD18	19	15	15	-	Internal power output pin	This pin is output 1.8 V from internal power circuit. Don't use the power supply to external device. For internal power circuit output stability, connect at least 0.1 μF + 1 μF one bypass capacitor between VDD18 and VSS.
OSC1	15	11	11	Input	High speed operation clock input pin	Connect these oscillation pins to ceramic or crystal ocsillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using STOP mode.
OSC2	16	12	12	Output	High speed operation clock output pin	
NRST	11	7	7	I/O	Reset pin [Active low]	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Typ. 50 kΩ). Setting this pin low initialize the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. If a capacitor is to be inserted between NRST and VSS, it is recommended that a discharge diode be placed between NRST and VDD5.
ATRST	10	6	6	input	Auto reset setting pin	Input "High" to enable auto reset function and "Low" to disable this function
P00	23	18	17	I/O	I/O port 0	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P0DIR register. A pull-up resistor for each bit can be selected individually by P0PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P01	24	19	18			
P02	25	20	19			
P03	26	21	20			
P04	27	22	21			
P05	28	23	-			
P06	29	24	-			
P07	30	-	-			
P20	31	25	22	I/O	I/O port 2	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P2DIR register. A pull-up resistor for each bit can be selected individually by P2PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance)
P21	32	26	23			
P22	33	27	24			
P23	34	28	-			
P24	35	29	-			
P25	15	11	11			
P26	16	12	12			
P27	11	7	7	input	input port 2	P27 has an N-channel open-drain configuration.
P33	73	-	-	I/O	I/O port 3	3-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P3DIR register. A pull-up /pull-down resistor for each bit can be selected individually by P3PLUD register. A pull-up/down resistor connection for each port can be selected individually in SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P34	72	-	-			
P35	71	-	-			
P43	70	-	-	I/O	I/O port 4	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P4DIR register. A pull-up resistor for each bit can be selected individually by P4PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P44	69	-	-			
P45	68	-	-			
P46	67	-	-			
P47	66	-	-			

Table remarks -: Without function

Pins	MN101EFA8/A3 Series	MN101EFA7/A2 Series	MN101EFG0 Series	I/O	Function	Description
P50	58	52	47	I/O	I/O port 5	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P5DIR register. A pull-up /pull-down resistor for each bit can be selected individually by P5PLUD register. A pull-up/down resistor connection for each port can be selected individually in SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistor is disabled (high impedance). Pull-down function is not equipped in MN101EFA8/A3 Series.
P51	59	53	-			
P52	60	54	-			
P53	61	55	-			
P54	62	56	48			
P55	63	57	49			
P56	64	58	50			
P57	65	59	51			
P62	57	51	46	I/O	I/O port 6	6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P6DIR register. A pull-up resistor for each bit can be selected individually by P6PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P63	56	50	45			
P64	55	49	44			
P65	54	48	43			
P66	53	47	42			
P67	52	46	41			
P70	51	45	40	I/O	I/O port 7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P7DIR register. A pull-up resistor for each bit can be selected individually by P7PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P71	50	44	39			
P72	49	43	38			
P73	48	42	37			
P74	47	41	36			
P75	46	40	35			
P76	45	39	34			
P77	44	38	33			
P80	43	37	32	I/O	I/O port 8	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P8DIR register. A pull-up resistor for each bit can be selected individually by P8PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P81	42	36	31			
P82	41	35	30			
P83	40	34	29			
P84	39	33	28			
P85	38	32	27			
P86	37	31	26			
P87	36	30	25			
P90	12	8	8	I/O	I/O port 9	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P9DIR register. A pull-up /pull-down resistor for each bit can be selected individually by P9PLUD register. A pull-up/down resistor connection for each port can be selected individually in SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P91	13	9	9			
P92	74	-	-			
P93	75	-	-			
P94	76	60	52			
PA0	1	61	53	I/O	I/O port A	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by PADIR register. A pull-up resistor for each bit can be selected individually by PAPLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
PA1	2	62	54			
PA2	3	63	55			
PA3	4	64	56			
PA4	5	1	1			
PA5	6	2	2			
PA6	7	3	3			
PA7	8	4	4			

Table remarks -: Without function

Pins	MN101EFA8/A3 Series	MN101EFA7/A2 Series	MN101EFG0 Series	I/O	Function	Description
PB0	80	-	-	I/O	I/O port B	4-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by PBDIR register. A pull-up /pull-down resistor for each bit can be selected individually by PBPLUD register. A pull-up/down resistor connection for each port can be selected individually in SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
PB1	79	-	-			
PB2	78	-	-			
PB3	77	-	-			
SBO0A	26	21	20	Output	Serial interface transmission data output pins	Transmission data output pins for serial interface 0,1,2,4. The output configuration, either COMS push-pull or Nch open-drain can be selected in P0ODC, P3ODC, P4ODC, P5ODC, P6ODC and P7ODC registers. Pull-up resistor can be selected in P0PLU, P3PLUD, P4PLU, P5PLU(D), P6PLU, and P7PLU registers. Select output mode in P0DIR, P3DIR, P4DIR, P5DIR, P6DIR, and P7DIR registers and set serial data output mode in serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC4MD1). These can be used as normal I/O pins when serial interface is not used.
SBO0B	70	-	-			
SBO1A	58	52	-			
SBO1B	46	40	35			
SBO2	54	48	43			
SBO4A	50	44	39			
SBO4B	72	-	-			
SBI0A	25	20	19	Input	Serial interface reception data input pins	Reception data input pins for serial interface 0,1,2,4. Pull-up resistor can be selected in P0PLU, P3PLUD, P4PLU, P5PLU(D), P6PLU and P7PLU registers. Select the output mode in P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and select serial data input mode in serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC4MD1). These can be used as normal I/O pins when serial interface is not used.
SBI0B	69	-	-			
SBI1A	59	53	-			
SBI1B	45	39	34			
SBI2	53	47	42			
SBI4A	51	45	40			
SBI4B	71	-	-			
SBT0A	27	22	21	I/O	Serial interface Clock I/O pins	Clock I/O pins for serial interface 0,1,2,4. The output configuration, either COMS push-pull or Nch open-drain can be selected in P0ODC, P3ODC, P4ODC, P5ODC, P6ODC and P7ODC registers. Pull-up resistor can be selected in P0PLU, P3PLUD, P4PLU, P5PLU(D), P6PLU and P7PLU registers. Select clock I/O in P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC4MD1) with the communication mode. These can be used as normal I/O pins when serial interface is not used.
SBT0B	68	-	-			
SBT1A	60	54	-			
SBT1B	44	38	33			
SBT2	52	46	41			
SBT4A	49	43	38			
SBT4B	72	-	-			
TXD0A	26	21	20	Output	UART transmission data output pins	In serial interface 0,1,2 in UART mode, this pin is configured as the transmission data output pin. The output configuration, either COMS push-pull or Nch open-drain can be selected in P0ODC, P4ODC, P5ODC, P6ODC and P7ODC registers. Pull-up resistor can be selected by P0PLU, P4PLU, P5PLU(D), P6PLU and P7PLU registers. Select the output mode in P0DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and select serial data output mode in serial mode register 1 (SC0MD1, SC1MD1, SC2MD1). These can be used as normal I/O pins when serial interface is not used.
TXD0B	70	-	-			
TXD1A	58	52	-			
TXD1B	46	40	35			
TXD2	54	48	43			
RXD0A	25	20	19	Input	UART reception data output pins	In serial interface 0,1,2 in UART mode, this pin is configured as the reception data input pin. Pull-up resistor can be selected in P0PLU, P4PLU, P5PLU(D), P6PLU and P7PLU registers. Select the input mode in P0DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and select serial input in serial mode register 1 (SC0MD1, SC1MD1, SC2MD1). These can be used as normal I/O pins when serial interface is not used.
RXD0B	69	-	-			
RXD1A	59	53	-			
RXD1B	45	39	34			
RXD2	53	47	42			
SDA4A	50	44	39	I/O	IIC data I/O pins	In serial interface 4 in IIC mode, this pin is configured as the data I/O pin. For the output configuration, select Nch open-drain in P3ODC and P7ODC register and set pull-up resistor in P3PLUD and P7PLU register. Select the output mode in P0DIR register and select serial data I/O mode by serial mode register 1 (SC4MD1). These can be used as normal I/O pin when serial interface is not used.
SDA4B	72	-	-			
SCL4A	49	43	38	I/O	IIC clock I/O pins	In serial interface 4 in IIC mode, this pin is configured as the clock I/O pin. For the output configuration, select Nch open-drain in P0ODC and P7ODC register and set pull-up resistor by P0PLU and P7PLU register. Select the output mode at P0DIR register and select serial clock I/O mode in serial mode register 1 (SC4MD1). These can be used as normal I/O pin when serial interface is not used
SCL4B	72	-	-			

Table remarks -: Without function

Pins	MN101EFA8/A3 Series	MN101EFA7/A2 Series	MN101EFG0 Series	I/O	Function	Description
TM0IOA	1	61	53	I/O	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 8-bit timer 0 to 3. To use this pin as event clock input, configure it as input by P0DIR, P6DIR and PADIR register. In the input mode, pull-up resistor can be selected in P0PLU, P6PLU, and PAPLU registers. For timer output, PWM signal output, select the special function pin in P0OMD1, P0OMD2, P6OMD and PAOMD registers, and set to the output mode in P0DIR, P6DIR and PADIR registers. These can be used as normal I/O pins when Timer I/O pin is not used.
TM0IOB	27	22	21			
TM1IOA	2	62	54			
TM1IOB	57	51	46			
TM2IOA	3	63	55			
TM2IOB	27	22	21			
TM3IOA	4	64	56			
TM3IOB	56	50	45			
BUZZERA	65	59	51	Output	Buzzer output pins	Piezoelectric buzzer driving pin. Buzzer output is available to Port 5, 8. The driving frequency can be set in DLYCTR register. In order to select Buzzer output, select the special function pin in P5OMD, P8OMD register, and set P5DIR, P8DIR register to the output mode. At the same time, select Buzzer output in oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when Buzzer output is not used.
BUZZERB	36	30	25			
NBUZZERA	64	58	50			
NBUZZERB	37	31	26			
TM7IOA	6	2	2	I/O	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer7,8 and 9. To use this pin as event clock input, configure it as input with P0DIR and PADIR registers. In the input mode, pull-up resistor can be selected by P0PLU and PAPLU registers. For timer output, PWM signal output, select the special function pin in P0OMD1 and PAOMD registers, and set to the output mode in P0DIR and PADIR registers. These can be used as normal I/O pins when not used as timer I/O pins.
TM7IOB	25	20	19			
TM8IOA	7	3	3			
TM8IOB	26	21	20			
TM9IOA	8	4	4			
TM9IOB	24	19	18			
TM9OD0	43	37	32	Output	Timer PWM output	PWM signal output pin for 16-bit timer 9. Select the special function pin in P8OMD register, and set to the output mode in P8DIR register. These can be used as normal I/O pins when not used as timer I/O pins.
TM9OD1	42	36	31			
TM9OD2	41	35	30			
TM9OD3	40	34	29			
TM9OD4	39	33	28			
TM9OD5	38	32	27			
VREF+	9	5	5	-	A/D reference voltage input pin	Reference power supply pin for A/D converter. Normally, the values of $V_{REF+} = V_{DD5}$ is used.
AN0	1	61	53	input	Analog input pins	[MN101EFA8/A3 Series] Analog input pins for 16-channel, 10-bit A/D converter. Select the analog input by P3IMD, P9IMD, PAIMD, PBIMD register. When not used for analog input, these pins can be used as normal input pins. [MN101EFA7/A2/G0 Series] Analog input pins for 12-channel, 10-bit A/D converter. Select the analog input by P5IMD, P9IMD, PAIMD register. When not used for analog input, these pins can be used as normal input pins.
AN1	2	62	54			
AN2	3	63	55			
AN3	4	64	56			
AN4	5	1	1			
AN5	6	2	2			
AN6	7	3	3			
AN7	8	4	4			
AN8	80	60	52			
AN9	79	59	51			
AN10	78	58	50			
AN11	77	57	49			
AN12	76	-	-			
AN13	75	-	-			
AN14	74	-	-			
AN15	73	-	-			

Table remarks -: Without function

Pins	MN101EFA8/A3 Series	MN101EFA7/A2 Series	MN101EFG0 Series	I/O	Function	Description
IRQ0	31	25	22	Input	External interrupt	External interrupt input pins. Select the external interrupt input enable by IRQCNT register. The valid edge for IRQ0 to 4 can be selected with IRQnICR register. IRQ2 to 4 can be set at both edges at pin voltage level. When not used for interrupts, these can be used as normal input pins.
IRQ1	32	26	23			
IRQ2	33	27	24			
IRQ3	34	28	-			
IRQ4	35	29	-			
KEY0	51	45	40	Input	Key interrupt input pins	Input pins for KEY interrupt based on OR condition result of pin inputs. These can be set to key input pins by 1-bit with KEY interrupt control register (KEYT3_1IMD, KEY3_2_IMD). When not used for KEY input, these pins can be used as normal I/O pins.
KEY1	50	44	39			
KEY2	49	43	38			
KEY3	48	42	37			
KEY4	47	41	36			
KEY5	46	40	35			
KEY6	45	39	34			
KEY7	44	38	33			
LED0	1	61	53	Output	LED drive pins	Large current output pins. Select the large current output by LEDCNT registers. When not used for LED output, these pins can be used as normal I/O pins.
LED1	2	62	54			
LED2	3	63	55			
LED3	4	64	56			
LED4	5	1	1			
LED5	6	2	2			
LED6	7	3	3			
LED7	8	4	4			
DMOD	20	16	15	Input	Mode switch input pins	Set always to V_{DD5} level.
MMOD	18	14	14	Input	ROM area switch input pins at start	Set always to V_{SS} level.
TS0IN0	80	60	-	Input	Touch sensor input pins These pins are not equipped in MN101EFA3 Series, MN101EFA2 Series and MN101EFG0 Series.	Input pins for Touch Sensor Timer of 12 channels (8 channels of MN101EFA7 Series). Set "Used" to corresponding channel by TS0TCHSEL, TS1TCHSEL register. This setup is available regardless of the setting of port control registers. These can be used as normal I/O pins when Touch Sensor Timer is not used.
TS0IN1	79	59	-			
TS0IN2	78	58	-			
TS0IN3	77	57	-			
TS0IN4	76	56	-			
TS0IN5	75	55	-			
TS0IN6	74	54	-			
TS0IN7	73	53	-			
TS1IN0	68	-	-			
TS1IN1	67	-	-			
TS1IN2	66	-	-			
TS1IN3	65	-	-			
TS0RC	72	52	-	Input	Touch sensor resistor connect pins. These pins are not equipped in MN101EFA3 Series, MN101EFA2 Series and MN101EFG0 Series.	These are used in the following cases. 1. External resistor connection for Touch Sensor Timer Set both TS0MD, TS1MD and RS0MD, RS1MD of TS0TMD, TS1TMD register to "1". 2. The capacitor/resistor connection for Touch Sensor using A/D converter Set TS0ADCNT, TS1ADCNT register. This setup is available regardless of the setting of port control registers. These can be used as normal I/O pins when Touch Sensor Timer is not used.
TS1RC	69	-	-			
TS0OP	71	51	-	Output		
TS1OP	70	-	-			

For the MMOD setup in rewriting the flash memory, refer to [Chapter 16 16.5 User Mode Microcontroller Rewriting], [Chapter 16 16.6 BOOT Mode Microcontroller Rewriting], [Chapter 16 16.7 Appendix].

1.4 Block Diagram

1.4.1 Block Diagram

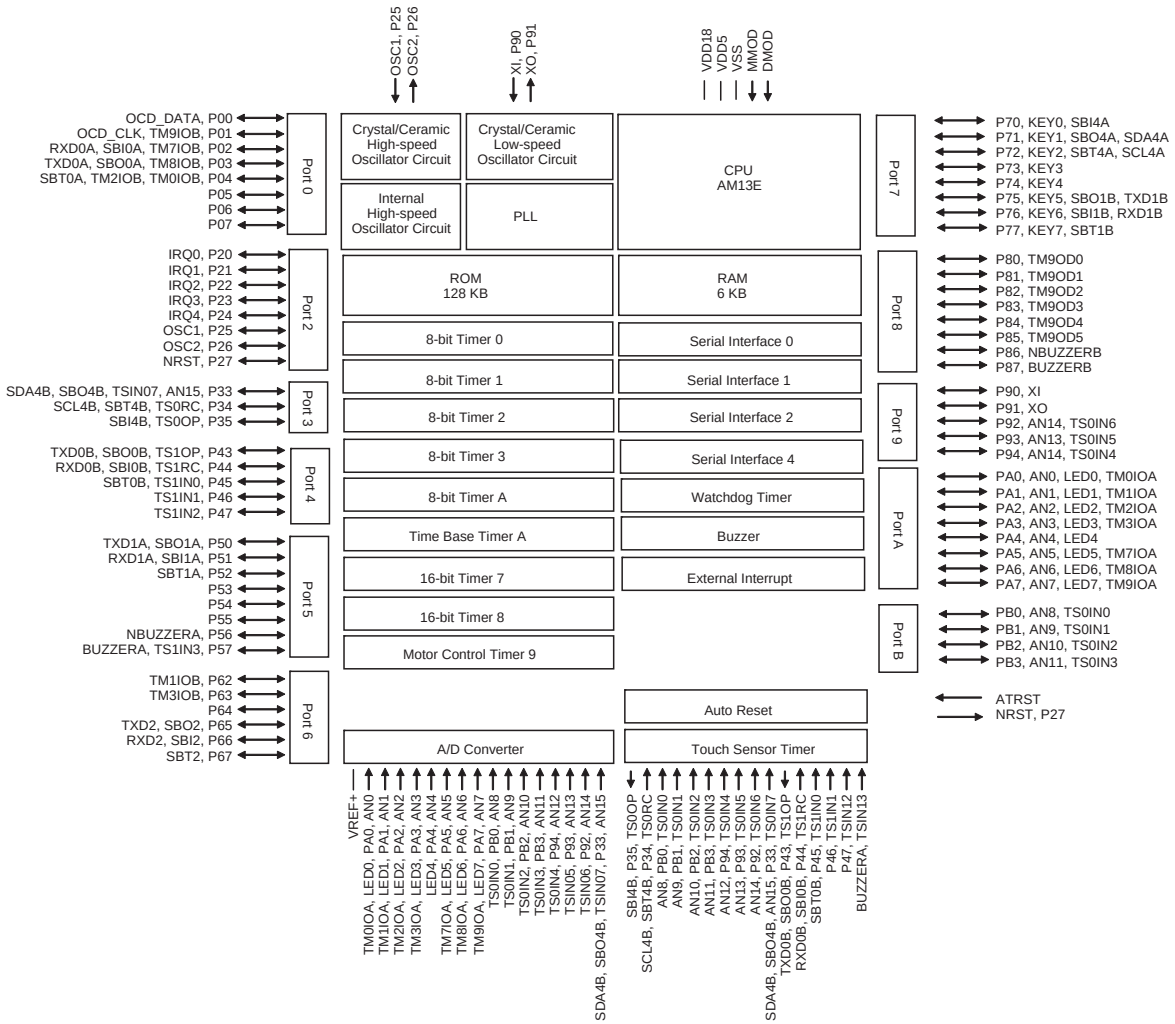

Figure:1.4.1 Block Diagram

* Varies depending on models.
  Refer to [Chapter 1.1.2 Product Summary] and [Chapter 1.3.3 Pin Functions].

1.5 Electrical Characteristics

This LSI manual describes standard specifications.

When using this LSI, consult our sales offices for the product specifications.

Structure	CMOS integrated circuit
Application	General-purpose
Function	CMOS 8-bit single chip microcomputer

1.5.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings *2 *3 *4 V_{SS} = 0 V

	Parameter		Symbol	Rating	Unit
A1	Power supply voltage		V_{DD5}	-0.3 to +7.0	V
A2	Power supply voltage		V_{DD18}	-0.3 to +2.5	
A3	Input pin voltage		V_I	-0.3 to V_{DD5} +0.3 (upper limit: 7.0 V)	
A4	Output pin voltage		V_O	-0.3 to V_{DD5} +0.3 (upper limit: 7.0 V)	
A5	I/O pin voltage		V_{IO1}	-0.3 to V_{DD5} +0.3 (upper limit: 7.0 V)	
A6	Peak output current	LED output	I_{OL1} (peak)	30	mA
A7		Other than LED output	I_{OL2} (peak)	20	
A8		All pins	I_{OH} (peak)	-10	
A9	Average output current *1	LED output	I_{OL1} (avg)	20	
A10		Other than LED output	I_{OL2} (avg)	15	
A11		All pins	I_{OH} (avg)	-5	
A12	Power dissipation		P_D	400	mW
A13					
A14					
A15					
A16	Operating ambient temperature		T_{opr}	-40 to +85	°C
A17	Storage temperature		T_{STG}	-55 to +125	

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 0.1 μF + 1.0 μF or larger between VDD5 pin and GND for the internal power voltage stabilization.

*3 Connect appropriate capacitor about 0.1 μF + 1.0 μF between VDD18 pin and VSS pin, near the microcontroller according to the Figure:1.5.1 shown below for the internal power supply stabilization.

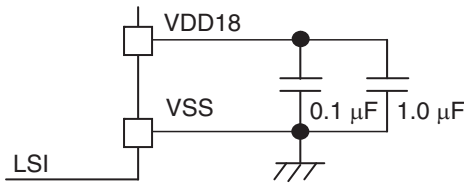

Figure:1.5.1 Capacitor Connection between VDD18 and VSS Pins

*4 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

1.5.2 Operating Conditions

B. Operating Conditions

V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage *5							
B1	Power supply voltage	V_{DD1}		4.0		5.5	V
B2	RAM retention power supply voltage	V_{DD2}	During STOP mode	2.2		5.5	
Operating speed *6							
B3	Instruction execution time fs	t_{c1}	V_{DD5} = 4.0 V to 5.5 V (When ROMHND of HANDSHAKE register is “1”.)	0.05			µs
B4		t_{c2}	V_{DD5} = 4.0 V to 5.5 V (When ROMHND of HANDSHAKE register is “0”.)	0.10			
B5		t_{c3}	V_{DD5} = 4.0 V to 5.5 V	61			

*5 fs: Machine clock frequency

*6 tc1 to 2 : when the machine clock is selected from external high-speed oscillation, internal high-speed oscillation, or both the oscillations multiplied by PLL.

tc7: when the machine clock is selected from external low-speed oscillation.

External Oscillator 1 Figure:1.5.2

B6	Frequency	f_{hosc1}	V_{DD5} is within the specified operating power supply voltage range. (Refer to the ratings of B1 to B2 for the operating supply voltage range)	2.0		10	MHz
B7	Internal feedback resistor	R_{f10}	V_{DD5} = 5.0 V		980		kΩ

External Oscillator 2 Figure:1.5.2

B8	Frequency	f_{sosc1}	V_{DD5} = 4.0 V to 5.5 V		32.768		kHz
B9	Internal feedback resistor	R_{f20}	V_{DD5} = 5.0 V		6.2		MΩ

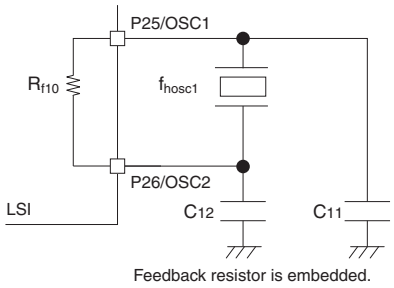

Figure:1.5.2 External Oscillator 1

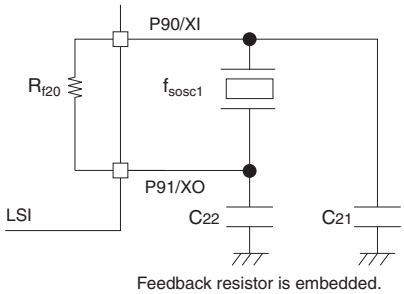

Figure:1.5.3 External Oscillator 2

Connect external capacitors suited for the used oscillator.
The reference value denotes external capacity value based on our matching result.
When crystal oscillator or ceramic oscillator is used, the oscillation frequency is changed depending on the value of capacitor. For external capacity value, please consult the oscillator manufacturer and perform matching tests enough for determining appropriate values.

V_{DD5} = 4.0 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected)							
B10	Clock frequency	f_{hosc2}		2		10.0	MHz
B11	High-level pulse width *7	t_{wh1}	Figure:1.5.4	45			ns
B12	Low-level pulse width *7	t_{wl1}		45			
B13	Rising time	t_{wr1}	Figure:1.5.4	0		5.0	
B14	Falling time	t_{wf1}		0		5.0	

*7 The clock duty ratio should be 45 % to 55 %

External clock input 2 XI (XO is unconnected)

B15	Clock frequency	f_{sosc2}			32.768		kHz
B16	High-level pulse width *7	t_{wh2}	Figure:1.5.5		4.5		µs
B17	Low-level pulse width *7	t_{wl2}			4.5		µs
B18	Rising time	t_{wr2}	Figure:1.5.5	0		20	ns
B19	Falling time	t_{wf2}		0		20	ns

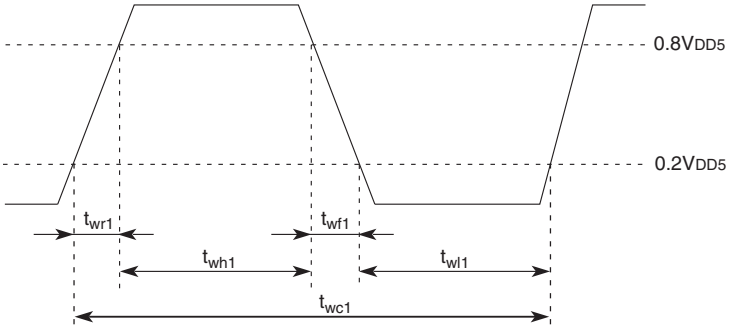

Figure:1.5.4 OSC1 Timing Chart

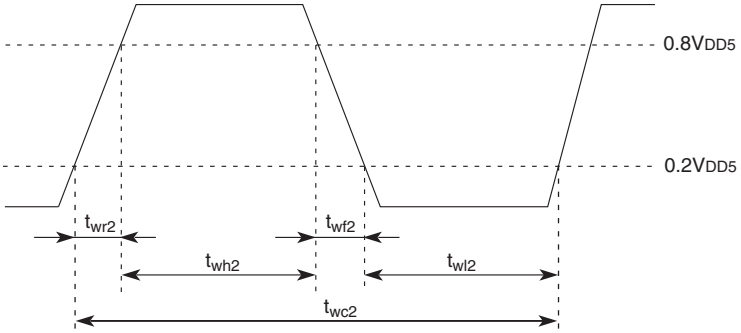

Figure:1.5.5 XI Timing Chart

1.5.3 DC Characteristics

C. DC Characteristics

V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current *8							
C1	Power supply current during operation	I_{DD1}	V_{DD5}=5 V fosc=10 MHz [Double-speed mode: fs=fosc] (PLL is not used) *9		5	14	mA
C2		I_{DD2}	V_{DD5}=5 V fosc=10 MHz [Multiplied by 2, Divided by 2: fs=fosc] (PLL is used) *9		6	18	
C3		I_{DD3}	V_{DD5}=5 V fosc=10 MHz [Multiplied by 2: fs=20 MHz] (PLL is used) *9		9	20	
C4		I_{DD4}	V_{DD5}=5 V frc=16 MHz [Double-speed mode: fs=16 MHz] (PLL is not used) *9		6	15	
C5	Power supply current during operation	I_{DD5}	V_{DD5}=5 V fx=32.768 kHz [fs=fx/2]		200	400	µA
C6	Power supply current during STOP mode	I_{DD6}	V_{DD5}=5 V		145	245	µA

*8 Measured without loading (pull-up and pull-down resistors are not connected.)

To measure the power supply current during operation I_{DD1} to I_{DD4};
1. Set all I/O pins to input mode,
2. Set the CPU mode to “NORMAL mode”,
3. Fix pin MMOD to V_{SS} level and input pins to V_{DD5} level
4. Input the rectangular wave of 10 MHz with amplitude of V_{DD5} and V_{SS}, from pin OSC1.

To measure the power supply current during SLOW mode I_{DD5};
1. Set all I/O pins to input mode
2. Set the CPU mode to "SLOW mode"
3. Fix the MMOD to V_{SS} level and input pins to V_{DD5} level

To measure the power supply current during STOP mode I_{DD6};
1. Set the CPU mode to “STOP mode”,
2. Fix pin MMOD to V_{SS} level and input pin to V_{DD5} level
3. Open pin OSC1.

*9 When ROMHND of HANDSHAKE register is set to “1”

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 ATRST, MMOD							
C7	Input high voltage	V_{IH1}		$0.8V_{DD5}$		V_{DD5}	V
C8	Input low voltage	V_{IL1}		0		$0.2V_{DD5}$	
C9	Input leakage current	I_{LK1}	V_{IN} = 0 V to V_{DD5}			± 2	μA
Input pin 2 P27/NRST							
C10	Input high voltage	V_{IH2}		$0.8V_{DD5}$		V_{DD5}	V
C11	Input low voltage	V_{IL2}		0		$0.15V_{DD5}$	
C12	Pull-up resistor	R_{RH2}	V_{DD5}=5 V, V_{IN}= V_{SS}	10	50	100	kΩ

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 3 P00 to P07, P20 to P26, P43 to P47, P50 to P57, P62 to P67, P70 to P77, P80 to P87 (MN101EFA8/A3 Series) P00 to P06, P20 to P26, P62 to P67, P70 to P77, P80 to P87 (MN101EFA7/A2 Series) P00 to P04, P20 to P22, P25, P26, P62 to P67, P70 to P77, P80 to P87 (MN101EFG0 Series)							
C13	Input high voltage	V_{IH3}		0.8V_{DD5}		V_{DD5}	V
C14	Input low voltage	V_{IL3}		0		0.2V_{DD5}	
C15	Input leakage current	I_{LK3}	V_{IN}=0 V to V_{DD5}			± 2	µA
C16	Pull-up resistor	R_{RH3}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C17	Output high voltage	V_{OH3}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C18	Output low voltage	V_{OL3}	V_{DD5}=5.0 V, I_{OL}=1.0 mA			0.5	
Input pin 4 PA0 to PA7							
C19	Input high voltage	V_{IH4}		0.8V_{DD5}		V_{DD5}	V
C20	Input low voltage	V_{IL4}		0		0.2V_{DD5}	
C21	Input leakage current	I_{LK4}	V_{IN}=0 V to V_{DD5}			± 2	µA
C22	Pull-up resistor	R_{RH4}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C23	Output high voltage	V_{OH4}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C24	Output low voltage 1	V_{OL41}	V_{DD5}=5.0 V, I_{OL}=1.0 mA LED output OFF			0.5	
C25	Output low voltage 2	V_{OL42}	V_{DD5}=5.0 V, IOL=15.0 mA LED output ON			1.0	
Input pin 5 P33 to P35, P90 to P94, PB0 to PB3 (MN101EFA8/A3 Series) P50 to P57, P90, P91, P94 (MN101EFA7/A2 Series) P50 , P54 to P57, P90, P91, P94 (MN101EFG0 Series)							
C26	Input high voltage	V_{IH5}		0.8V_{DD5}		V_{DD5}	V
C27	Input low voltage	V_{IL5}		0		0.2V_{DD5}	
C28	Input leakage current	I_{LK5}	V_{IN}=0 V to V_{DD5}			± 2	µA
C29	Pull-up resistor	R_{RH5}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C30	Pull-down resistor	R_{RL5}	V_{DD5}=5.0 V, V_{IN}=V_{DD5} Pull-down resistor ON	10	50	100	
C31	Output high voltage	V_{OH5}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C32	Output low voltage	V_{OL5}	V_{DD5}=5.0 V, I_{OL}=1.0 mA			0.5	

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 6 DMOD							
C33	Input high voltage	V_{IH6}		$0.8V_{DD5}$		V_{DD5}	V
C34	Input low voltage	V_{IL6}		0		$0.2V_{DD5}$	
C35	Pull-up resistor	R_{RH6}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ

1.5.4 A/D Converter Characteristics

D. A/D Converter Characteristics *11

V_{DD5} = 5.0 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D1	Resolution					10	Bits
D2	Non-linearity error 1		V_{DD5}=5.0 V, V_{SS}=0 V V_{REF+}=5.0 V T_{AD}=800 ns			± 3	LSB
D3	Differential non-linearity error 1					± 3	
D4	Zero transition voltage		V_{DD5}=5.0 V, V_{SS}=0 V V_{REF+}=5.0 V T_{AD}=800 ns		10	30	mV
D5	Full-scale transition voltage			4970	4990		
D6	A/D conversion time		T_{AD}=800 ns	12.93			µs
D7	Sampling time		T_{AD}=800 ns	1.6			
D8	Reference voltage	V_{REF+}	Note)	4.0		V_{DD5}	V
D9	Analog input voltage			V_{SS}		V_{REF+}	
D10	Analog input leakage current		Channel OFF V_{ADIN}=V_{SS} to V_{DD5}			± 2	µA
D11	Reference voltage pin input leakage current		Ladder resistance OFF $V_{SS} \leq V_{REF+} \leq V_{DD5}$			± 5	
D12	Ladder resistance	R_{LADD}	V_{DD5}=5.0 V	15	40	80	kΩ

*11 T_{AD} is A/D conversion clock cycle.
The specification values of D2 to D5 are guaranteed on the condition of V_{DD5}=V_{REF+}=5 V, V_{SS}=0 V.

Even if A/D function is not used, the voltage of VREF+ pin must be set between V_{DD5} and 4.0 V.

1.5.5 Auto Reset Characteristics

E. Auto Reset Characteristics

$V_{DD5} = V_{RST}$ to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
E1	Operating supply voltage	V_{DD7}	Auto reset is used	V_{RST}		5.5	V
Power supply voltage							
E2	Power detection level	V_{RST1}	At rising	4.10	4.30	4.50	V
E3	Power detection level	V_{RST2}	At falling	4.00	4.20	4.40	
E4	Supply voltage change rate	$\Delta t/\Delta V$		2			ms/V

1.5.6 Internal High-speed Oscillation Circuit

F. Internal High-speed Oscillation Circuit

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
F1	Internal high-speed oscillation circuit frequency	f_{rc}	Ta = -40 °C to +85 °C		16		MHz
F2	Temperature dependence of oscillation frequency	f_{rc3}	Ta = 25 °C	-5.0		5.0	%
F3		f_{rc4}	Ta = -40 °C to +85 °C				

1.5.7 Flash EEPROM Program Conditions

G. Flash EEPROM Program Conditions

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
G1	Supply voltage	V_{DDEW}		4.0		5.5	V
G2	Programming/Erasing times of 32KB, 20KB Sector *2	E_{MAX1}		1000			Times
G3	Programming/Erasing times of 4KB Sector *2	E_{MAX2}		10000			Times
G4	Data retention period of 32KB, 20KB Sector *1	T_{HOLD1}	Ta= 85°C, P/E times ≤ 1000	20			Years
G5	Data retention period of 4KB Sector *1	T_{HOLD2}	Ta= 85°C, P/E times ≤ 1000 *2	20			Years
		T_{HOLD3}	Ta= 65°C, P/E times ≤ 10000 *2	20			Years

*1 Contain the period when power supply voltage is not supplied.

*2 Programming/Erasing times(P/E Times) is counted by the number of time a sector is erased.
It is controlled on sector basis.
For example, if writing 1 byte of data in any sector for hundred of times and then erasing the sector, a single rewriting is counted. Also, the number of times of rewriting in another sector, in which erasing is not performed, is not counted.
Overwriting data is disabled. To rewrite data, write the data after erasing sectors.

1.6 Package Dimension

■ Package code: TQFP080-P-1212FUnit: mm

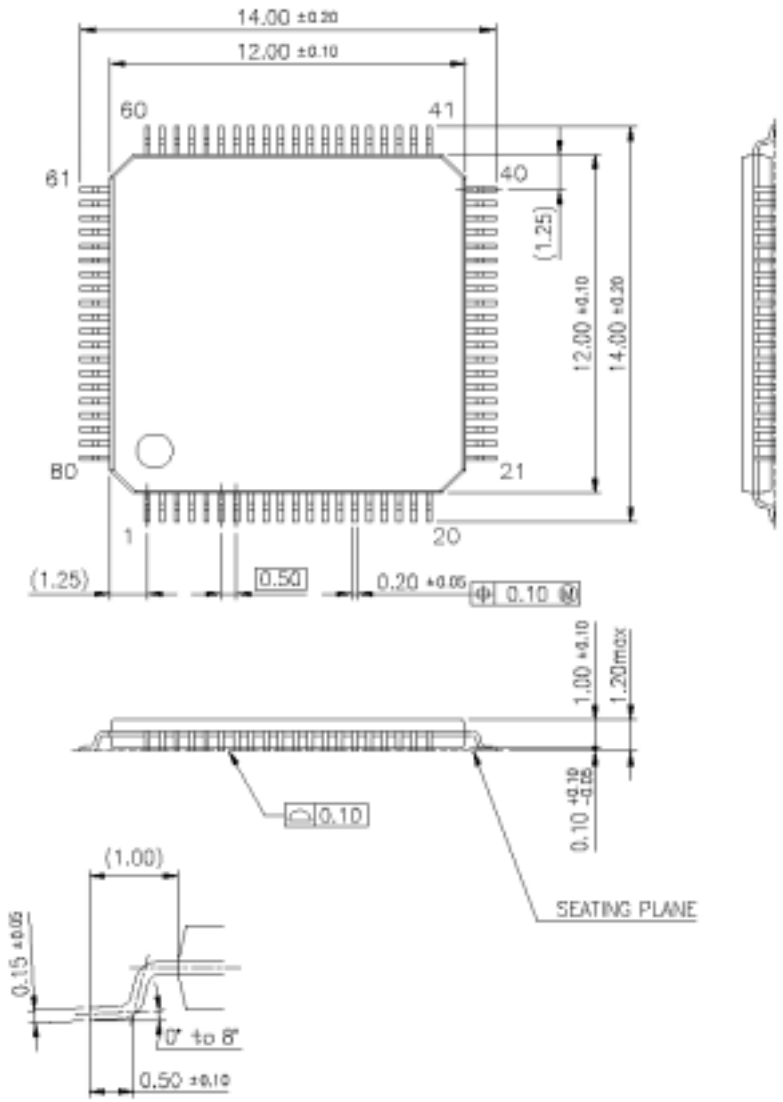

Figure:1.6.1 80-pin TQFP Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

■ Package code: LQFP080-P-1414EUnit: mm

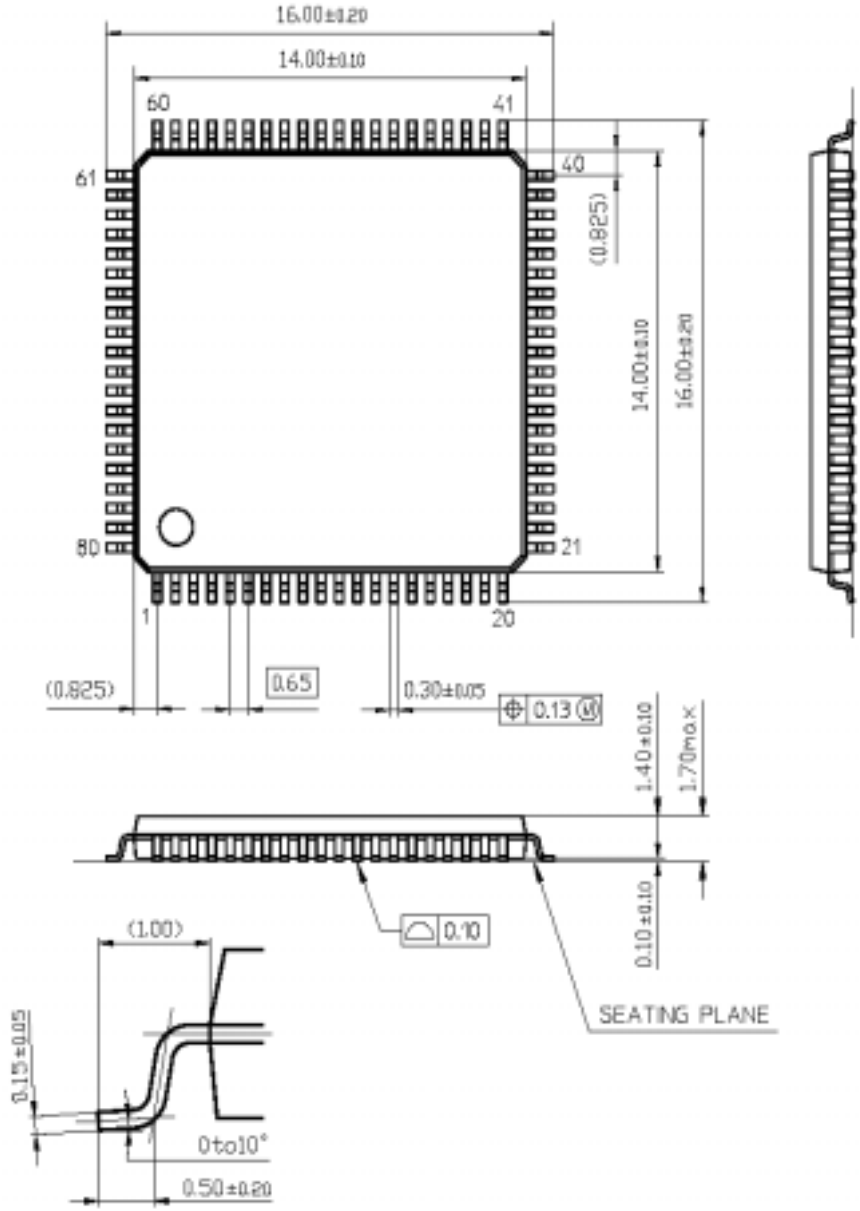

Figure:1.6.2 80-pin LQFP Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

■ Package code: TQFP064-P-1010DUnit: mm

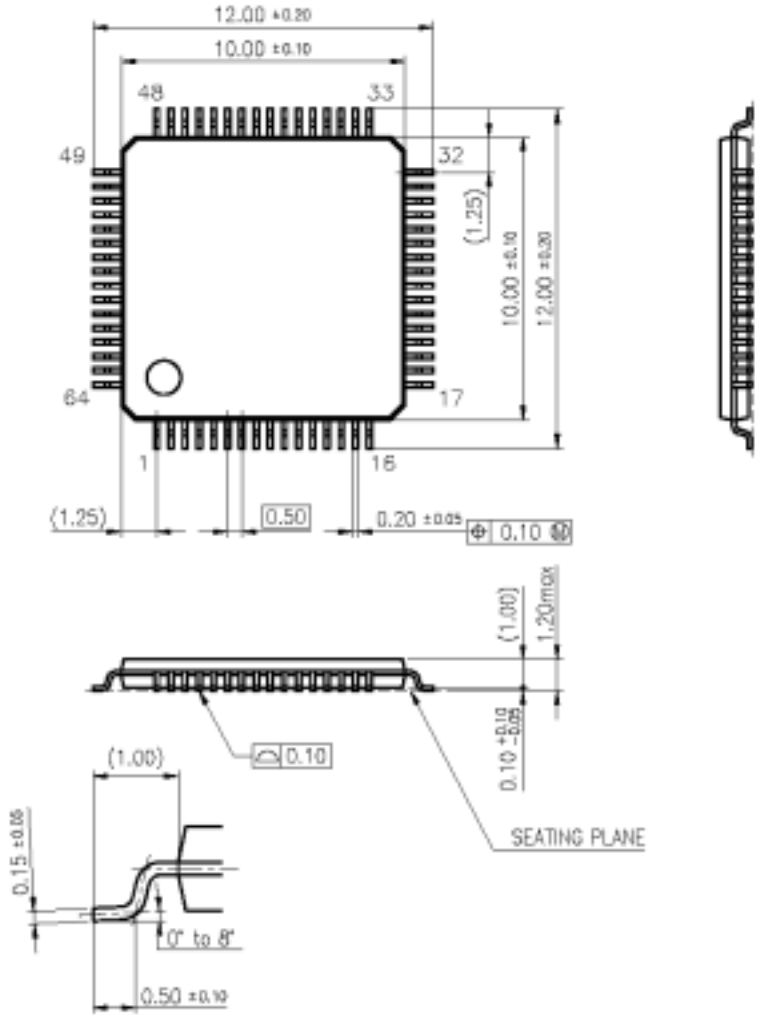

Figure:1.6.3 64-pin TQFP Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

■ Package code: LQFP064-P-1414Unit: mm

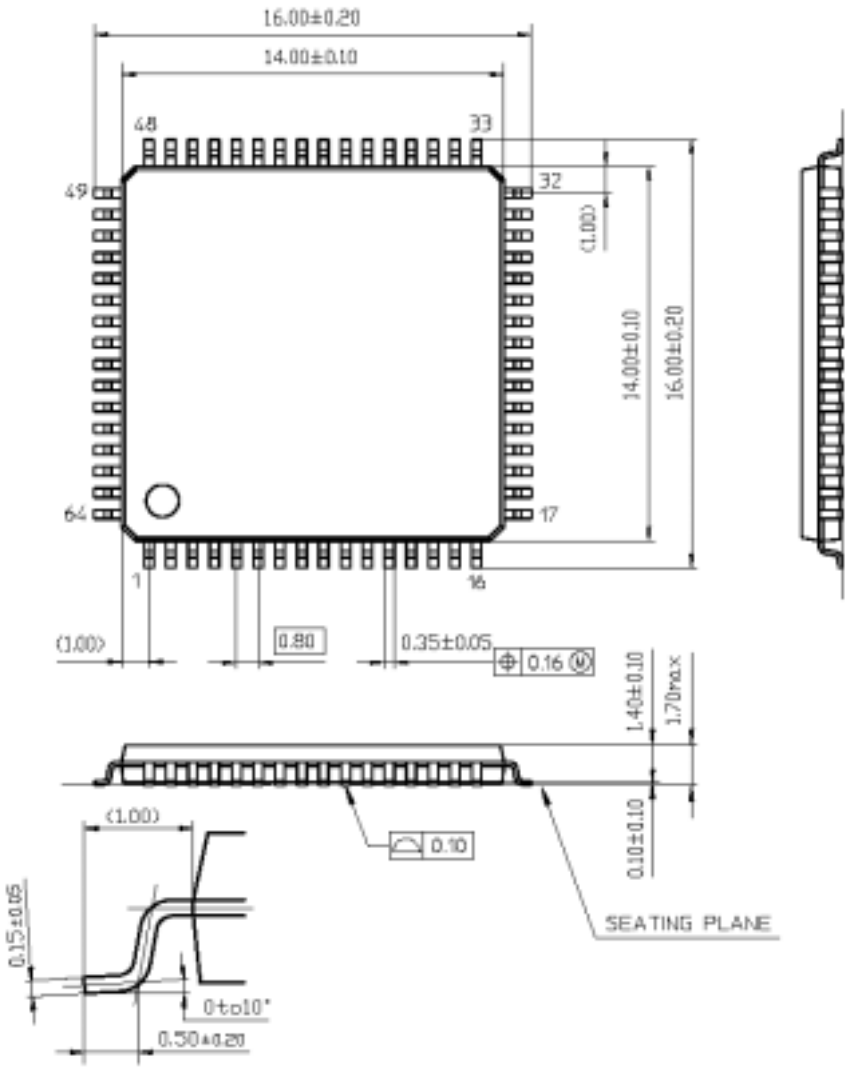

Figure:1.6.4 64-pin LQFP Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

■ Package code: TQFP056-P-1414Unit: mm

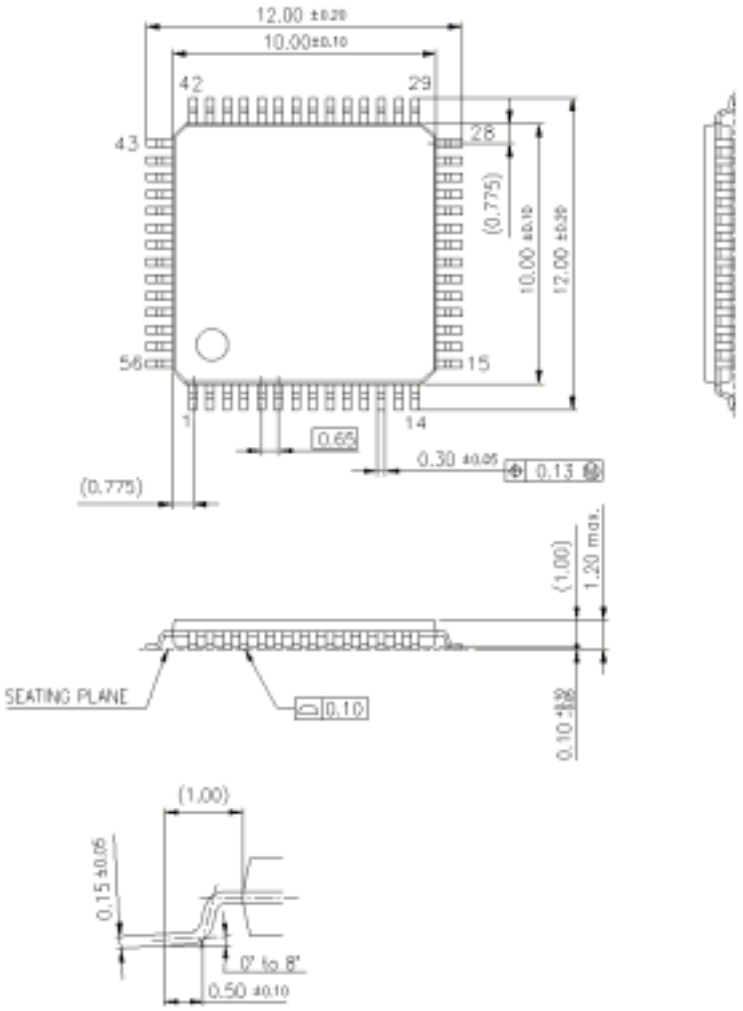

Figure:1.6.5 56-pin TQFP Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

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(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Please consult with our sales staff in advance for information on the following applications, moreover please exchange documents separately on terms of use etc.: Special applications (such as for in-vehicle equipment, airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, medical equipment and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
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(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. We do not guarantee quality for disassembled products or the product re-mounted after removing from the mounting board.
When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

(7) When reselling products described in this book to other companies without our permission and receiving any claim of request from the resale destination, please understand that customers will bear the burden.

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