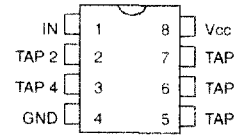
DALLAS SEMICONDUCTOR

DS1004
5-Tap High–Speed Silicon Delay Line

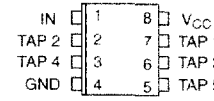
FEATURES

- All–silicon timing circuit
- Five equally delayed clock phases per input
- Precise tap–to–tap delay tolerances of ±0.5, ±0.75, or ±1 ns
- Input–to–tap 1 delay of 5 ns
- Delay tolerances of ±1.5 ns over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- CMOS design with TTL compatibility
- Standard 8–pin DIP and 150 mil 8–pin SOIC
- Vapor phase, IR and wave solderable
- Available in tape and reel

PIN ASSIGNMENT



DS1004M 8-PIN DIP
(300 MIL)
See Mech. Drawings
Section



DS1004Z 8-PIN SOIC
(150 MIL)
See Mech. Drawings
Section

PIN DESCRIPTION

TAP 1–5	–	Tap Output Number
V_{CC}	–	+5 Volt Supply
GND	–	Ground
IN	–	Input

DESCRIPTION

The DS1004 is a 5–tap all silicon delay line which can provide 2, 3, 4, or 5 ns tap–to–tap delays within a standard part family. The device is Dallas Semiconductor's fastest 5–tap delay line. It is available in a standard 8–pin DIP and 150 mil 8–pin mini–SOIC. The device features precise leading and trailing edge accuracies and has the inherent reliability of an all–silicon delay line solution.

The DS1004 is specified for tap–to–tap tolerances as shown in Table 1. Each device has a minimum input–to–tap 1 delay of 5 ns. Subsequent taps (taps 2 through 5) are precisely delayed by 2, 3, 4, or 5 ns. See Table 1 for details. Tolerance over temperature and voltage is ±1.5 ns. Nominal tap–to–tap tolerances range from ±0.5 ns to ±1.0 ns. Each output is capable of driving up to 10 LS loads.

For customers needing non–standard delay values, the Late Package Program (LPP) is available. Customers may contact Dallas Semiconductor at (972) 371–4348 for further details.