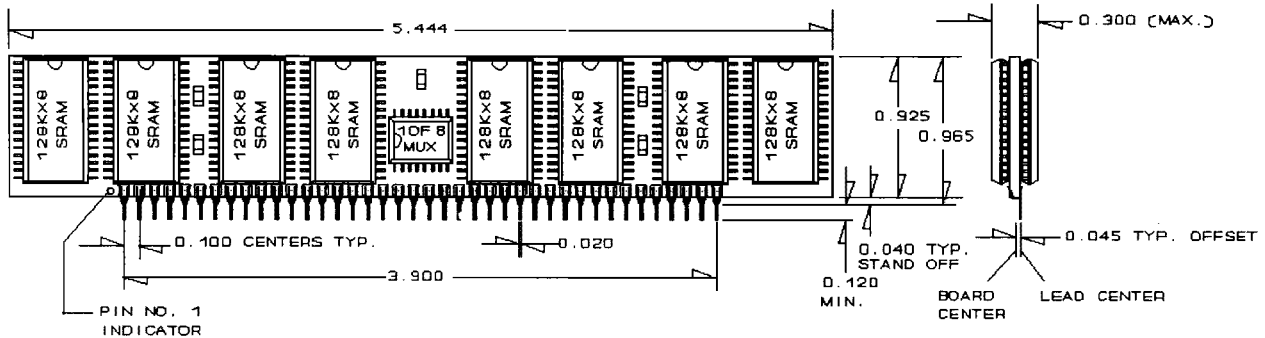


**2 MEGWORD BY 8 BIT  
 HIGH SPEED SRAM MODULE  
 WITH ON BOARD DECODERS**

**SPECIFICATION DRAWING**



FRONT AND SIDE VIEWS  
 (SHOWING VERTICAL MOUNTING LEADS OPTION)



BOTTOM, REAR, AND SIDE VIEWS  
 (SHOWING HORIZONTAL MOUNTING LEADS OPTION)

AEP  
 2MEGx8 SRAM  
 DIMENSIONS IN INCHES  
 TOLERANCE: +/- 0.010  
 UNLESS SPECIFIED

PRELIMINARY



**2M x 8 STATIC RAM MODULE**

**SIP PIN-OUT CONFIGURATION**

1	—	ANC		
2	—	A <sub>19</sub>		
3	—	NC		
4	—	VDD	A0 - A20	ADDRESS INPUTS
5	—	WE*		
6	—	I/O <sub>3</sub>	I/O1 - I/O8	DATA LINES
7	—	I/O <sub>4</sub>		
8	—	I/O <sub>1</sub>	WE*	WRITE ENABLE
9	—	A <sub>1</sub>		
10	—	A <sub>2</sub>	SIPE*	SIP ENABLE
11	—	A <sub>3</sub>		
12	—	A <sub>4</sub>	OE*	OUTPUT ENABLE
13	—	VSS		
14	—	I/O <sub>6</sub>	VDD	POWER +5V
15	—	A <sub>10</sub>		
16	—	A <sub>11</sub>	VSS	GROUND
17	—	A <sub>5</sub>		
18	—	A <sub>13</sub>	NC	NO CONNECT
19	—	A <sub>14</sub>		
20	—	NC	ANC	NO CONNECT (reserved for next generation address lines)
21	—	SIPE*		
22	—	A <sub>15</sub>		
23	—	A <sub>16</sub>		
24	—	A <sub>12</sub>		
25	—	A <sub>18</sub>		
26	—	A <sub>6</sub>		
27	—	I/O <sub>2</sub>		
28	—	VSS		
29	—	A <sub>0</sub>		
30	—	A <sub>7</sub>		
31	—	A <sub>8</sub>		
32	—	A <sub>9</sub>		
33	—	I/O <sub>8</sub>		
34	—	I/O <sub>5</sub>		
35	—	I/O <sub>7</sub>		
36	—	A <sub>17</sub>		
37	—	VDD		
38	—	OE*		
39	—	A <sub>20</sub>		
40	—	ANC		

\* ACTIVE WHEN LOW

