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**iATC™ 29C51/29C52  
FEATURE CONTROL COMBO  
LINE CARD CONTROLLER  
ARCHITECTURAL OVERVIEW**

Intel is developing a family of advanced telephony line-interface circuit components which give OEM's an evolutionary growth path toward an all-digital network. These new VSLI devices fit into system architectures which are flexible enough to support both analog and digital subscriber lines.

These components are based on the following design philosophy:

- Integrate as much of the low-voltage, per-line functions of the analog line circuit as is cost effective.
- Support an all-serial backplane bus architecture for digital TDM highways, signaling and control buses, and line-card addressing.
- Add a wide variety of per-line features to the normal BORSCHT functions for the analog line circuit.
- Make analog and digital subscriber line circuit cards plug-compatible in a line equipment shelf.
- Allow all system transmission, signaling, and control buses to serve analog and/or digital subscriber lines, or analog trunks, interchangeably.
- Provide a graceful upgrade path from today's analog telephone service to future digital voice/data services by allowing a common system hardware design using distributed control.
- Retain compatibility with international transmission, signaling and control standards as they evolve.

The first two members of the family, the 29C51 Feature Control Combo and the 29C52 Line Card Controller are described in this document. Future members of the family will provide digital subscriber capability for both private and public network switching systems in a manner compatible with CCITT standards for the ISDN.

The analog line card partitioning shown in Figure 1 illustrates the generalized interfaces of both components. The 29C51, plus the SLIC functions, provide the familiar BORSCHT functions. When the 29C52 functions are added, the analog line interface circuit functions are complete. The digital line interface has a similar architecture.

The combined use of the 29C51 and 29C52 for analog line cards provides all of the PCM encoding, decoding, filtering, multiplexing, line card addressing and feature control functions associated with the analog line circuit. The 29C52 handles all digital data transfers between the line-group TMD highways and the 29C51's. Each 29C52 line card controller can be slaved or supported by a local microprocessor.

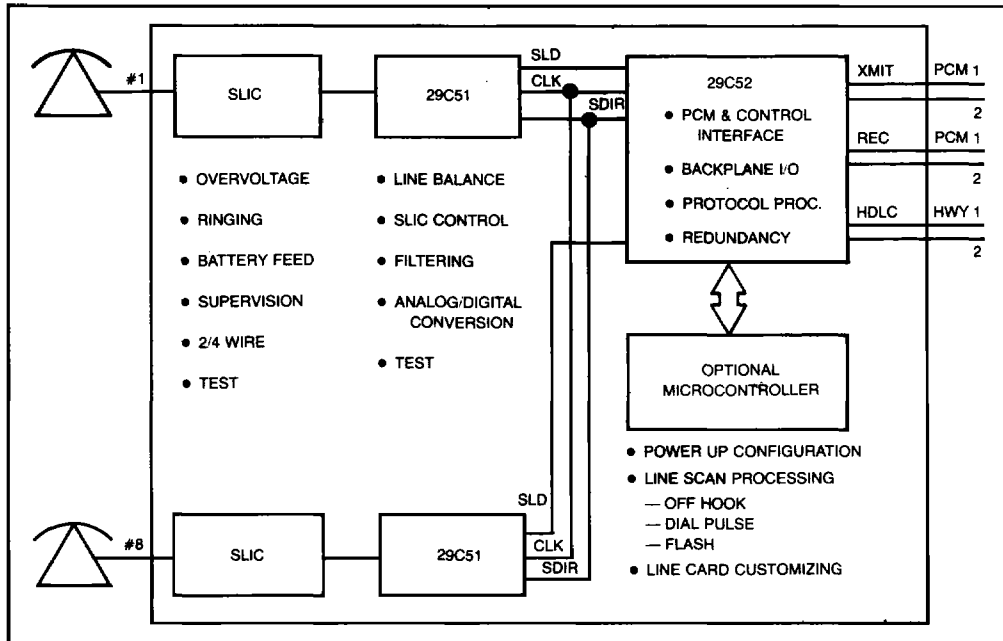


Figure 1. Analog Line Card

### IATC™ 29C51 FEATURE CONTROL COMBO

- Programmable Transmit and Receive Gain
- Programmable Hybrid Balance Network Select
- Programmable Analog and Digital Loopback
- Programmable  $\mu$ /A-Law Select
- Flexible Signaling Interface
- Secondary Analog Channel
- Three-Party Conferencing

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The Intel IATC 29C51 Feature Control Combo is an advanced user-programmable, fully integrated PCM Codec with transmit/receive filters fabricated in a CHMOS technology. This technology is built on HMOS-E and will allow the 29C51 to achieve excellent transmission performance as in the 2913/2914 combo while achieving the low power consumption typical of CMOS circuits.

The 29C51 is intended for use with the 29C52 Line Card Controller in switching environments in which the transmit and receive channels are synchronous in frequency. The 29C52 handles the transfer of voice, user data, signaling, and feature control information between the backplane and up to 8 29C51's.

The 29C51, like its 2914 predecessor, includes the codec, transmit/receive filters, external gain adjust, programmable  $\mu$ /A-law commanding, and programmable power-down mode. Additional user programmable features have been added. These include: three internal and two external hybrid balance networks; programmable transmit and receive gain — for use in meeting the network loss plan; three loopback modes — for use in system and component testing; secondary analog transmit and receive channels — for SLIC control; and three-party conferencing.

The 29C51 is shown in a simplified block diagram in Figure 2. The subscriber interface provides for signaling, voice I/O, and optional secondary analog I/O. The 29C52 interface provides clock, frame sync, and bidirectional serial data transfer. Programmable feature selections and values are preserved in the control registers, even while the 29C51 is in power-down mode, and requires reloading only during a power-on excursion. All internal switch settings are programmable, allowing the user to customize the internal features according to system needs.

The 29C51 will be packaged in 22 and 28 pin DIP and 28 lead LCC.

### IATC™ 29C52 LINE CARD CONTROLLER

- Provides Interface for up to 8 Subscribers
- Performs all Timeslot Assignments
- 2 Full-Duplex, Serial TDM Highways
- 2 Serial, Bidirectional Packetized Highways for Signaling Control
- Implements HDLC Protocol to Guarantee Integrity of all Signaling and Control Information
- 8-Bit Addressing Allows up to 255 Controllers Plus a "Broadcast" Address Per Control Path
- Operates at 1.536, 1.544, 2.048, 3.072, 3.088, or 4.096 MHz

The Intel iATC 29C52 Line Card Controller (LCC) is a special purpose I/O controller optimized for use in digital voice/data switching systems. It is fabricated in Intel's highly-reliable, +5V CHMOS technology, which realizes the high speed and high densities obtained in HMOS-II, while achieving the low power consumption typical of CMOS circuits. The 29C52 is intended for use with up to eight 29C51 Feature Control Combos. It is also useful as a general purpose I/O controller for other applications.

The 29C52 concentrates and multiplexes all digital information which passes between a line-card and the next higher switching or control level in the system hierarchy. The data paths supported are shown in Figure 3. The first path (1) is between the TDM highways and the 29C51. The LCC performs the first stage space and time switching function for the PCM information. It also controls the transfer of feature control and signaling information for the 29C51 (or other subscriber circuit) from the signaling/control highways (2) or from optional local microcontroller (3).

The 29C52 LCC performs all protocol control functions, using the HDLC protocol format, for all information which passes between the line card and the next higher control level. These HDLC packetized signaling/control messages can be transferred via the signaling/control highways (4) or be disassembled and interleaved on the TDM highways (5). The messages can be executed by the 29C52 using its instruction set, or passed to the local microcontroller for interpretation and execution by configuring the appropriate 29C52 registers.

The 29C52 will be packaged in 40 pin DIP and 44 lead LCC.

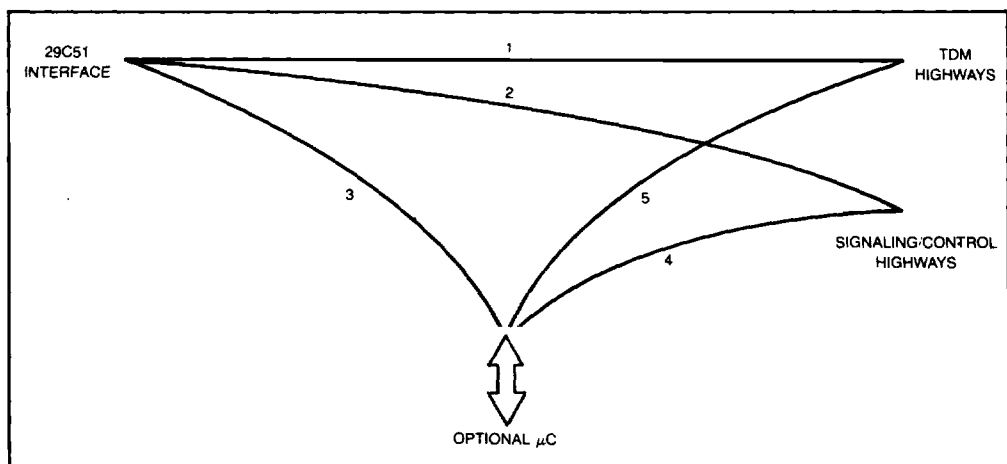


Figure 3. 29C52 Data Path Map

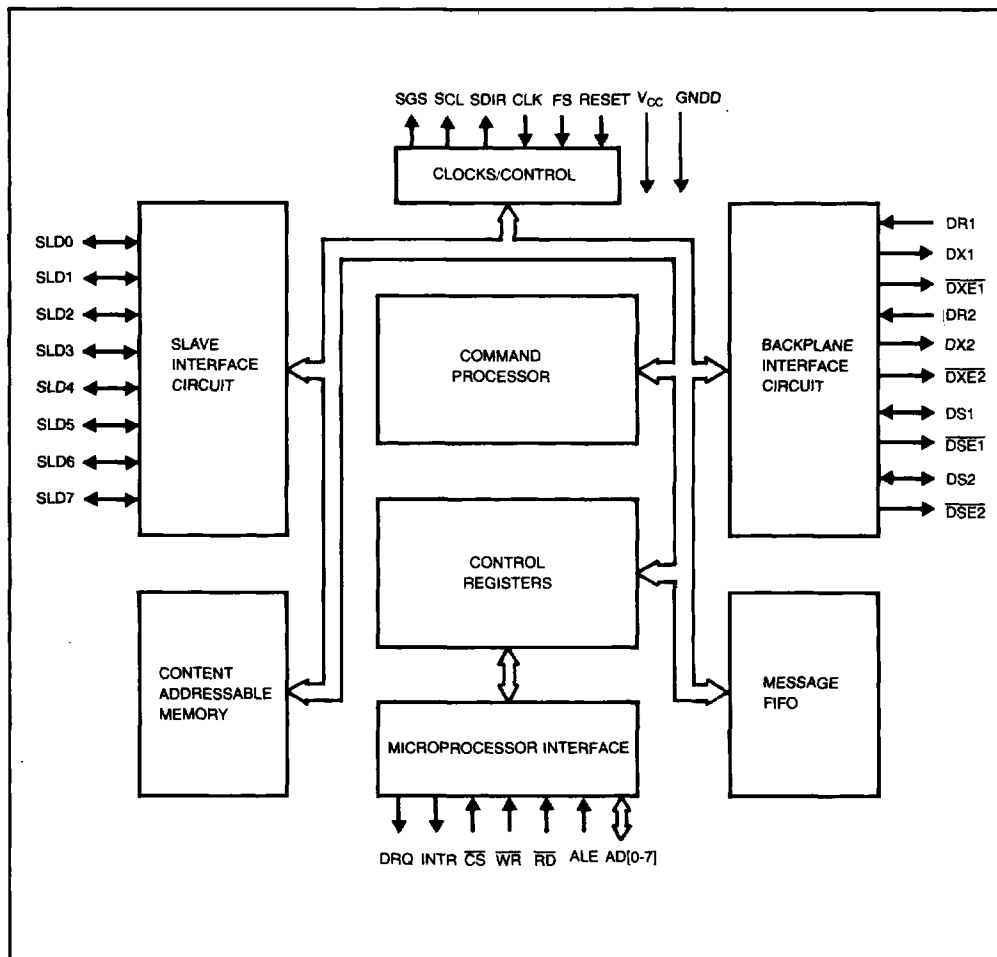


Figure 4. Block Diagram

SLD0,SLD1,....,SLD7	Slave Data Leads	V <sub>CC</sub>	Power (+5V)
SCL	Slave Clock	GNDD	Digital Ground
SDIR	Slave Direction	CLK	Master Clock
SGS	Signaling Strobe	FS	Frame Sync Input
AD(0-7)	Address/Data Bus	Reset	
ALE	Address Latch Enable	DR1,DR2	Receive TDM Highway
WR	Write	DX1,DX2	Transmit TDM Highway
RD	Read	DXE1,DXE2	External Buffer Enable
CS	Chip Select	DS1,DS2	Signaling/Control Highway
INTR	Interrupt	DSE1,DSE2	External Buffer Enable
DRQ	Data Request		

PIN NAMES