HARRIS SEMICONDUCTOR

HS-3374RH

Radiation Hardened 8-Bit Bidirectional CMOS/TTL Level Converter

December 1992

Features

- Radiation Hardened EPI-CMOS
  - Total Dose 1 x 10^5 RAD(Si)
  - Latch-Up Immune > 1 x 10^{12} RAD(Si)/s*
- Low Propagation Delay Time
  - Typical CMOS to TTL Pre-Rad 40ns
  - Typical CMOS to TTL Post 100K RADs 40ns
  - Typical TTL to CMOS Pre-Rad 50ns
  - Typical TTL to CMOS Post 100K RADs 50ns
- Low Standby Power
- +10V CMOS and +5V TTL Power Supply Inputs
- Eight Non-Inverting Three-State Input/Output Channels
- No External TTL Input Pull-Up Resistors Required
- High TTL Sink Current
- Equivalent to Sandia SA2996
- Military Temperature Range -55°C to +125°C

Description

The Harris HS-3374RH is a radiation hardened 8-bit bidirectional level converter designed to interface CMOS logic levels with TTL logic levels in radiation hardened bus oriented systems. The HS-3374RH is fabricated using a radiation hardened EPI-CMOS process and features eight parallel bidirectional buffer/level converters.

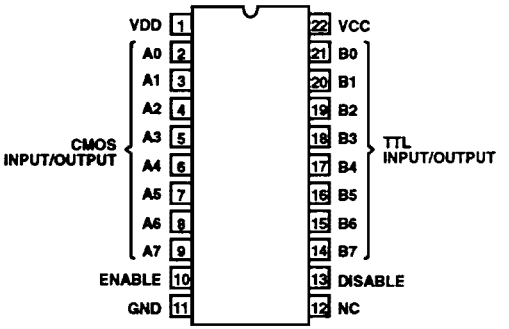
Two control inputs, ENABLE and DISABLE, are used to determine the direction of data flow, and to set both the in puts and outputs in the high impedance state. The control inputs may be driven by either TTL or CMOS logic drivers capable of sinking one standard TTL load.

The HS-3374RH is a non-inverting version of the industry standard CD40116. The non-inverting outputs of the HS-3374RH reduce PC board chip count by eliminating the need to restore data back to a non-inverted format.

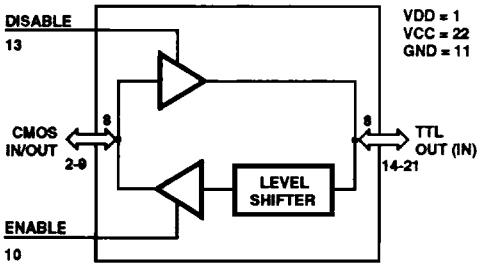
* For operation at 10V and transient levels above 1 x 10^{10} Rad(Si)/s, please refer to Application Note 401.

Pinout

INTERNAL PACKAGE CODE HSX
CASE OUTLINE D7, CONFIGURATION 3
TOP VIEW



Functional Diagram



11 µPROCESSOR PERIPHERALS

File Number 3038

Absolute Maximum Ratings

Supply Voltage ..... +11.0V
I/O Voltage Applied ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic Dip Package	74.8°C/W	123°C/W

Maximum Package Power Dissipation at +125°C
Ceramic Dip Package ..... .67W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range VDD ..... +9.5V to +10.5V
VCC ..... +4.75V to +5.25V
Operating Temperature Range ..... -55°C to +125°C
Input Voltage Range
Data Inputs (CMOS) ..... GND-0.3 to VDD+0.3
Data Inputs (TTL) ..... GND-0.3 to VCC+0.3
Enable, Disable Inputs ..... GND-0.3 to VDD+0.3

Input Low Voltage (CMOS) ..... GND to 1V
Input High Voltage (CMOS) ..... VDD-1.0V to VDD
Input Low Voltage (TTL) 0.8V
Input High Voltage (TTL) 2.8V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
ENABLE AND DISABLE IINPUTS							
Input Leakage Current	IIH CMOS	VDD = 10.5V, VCC = 5.25V, VIN = 10.5V, Floating Outputs	1, 2, 3	-55°C, +25°C, +125°C	-	1	µA
TTL INPUT TO CMOS OUTPUTS							
Input Leakage Current	IIL IIH	VDD = 10.5V, VCC = 5.25V, VIN = 0.8V, Other Inputs at 2.8V	1, 2, 3	-55°C, +25°C, +125°C	-1	-	µA
		VDD = 10.5V, VCC = 5.25V, VIN = 2.8V, other Inputs = 0.8V	1, 2, 3	-55°C, +25°C, +125°C	-	1	µA
High Level Output Voltage	VOH	VDD = 9.5V, VCC = 4.75V, VIH = 2.8V, VIL = 0.8V, IOH = -2.0mA	1, 2, 3	-55°C, +25°C, +125°C	3	-	V
Low level output Voltage	VOL	VDD = 10.5V, VCC = 5.25V, VIH = 2.8V, VIL 0.8V, IOL = 2.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
CMOS to TTL OUTPUTS							
High Level Output Voltage	VOH	VDD = 9.5, VCC = 4.75V, VIH = 8.5V, VIL = 1.0V, IOH = -2.0mA	1, 2, 3	-55°C, +25°C, +125°C	9	-	V
Low Level Output Voltage	VOL	VDD = 10.5V, VCC = 5.25V, VIH = 4.5V, VIL = 1.0V, IOL = 11mA	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	V
Output Leakage Current	IOZL	VDD = 10.5V, VCC = 5.25V, VIN = 0V, All other pins high	1, 2, 3	-55°C, +25°C, +125°C	-10	-	µA
	IOZH	VDD = 10.5V, VCC = 5.25V, VIN = 2.8V, All other pins at GND	1, 2, 3	-55°C, +25°C, +125°C	-	10	µA
Functional Tests	FT	CMOS: 1.) VDD = 10.5V, VCC = 5.25V 2.) VDD = 9.5V, VCC = 4.75V, VIH = VDD-1V, VIL = 1V TTL: 1.) VDD = 10.5V, VCC = 5.25V 2.) VDD = 9.5V, VCC = 4.75V, VIH = 2.8V, VIL = 0.8V	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Static Current 1	SIDD1	VDD = 10.5V, VCC = 5.25V, EN = 2.8V, DISABLE = 2.8V, Floating Outputs	1, 2, 3	-55°C, +25°C, +125°C	-	300	µA
Static Current 2	SIDD2	VDD = 10.5V, VCC = 5.25V, EN = 0V, DISABLE = 2.8V, Floating Outputs	1, 2, 3	-55°C, +25°C, +125°C	-	100	µA
Static Current	SICC	VDD = 10.5, VCC = 5.25V, EN = 0V, DISABLE = 2.8V, Floating Output, Measure VCC pin	1, 2, 3	-55°C, +25°C, +125°C	-	5	µA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Times CMOS/TTL Data In to Data Out	TPHLCT	9, 10, 11	-55°C, +25°C, +125°C	-	40	ns
Propagation Delay Times CMOS Data In to Data Out	TPLHCT	9, 10, 11	-55°C, +25°C, +125°C	-	50	ns
Propagation Delay Times CMOS/TTL Data In to Data Out	TPHLTC	9, 10, 11	-55°C, +25°C, +125°C	-	85	ns
Propagation Delay Time TTL/CMOS Data In to Data Out	TPLHTC	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
Transition Time CMOS/TTL Input/Output	TTHLCT	9, 10, 11	-55°C, +25°C, +125°C	-	20	ns
Transition Time CMOS/TTL Input/Output	TTLHCT	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
Transition Time CMOS/TTL Input/Output	TTHLTC	9, 10, 11	-55°C, +25°C, +125°C	-	50	ns
Transition Time CMOS/TTL Input/Output	TTLHTC	9, 10, 11	-55°C, +25°C, +125°C	-	50	ns
Propagation Delay Time TTL/CMOS Enable to CMOS Out	TPHZTC	9, 10, 11	-55°C, +25°C, +125°C	-	90	ns
Propagation Delay Time TTL/CMOS Enable to CMOS Out	TPZHTC	9, 10, 11	-55°C, +25°C, +125°C	-	90	ns
Propagation Delay Time TTL/CMOS Enable to CMOS Out	TPLZTC	9, 10, 11	-55°C, +25°C, +125°C	-	85	ns
Propagation Delay Time TTL/CMOS Enable to CMOS Out	TPZLTC	9, 10, 11	-55°C, +25°C, +125°C	-	85	ns
Propagation Delay Time CMOS/TTL Disable to TTL Out	TPHZCT	9, 10, 11	-55°C, +25°C, +125°C	-	70	ns
Propagation Delay Time CMOS/TTL Disable to TTL Out	TPZHCT	9, 10, 11	-55°C, +25°C, +125°C	-	130	ns
Propagation Delay Time CMOS/TTL Disable to TTL Out	TPLZCT	9, 10, 11	-55°C, +25°C, +125°C	-	120	ns
Propagation Delay Time CMOS/TTL Disable to TTL Out	TPZLCT	9, 10, 11	-55°C, +25°C, +125°C	-	125	ns

NOTE: Timings are measured with the following conditions: CL = 100pF, VDD = 9.5V, VCC = 4.75V, VIH = 8.5V (2.8V), VIL = 1.0V (0.8V).

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input, Output Capacitance	CMOS CI/O	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	+25°C	-	13	pF
Input Capacitance	CIN	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	+25°C	-	15	pF
Input, Output Capcitance	TTL CI/O	VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground	+25°C	-	17	pF

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The Post Irradiation test conditions and limits are the same as those listed in Table 1 and Table 2.

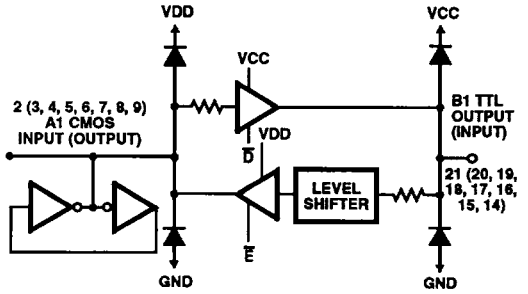
TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current 1	SIDD1	±50µA
Static Current 2	SIDD2	±30µA
Low Input Leakage Current	IIL	±100nA
High Input Leakage Current	IIH	±100nA
Low Output Leakage Current	IOZL	±1µA
High Output Leakage Current	IOZH	±1µA

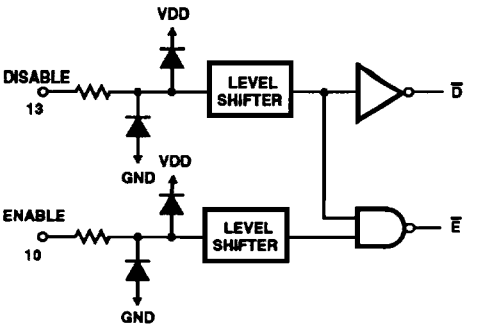
TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test	100%/5004	1, 7, 9
PDA	100%/5004	1, 7
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D Others	Samples/5004	1, 7
Group E Subgroup 2	Samples/5004	1, 7, 9

Functional Block Diagram



1 OF 8 IDENTICAL CIRCUITS



NOTES:

1. Enable and disable are TTL type inputs
2. D and E outputs are common to all 8 channels

INPUT (OUTPUT)		OUTPUT (INPUT)	
DATA	TERMINAL NUMBER	DATA	TERMINAL NUMBER
A0	2	B0	21
A1	3	B1	20
A2	4	B2	19
A3	5	B3	18
A4	6	B4	17
A5	7	B5	16
A6	8	B6	15
A7	9	B7	14

TRUTH TABLE

ENABLE	DISABLE	FUNCTION
X	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z)

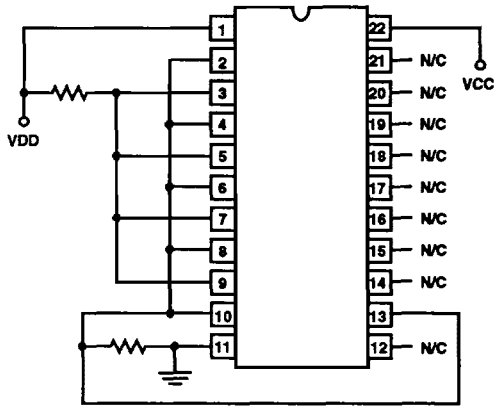
0 = Low Level 1 = High Level X = Don't Care
Z = High Impedance on Both CMOS and TTL sides.

NOTE: An important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule applies to inputs connected to a three-state bus. The need for external pull-up resistors during three-state bus conditions is eliminated by the presence of regenerative latches on the following HS-3374RH pins: A0 - 7.

The functional block diagram depicts one of these pins with the regenerative latch. When the CMOS driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the three-state condition. A transient drive current of ±1.5mA at VDD/2 ±0.5V for 10ns is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during three-state conditions.

* WARNING: Do not activate the Disable input by hardwiring to any TTL input pins. This is an incorrect mode of operation.

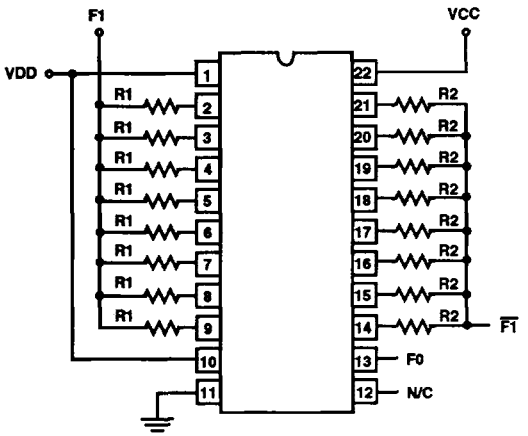
Burn-In Circuits



STATIC CONFIGURATIONS

NOTES:

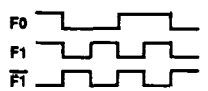
Minimum Temperature +125°C
VCC = 5.0V ±10%
VDD = 10.0V ± 10%
All Resistors R1 = 10K 1/4 watt
Static Sensitive: All Voltages Must be Ramped
ICC = 100µA
IDD = 1mA



DYNAMIC CONFIGURATION

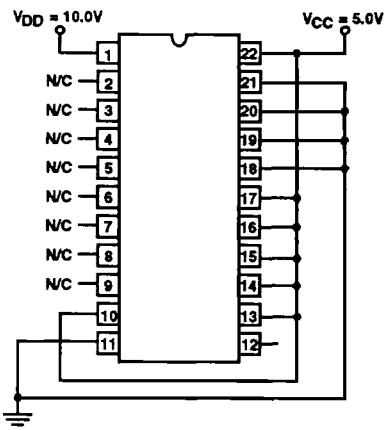
NOTES:

VDD = 10.0 ± 5%
VCC = 5V ± 10%
R1 = 10K, R2 = 2.5K



F0 + F1 are 10V Peak to Peak
F1 = 100KHz 50% Duty cycle
F0 = F1 = 50KHz 50% Duty Cycle
F1 is 5V Peak to Peak

Irradiation Circuit



Radiation Screening Procedure

1. A random sample of two dice per wafer is drawn from the wafer lot. Wafer identity is retained.
2. The sample die shall be assembled and tested for functionality, in a ceramic dip.
3. The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Ras(Si) +10% from a Gammacell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = +5V. The dose rate shall be between 50 rads/sec and 300 rads/sec.
4. The Irradiation Bias circuit is shown to the left.
5. The sample devices shall be started into test within 1 hour of irradiation and have completed test within 2 hours of irradiation. The wafers are accepted only if the sample, exclusive of non-radiation failures, meets all electrical specifications at room temperature.
6. Radiation screening to a higher total dose is available. Customers should contact their closest Harris Representative for details.

Radiation Effects

The HS-3374RH has been designed to survive in a radiation environment and to meet the electrical characteristics. Latching up free operation is achieved by the use of epitaxial starting material. Improved total dose hardness is obtained when special low temperature processing cycles. On a production basis, Harris performs screens for total dose hardness to a level of 1 x 10^5 Rad(Si). Transient radiation tests have shown the following results:

- Latch-up free to doses ≥ 1 x 10^{12} rads/sec*

* For operation at 10 volts and transient levels above 1 x 10^{10} Rad(Si)/s please refer to Application Note 401.

Harris - Space Level Product Flow (Note 1)

SEM - Traceable to Diffusion - Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection - Method 2010, Condition A

Gamma Radiation Assurance Tests - Method 1019

Nondestructive Bond Pull - Method 2023

Customer Pre-Cap Visual Inspection (Notes 2)

Temperature Cycling - Method 1010, Condition C

Constant Acceleration - Method 2001, Condition E Min., Y1

Particle Impact Noise Detection - Method 2020, Condition A

Electrical Tests - Harris' Option

Serialization

X-Ray Inspection - Method 2012

Electrical Tests - Subgroup 1; Read and Record (T0)

Static Burn-In - Method 1015, Condition B; 72 Hours, +125°C Minimum

Electrical Tests - Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0-T1)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Dynamic Burn-In, Method 1015, Condition D, 240 Hours, +125°C (Note 3)

Electrical Tests - Subgroup 1; Read and Record (T2)

Alternate Group A - Subgroups 1, 7, 9; Method 5005; Paragraph 3.5.1.1

Burn-In Delta Calculation (T0-T2)

PDA Calculation 3%: Subgroup 7
5% Subgroups 1, 7, Delta

Electrical Tests - Subgroup 3; Read and Record

Alternate Group A - Subgroup 3, 8B, 11; Method 5005; Paragraph 3.5.1.1

Marking

Electrical Tests - Subgroups 2; Read and Record

Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Paragraph 3.5.1.1

Fine and Gross Leak Tests - Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection - Method 5005 (Notes 2)
End-Point Electrical Parameters: B5; Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11

Group D Inspection - Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: B5; Subgroups 1, 7, 9

External Visual Inspection - Method 2009

Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table I shall apply; unless otherwise specified.
2. These steps are optional, and should be listed on the purchase order if required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table O of Method 1015.
4. For Group D, subgroup 3 inspection of package configurations which utilize a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains: Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (includes SEM report)
   X-Ray Report and Film
   Test Variables Data

Metallization Topology

DIE DIMENSIONS:
89.4 x 76.0 x 14 ± 1mils

METALLIZATION:
Type: AlSi
Thickness: 8kÅ ± 1kÅ

GLASSIVATION:
Type: SiO2
Thickness: 11kÅ ± 2kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP- 460°C (Max)

Metallization Mask Layout

HS-3374RH