ALVCH16245

16 Bit Bus Transceiver with 3-State Outputs

Preliminary

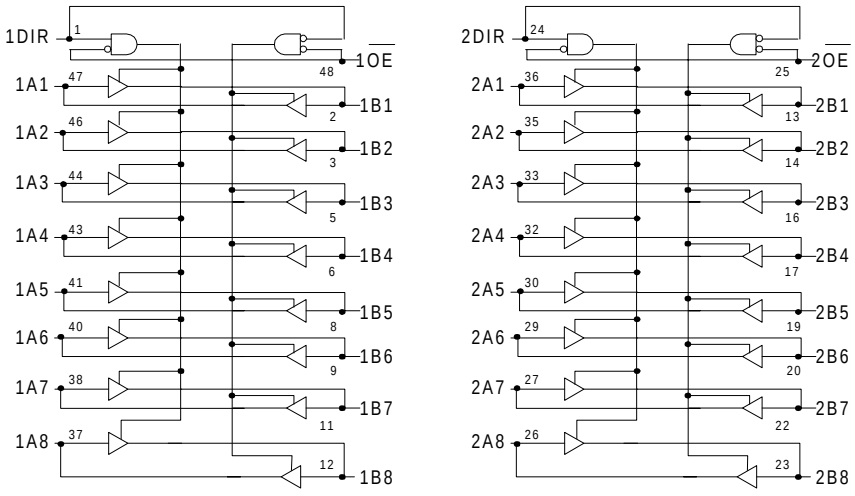
Product Features

- 16 bit transceiver with nibble output enable control
- Output buffers have controlled edge rates.
- Bus Hold on data inputs eliminates need for external pullup/pulldown resistors
- 1.65V to 3.6V voltage range
- 2 KV ESD protection
- Latch-up performance exceeds 250 mA per JESD17
- Extended temperature range of -40°C to + 85°C
- 48 pin SSOP, TSSOP, and TVSOP package availability.

Product Description

The ALVCH16245 is designed specifically for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

Block Diagram



Product Description (Cont.)

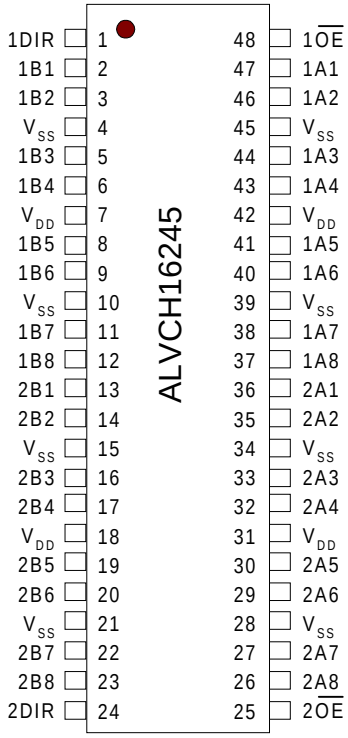
The device can be used as two 8-bit transceivers, or one 16-bit transceiver. It allows data transmission for the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The outputs, which are designed to sink up to 24 mA, include controlled edge rates to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{DD} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driving device.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Pin Description



Preliminary

Pin Description

Pin Number	Pin Name	Description
25, 48	$n\overline{OE}$	Output enable input (active LOW)
4, 10, 15, 21, 28, 34, 39, 45	V_{SS}	Ground (0V)
7, 18, 31,42	V_{DD}	Positive supply voltage
2, 3, 5, 6, 8, 9, 11, 12 , 13, 14, 16, 17, 19, 20, 22, 23	1B1 to 1B8 2B1 to 2B8	Data inputs (or 3-state Outputs)
47, 46, 44, 43, 41, 40, 38, 37 36, 35, 33, 32, 30, 29, 27, 26	1A1 to 1A8 2A1 to 2A8	Data inputs (or 3-state Outputs
1, 48	1DIR, 2DIR	Direction Control Inputs

Function Table (each 8-bit section)(1)

Inputs		Outputs
$n\overline{OE}$	**nDIR**	
L	L	B data to A bus
L	H	A data to B bus
H	X	High Z state

Note:
H = HIGH voltage level
L = LOW voltage level
X = Don't Care

Capacitance Table

Symbol	Parameter(1)	Cond.	Typ	Max	Unit
Cin	Input Cap.	Vin = 0V	5	7	pF
Cout	Output Cap.	Vout = 0V	7	9	pF
CI/O	I/O Port Cap.	Vin = 0V	7	9	pF

Note1: As applicable to device type.

Absolute Maximum Rating(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with respect to V_{SS}	-0.5 to + 4.6	V
V_{TERM}(3)	Terminal Voltage with respect to V_{SS}	- 0.5 to V_{DD} + 0.5	V
T_{STG}	Storage Temperature	- 65° to + 150° C	°C
I_{OUT}	DC Output Current	- 50 to + 50	mA
I_{IK}	Continous Clamp Current, VI<0 or VI>V_{SS}	± 50	mA
I_{OK}	Continuous Clamp Current, Vo<0	-50	mA
I_{dd} I_{SS}	Continuous Current through each V_{DD} or V_{SS}	±100	mA

Notes:

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. V_{DD} terminals.
3. All terminals except V_{DD}.

DC Parameters (T_{amb} = - 40° to + 85° C)

Symbol	Parameter	Test Conditions		Min	Typ(1)	Max.	Unit
V_{IH}	HIGH level input voltage	V_{DD} = 1.65V to 1.95V		0.65 x V_{DD}	-	-	V
		V_{DD} = 2.3V to 2.7V		1.7	-	-	V
		V_{DD} = 2.7V to 3.6V		2.0	-	-	V
V_{IL}	LOW level input voltage	V_{DD} = 1.65V to 1.95V		-	-	0.35 x V_{DD}	V
		V_{DD} = 2.3V to 2.7V			-	0.7	V
		V_{DD} = 2.7V to 3.6V			-	0.8	V
V_{OH}(2)	HIGH level output voltage	V_{DD} = 1.65V to 3.6V	I_o = -100 µA	VDD – 0.2	-	-	V
		V_{DD} = 1.65V	I_o = - 4 mA	1.2	-	-	
		V_{DD} = 2.3V	I_o = - 6 mA	2.0	-	-	
		V_{DD} = 2.3V	I_o = - 12 mA	1.7	-	-	
		V_{DD} = 2.7V	I_o = - 12 mA	2.2	-		
		V_{DD} = 3.0V	I_o = - 12 mA	2.4	-	-	
		V_{DD} = 3.0V	I_o = -24 mA	2.0			
V_{OL}(2)	LOW level output voltage	V_{DD} = 1.65V to 3.6V	I_o = 100 µA	-	-	0.2	V
		V_{DD} = 1.65V	I_o = 4 mA	-	-	0.45	
		V_{DD} = 2.3V	I_o = 6 mA	-	-	0.40	
		V_{DD} = 2.3V	I_o = 12 mA	-	-	0.70	
		V_{DD} = 2.7V	I_o = 12 mA	-	-	0.4	
		V_{DD} = 3.0V	I_o = 24 mA	-	-	0.55	
V_{IK}	Clamp Voltage	V_{DD} = 2.3V	I_{IN} = -18 mA	-	-	-1.2	V
V_H	Input Hysteresis	V_{DD} = 3.3V			100		mV
I_I	Input leakage current per pin	V_{DD} = 3.6V	V_{IN} =V_{DD} or V_{SS}	-		± 5	µA
I_{OZ}(2)	3-state output OFF-state current	V_{DD} = 3.6V	V_O = V_{DD} or V_{SS} $\overline{OE}$ = V_{DD}			± 10	µA
I_{DD}	Quiescent supply Current	V_{DD} = 3.6V	I_o = 0 V_{IN} = V_{DD} or V_{SS}			40	µA
ΔI_{DD}	Additional quiescent supply current	V_{DD} = 3.6V	I_o = 0 One input at V_{DD} - .6V, All others at V_{DD} or V_{SS}			750	µA

Notes:
1. All typical values are measured at T_{amb} = 25 ° C
2. V_{IN} = V_{IL} or V_{IH}

Bus Hold Characteristics

Symbol	Parameter[1]	Test Conditions		Min	Typ[2]	Max	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{DD} = 3.0V	VI = 2.0V	-	-50	-	µA
I_{BHL}	HIGH/LOW		VI = 0.8V	-	50	-	
I_{BHH}	Bus-Hold Input Sustain Current	V_{DD} = 2.3V	VI = 1.7V	-	-40	-	µA
I_{BHL}	HIGH/LOW		VI = 0.7V	-	40	-	
I_{BHH}	Bus-Hold Input Sustain Current	V_{DD} = 1.65V	VI = 1.07V	-	-20	-	µA
I_{BHL}	HIGH/LOW		VI = 0.58 V	-	20	-	
I_{BHHO} I_{BHLO}	Bus-Hold Input Overdrive Current HIGH/LOW	V_{DD} = 3.6V	VI = 0 to 3.6V	-	-	± 200	µA

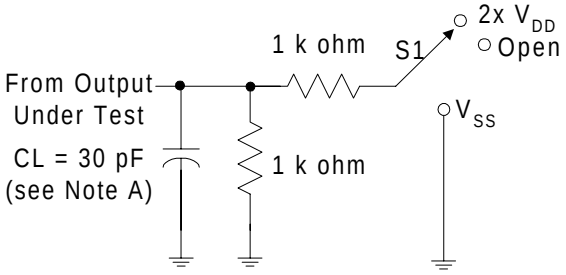
Notes:
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{DD} = 3.3V, + 25°C.

AC Parameters[1]

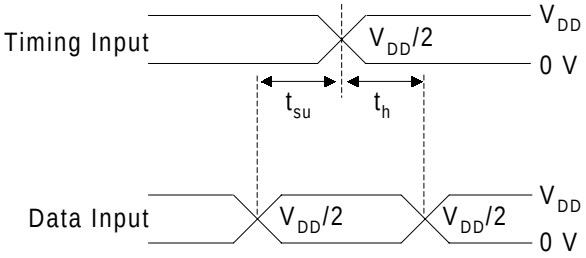
Symbol	Parameter	V_{DD} = 2.5V ± 0.2V		V_{DD} = 2.7V		V_{DD} = 3.3V ± 0.3V		
		Min	Max	Min	Max	Min	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay nAm to nYm	1	3.7	-	3.6	1	3.0	ns
t_{PZH} t_{PZL}	Output Enable Time nOE to nYm	1	5.7	-	5.4	1	4.4	ns
t_{PHz} t_{PLZ}	Output Enable Time nOE to nYm	1	5.2	-	4.6	1	4.1	ns
$t_{sk}(0)$	Output Skew[2]	-	-	-	-	-	500	ps

Notes:
1. See test circuits and waveforms. T_A = -40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

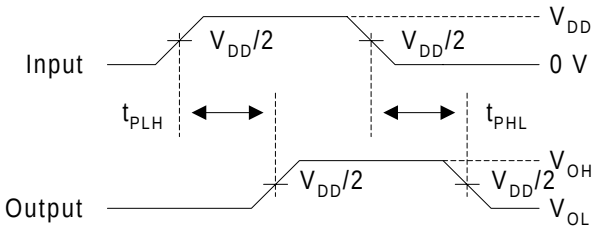
Parameter Measurement Information
V_{DD} = 1.8V



Load Circuit

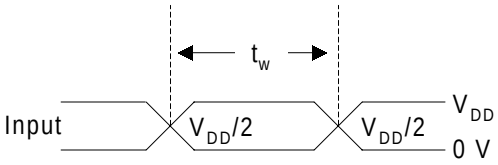


Voltage Waveforms
Setup and Hold Times

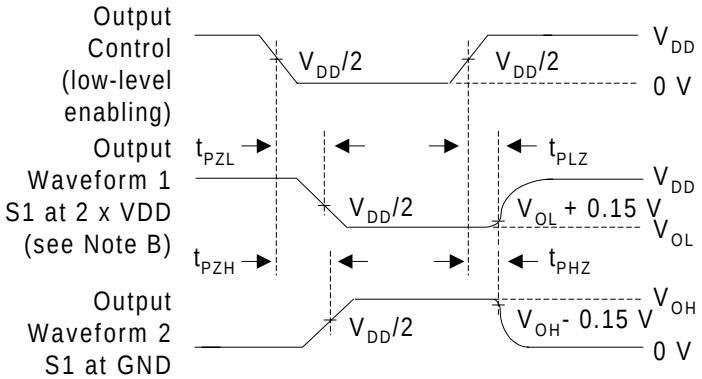


Voltage Waveforms
Propagation Delay Times

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{DD}
t_{PHZ}/t_{PZH}	V_{SS}



Voltage Waveforms
Pulse Duration



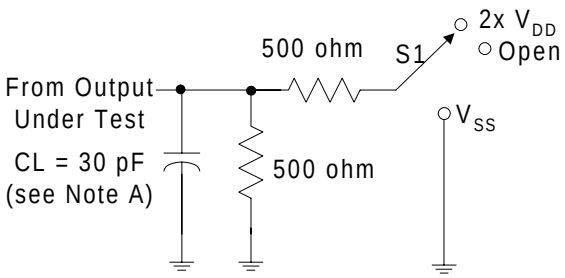
Voltage Waveforms
Enable and Disable Times

Notes:

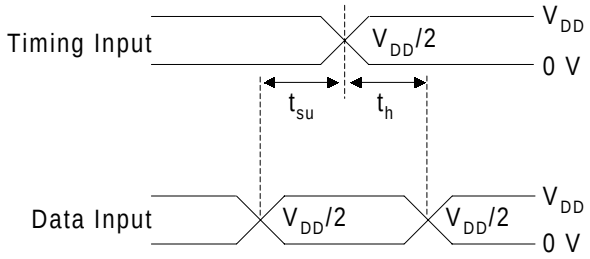
A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω $t_r \leq$ 2 nS, $t_f \leq$ 2nS.
D. The outputs are measured one at a time with on transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Preliminary

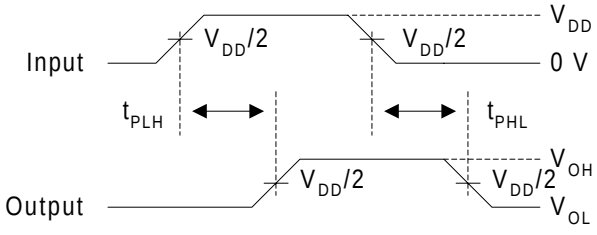
Parameter Measurement Information
V_{DD} = 2.5V ± 0.2 V



Load Circuit

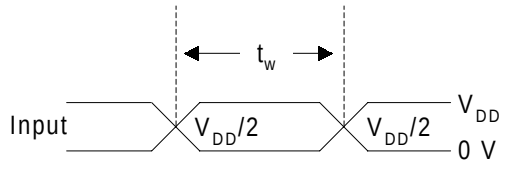


Voltage Waveforms
Setup and Hold Times

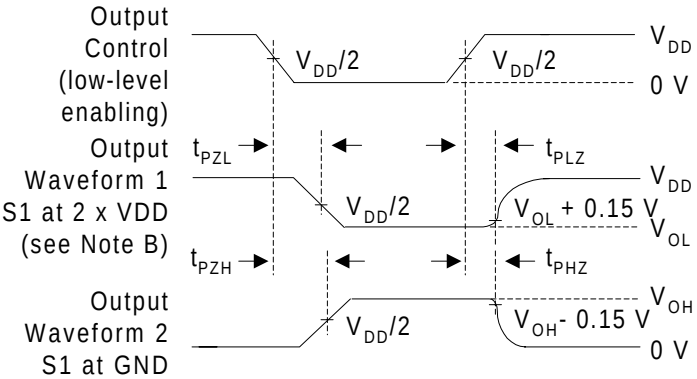


Voltage Waveforms
Propagation Delay Times

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{DD}
t_{PHZ}/t_{PZH}	V_{SS}



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Enable and Disable Times

Notes:

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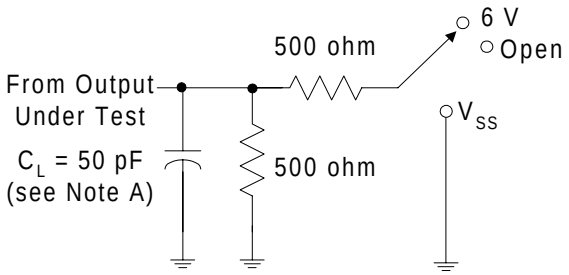
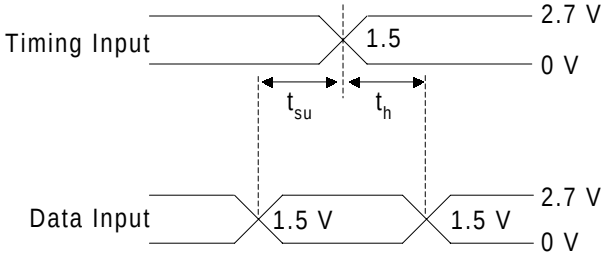
D. The outputs are measured one at a time with on transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Preliminary

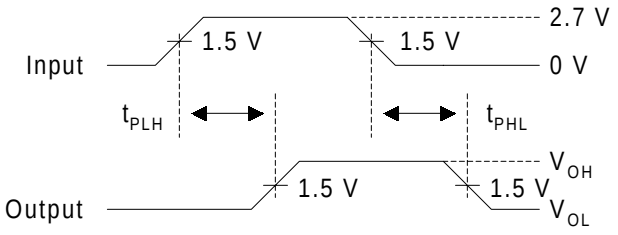
Parameter Measurement Information
VDD = 2.7V and 3.3V ± 0.3V



Load Circuit

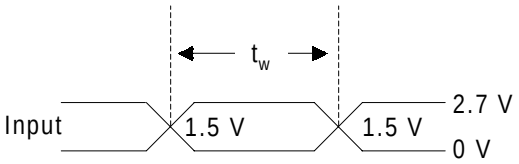


Voltage Waveforms
Setup and Hold Times

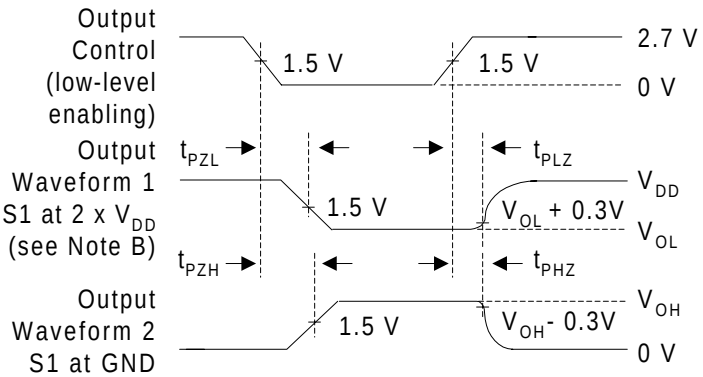


Voltage Waveforms
Propagation Delay Times

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{DD}
t_{PHZ}/t_{PZH}	V_{SS}



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Enable and Disable Times

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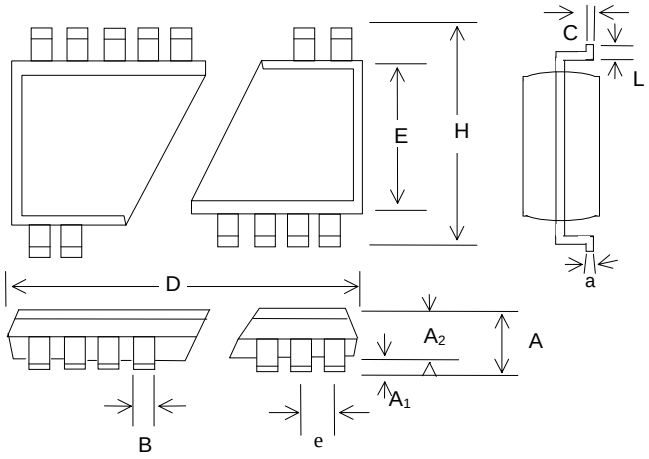
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 nS, $t_f \leq$ 2.5nS.
D. The outputs are measured one at a time with on transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Preliminary

Package Drawing and Dimensions



48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

48 Pin TVSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.005	-	0.009	0.13	-	0.23
C	0.004	-	0.008	0.09	-	0.20
D	0.378	0.382	0.386	9.60	9.70	9.80
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.016 BSC			0.40 BSC		
H		0.252			6.40	
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

48 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.011	0.17	-	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.488	0.492	0.496	12.40	12.50	12.60
E	0.236	0.240	0.244	6.00	6.10	6.20
e	0.02 BSC			0.50 BSC		
H	0.315	0.319	0.323	8.00	8.10	8.20
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

Preliminary

Ordering Information

Part Number	Package Type
ALVCH16245Y	48 Pin SSOP
ALVCH16245T	48 Pin TSSOP
ALVCH16245V	48 Pin TVSOP

Note: the ordering part number is formed by a combination of device number, package and screening as shown below.

Marking: Example:

IMI
ALVCH16245Y
Date Code, Lot #

ALVCH16245Y

Package
Y = SSOP
T = TSSOP
V = TVSOP

IMI Device Number

Notice