

FAST Products

FEATURES

- Combines dual demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as dual 1-of-4 active-High decoder

DESCRIPTION

The 74F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset (\overline{MR}) and Enable (\overline{E}) inputs (see Function Table). In the addressable latch mode, data at the Data inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states, and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held High (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR}=\overline{E}=\text{Low}$), addressed outputs will follow the level of the Data inputs, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

Dual Addressable Latch

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F256	7.0ns	28mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$
16-Pin Plastic DIP	N74F256N
16-Pin Plastic SO	N74F256D

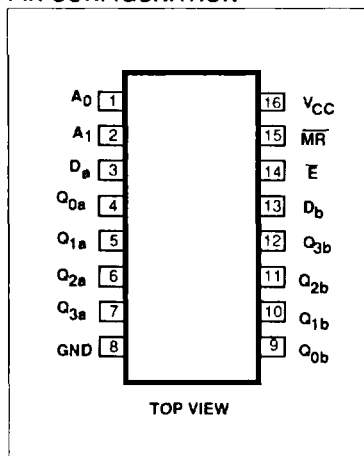
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_a, D_b	Port A, port B inputs	1.0/1.0	20 μ A/0.6mA
A_0, A_1	Address inputs	1.0/1.0	20 μ A/0.6mA
\overline{E}	Enable (active Low)	1.0/1.0	20 μ A/0.6mA
\overline{MR}	Master Reset inputs (active Low)	1.0/1.0	20 μ A/0.6mA
$Q_{0a} - Q_{3a}$	Port A outputs	50/33	1.0mA/20mA
$Q_{0b} - Q_{3b}$	Port B outputs	50/33	1.0mA/20mA

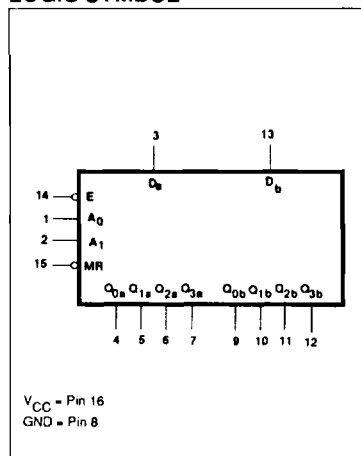
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

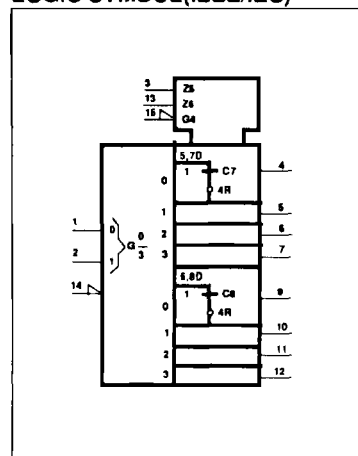
PIN CONFIGURATION



LOGIC SYMBOL



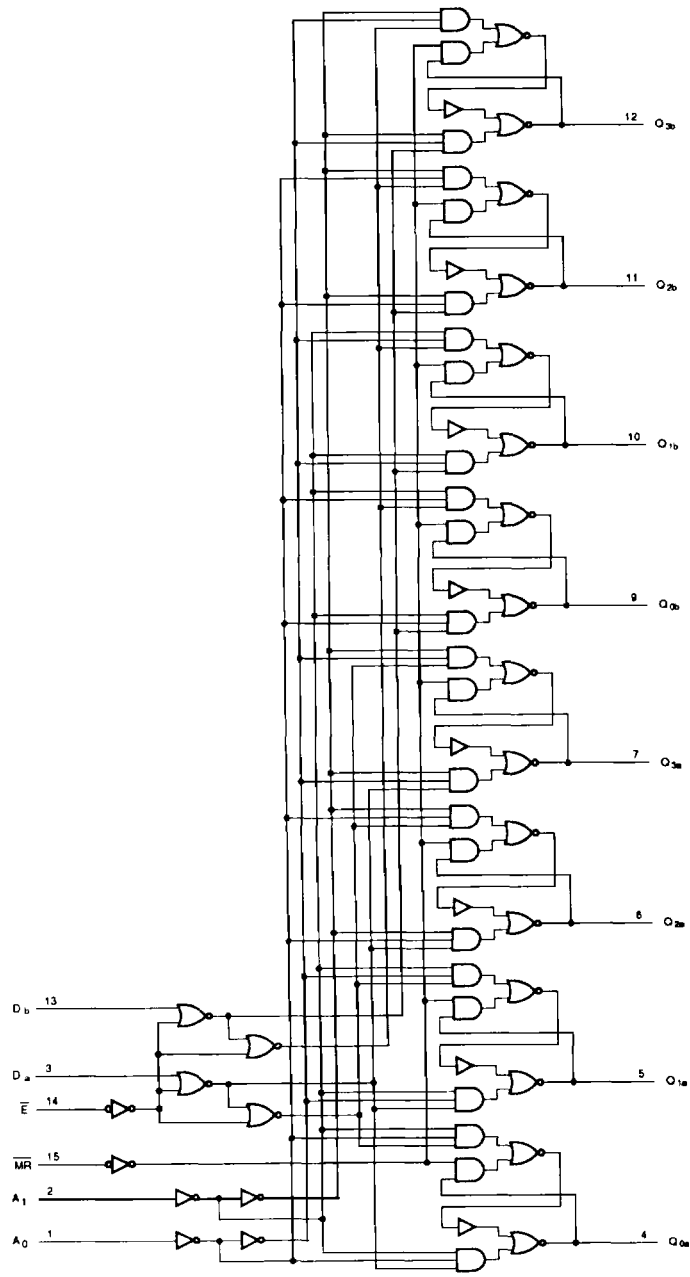
LOGIC SYMBOL (IEEE/IEC)



Latch

FAST 74F256

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

Latch

FAST 74F256

FUNCTION TABLE

INPUTS					OUTPUTS				OPERATING MODE
MR	E	D	A ₀	A ₁	Q ₀	Q ₁	Q ₂	Q ₃	
L	H	X	X	X	L	L	L	L	Master Reset
L	L	d	L	L	Q=d	L	L	L	Demultiplex (active-High decoder when D=H)
L	L	d	H	L	L	Q=d	L	L	
L	L	d	L	H	L	L	Q=d	L	
L	L	d	H	H	L	L	L	Q=d	
H	H	X	X	X	q ₀	q ₁	q ₂	q ₃	Store (do nothing)
H	L	d	L	L	Q=d	q ₁	q ₂	q ₃	Addressable Latch
H	L	d	H	L	q ₀	Q=d	q ₂	q ₃	
H	L	d	L	H	q ₀	q ₁	Q=d	q ₃	
H	L	d	H	H	q ₀	q ₁	q ₂	Q=d	

- H = High voltage level
- L = Low voltage level
- X = Don't care
- d = High or Low data one setup time prior to the Low-to-High Enable transition
- q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	-0.5 to +V _{CC}	V
I _{OUT}	Current applied to output in Low output state	40	mA
T _A	Operating free-air temperature range	0 to +70	°C
T _{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-1	mA
I _{OL}	Low-level output current			20	mA
T _A	Operating free-air temperature range	0		70	°C

Latch

FAST 74F256

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			Min	Typ ²	Max		
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX	±10%V _{CC}	2.5		V	
		V _{IH} = MIN, I _{OH} = MAX	±5%V _{CC}	2.7	3.4	V	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX	±10%V _{CC}		0.35 0.50	V	
		V _{IH} = MIN, I _{OL} = MAX	±5%V _{CC}		0.35 0.50	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}		-0.73	-1.2	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			100	μA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V			-0.6	mA	
I _{OS}	Short circuit output current ³	V _{CC} = MAX			-60	-150	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX		21 42	mA	
		I _{CCL}	V _{CC} = MAX		33 60	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- To reduce the effect of external noise during test.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T _A = +25°C V _{CC} = 5V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = 5V ±10% C _L = 50pF R _L = 500Ω			
			Min	Typ	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation delay D _n to Q _n	Waveform 2	4.0 3.0	7.0 5.0	9.5 7.0	4.0 2.5	10.0 7.5	ns	
t _{PLH} t _{PHL}	Propagation delay E to Q _n	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 7.5	ns	
t _{PLH} t _{PHL}	Propagation delay A _n to Q _n	Waveform 3	5.0 4.5	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns	
t _{PHL}	Propagation delay MR to Q _n	Waveform 4	5.0	7.0	9.0	4.5	10.0	ns	

Latch

FAST 74F256

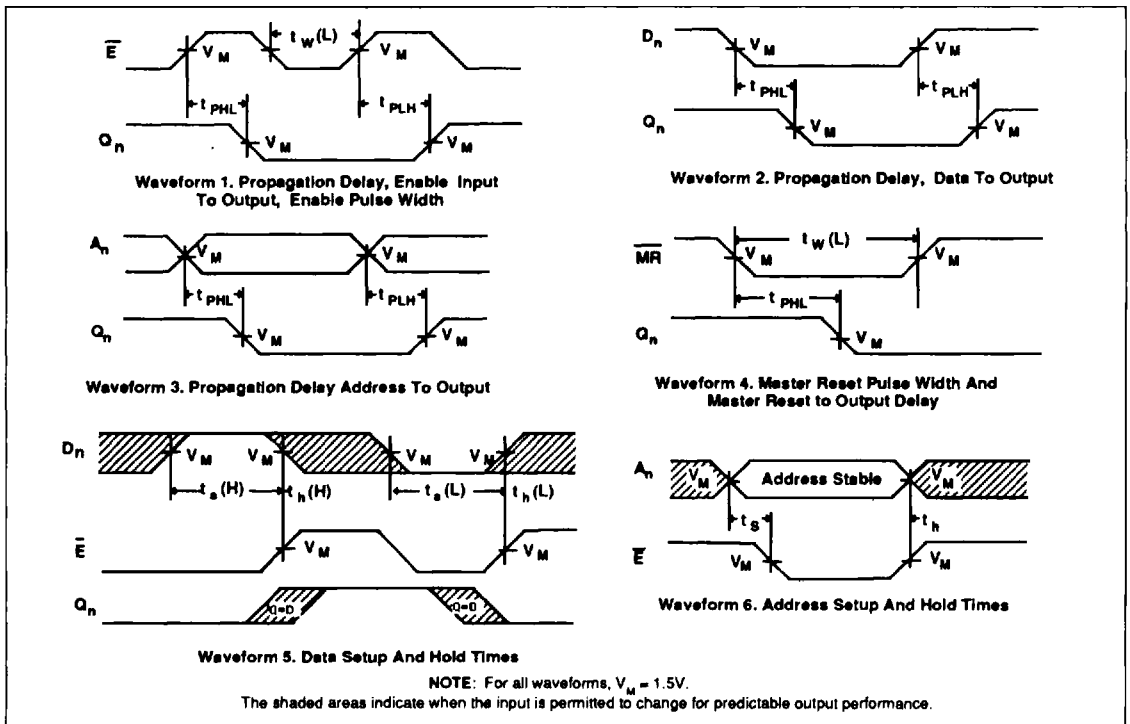
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _A = +25°C V _{CC} = 5V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = 5V ±10% C _L = 50pF R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Setup time, High or Low D _n to E	Waveform 5	3.0 6.5			3.0 7.0		ns
t _h (H) t _h (L)	Hold time, High or Low D _n to E	Waveform 5	0 0			0 0		ns
t _s (H) t _s (L)	Setup time, High or Low A _n to E ¹	Waveform 6	2.0 2.0			2.0 2.0		ns
t _h (H) t _h (L)	Hold time, High or Low A _n to E ²	Waveform 6	0 0			0 0		ns
t _w (L)	E Pulse width, Low	Waveform 1	7.5			8.0		ns
t _w (L)	MR Pulse width, Low	Waveform 4	3.0			3.0		ns

NOTES:

- 1.The Address to Enable setup time is the time before the High-to -Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- 2.The Address to Enable hold time is the time before the Low-to -High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

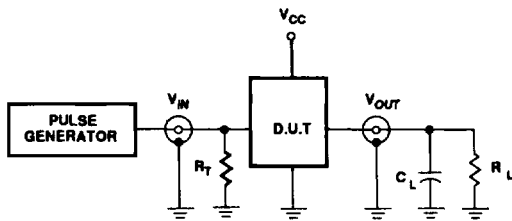
AC WAVEFORMS



Latch

FAST 74F256

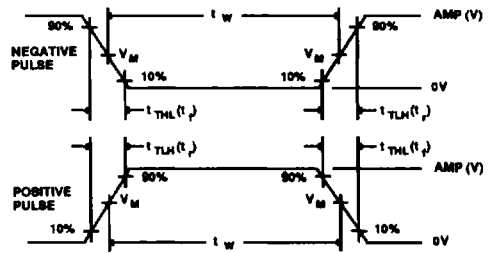
TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns