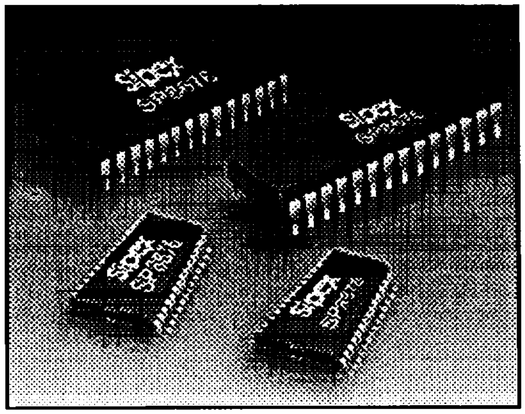
Sipex SP8676

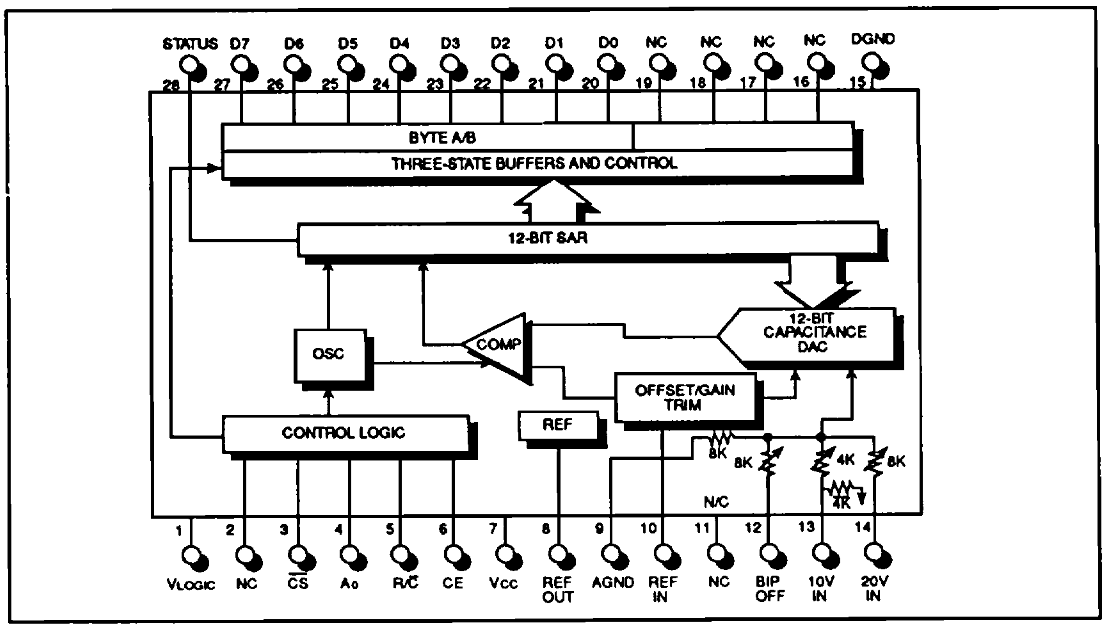
16–Bit Sampling A/D Converter

- Drop in 16-Bit upgrade for existing 12-Bit 674
- Complete Monolithic 16–Bit A/D Converter with Sample–Hold, Reference, Clock and Tri–state Outputs
- Full Nyquist Sampling at 66kHz Sample Rate
- Low Power Dissipation – 200mW
- 15-Bit Linearity Over Temperature
- Commercial and Industrial Temperature Ranges
- Next–Generation Replacement for 674A, 674B, 574A & 574B Devices



DESCRIPTION...

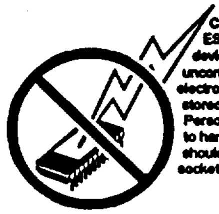
The SP8676 is a complete 16-bit successive approximations A/D converter integrated on a single die with tri-state output latches, internal reference, clock and sample hold. The device is a drop in 16 bit upgrade for the SP674B 12-bit converter (data is read in byte format) and features true Nyquist sampling.



ABSOLUTE MAXIMUM RATINGS

V_{cc} to Digital Common .... 0 to +16.5V
V_{LOGIC} to Digital Common .... 0 to +7V
Analog Common to Digital Common .... ±1V
Control Inputs to Digital Common .... –0.5V to V_{LOGIC} +0.5V
(CE, CS, A_0, R/C)
Analog Input Voltage Range .... ±FS ±30%
Analog Inputs to Analog Common .... ±16.5V
(REF IN, BIP OFF, $10V_{IN}$)
$20V_{IN}$ to Analog Common .... ±24V
REF OUT .... Indefinite short to common
.... Momentary short to V_{cc}
Power Dissipation 1000mW
Lead Temperature, Soldering .... 300°C, 10Sec
J/C .... 45°C/W
MTBF–25°C .... 2.915 million hours

*Inputs exceeding +30% or –30% of FS will cause erratic performance.



CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

(Typical @ 25°C with V_{cc} = +15V, V_{LOGIC} = +5V unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RESOLUTION					
All models			16	Bits	
ANALOG INPUTS					
Input Ranges					
Bipolar		±5, ±10		V	
Unipolar		0 to +10, 0 to +20		V	
Input Impedance					
10 Volt Input	2	2.7	3.5	kΩ	
20 Volt Input	9	10.7	15	kΩ	
Nyquist Frequency		33		kHz	
DIGITAL INPUTS					
Logic Inputs CE, $\overline{CS}$ R/$\overline{C}$, A_0,					
Logic 1	+2.4		+5.5	V	
Logic 0	–0.3		+0.8	V	
Current		±0.1	±50	µA	–0.3V to +5.5V Input
			±5	µA	0V to +5.5V Input
Capacitance		5		pF	
DIGITAL OUTPUTS					
Logic Outputs DB_7–DB_0, STATUS					
Logic 1	+2.4			V	$I_{SOURCE} \leq 500\mu A$
Logic 0			+0.4	V	$I_{SINK} \leq 1.6mA$
Leakage (High Z State)			±40	µA	Data bits only
Capacitance		5		pF	
Parallel Data Output Codes					
Unipolar		Positive true binary			
Bipolar		Positive true offset binary			
INTERNAL REFERENCE					
Output Voltage			10.00 ±0.1	V	
Output Current		2		mA	Note 1
CONVERSION TIME	9		15	µS	

SPECIFICATIONS *(continued)*

(Typical @ 25°C with V_{CC} = +15V, V_{LOGIC} = +5V unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
ACCURACY					
Linearity Error					
–A, –J, –S		.01		%FSR	@ 25°C and T_{MIN} to T_{MAX}
–B, –K, –T		.005		%FSR	@ 25°C and T_{MIN} to T_{MAX}
Differential Linearity Error					Note 2
–A, –J, –S	.01			%FSR	@ 25°C
	.01			%FSR	T_{MIN} to T_{MAX}
–B, –K, –T	.005			%FSR	@ 25°C
	.006			%FSR	T_{MIN} to T_{MAX}
Offset					Note 3
Unipolar		±0.05	±0.075	%FSR	
Bipolar					
–A, –J, –S		±0.125	±0.25	%FSR	
–B, –K, –T		±0.075	±0.15	%FSR	
Full Scale (Gain) Error					% of full scale; T_{MIN} to T_{MAX}
			±0.3	%FS	Note 4
–A			±0.6	%FS	No adjustment @ 25°C
			±0.3	%FS	With adjustment @ 25°C
–B			±0.45	%FS	No adjustment @ 25°C
			±0.15	%FS	With adjustment @ 25°C
–J			±0.5	%FS	No adjustment @ 25°C
			±0.22	%FS	With adjustment @ 25°C
–K			±0.4	%FS	No adjustment @ 25°C
			±0.12	%FS	With adjustment @ 25°C
–S			±0.8	%FS	No adjustment @ 25°C
			±0.5	%FS	With adjustment @ 25°C
–T			±0.6	%FS	No adjustment @ 25°C
			±0.25	%FS	With adjustment @ 25°C
STABILITY					
Unipolar Offset					
–J			±10	ppm/°C	T_{MIN} to T_{MAX}
–K, –A, –S			±3	ppm/°C	T_{MIN} to T_{MAX}
–B, –T			±2.5	ppm/°C	T_{MIN} to T_{MAX}
Bipolar Offset					
–J, –A, –S			±15	ppm/°C	T_{MIN} to T_{MAX}
–K, –B, –T			±5	ppm/°C	T_{MIN} to T_{MAX}
Gain (Scale Factor)					
–J, –A, –S			±50	ppm/°C	T_{MIN} to T_{MAX}
–K, –B, –T			±25	ppm/°C	T_{MIN} to T_{MAX}

SPECIFICATIONS *(continued)*

(Typical @ 25°C with V_{CC} = +15V, V_{EE} = 0V, V_{LOGIC} = +5V unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
POWER REQUIREMENTS					
V_{LOGIC}	+4.5		+5.5	V	
I_{LOGIC}		1	3	mA	
V_{CC}	+11.4		+16.5	V	
I_{CC}		10	12.5	mA	
POWER DISSIPATION		155	200	MW	
ENVIRONMENTAL					
Operating Temperature Range					
–J, –K	0		+70	°C	
–A, –B	–40		+85	°C	
Storage Temperature Range					
–J, –K	–40		+85	°C	
–A, –B, –S, –T	–65		+150	°C	

Notes:
1. Available for external loads. External load should not change during conversion. When supplying an external load and operating on a +12V supply, a buffer amplifier must be provided for the reference output.
2. Minimum resolution for which no missing codes are guaranteed.
3. Externally adjustable to zero. See *Calibration* information.
4. Fixed 50Ω resistor between REF OUT and REF IN.

PIN ASSIGNMENTS...

PIN	FUNCTION	PIN	FUNCTION
1	V_{LOGIC}	28	STATUS
2	NC	27	D7
3	$\overline{CS}$	26	D6
4	A_0	25	D5
5	$R/\overline{C}$	24	D4
6	CE	23	D3
7	V_{CC}	22	D2
8	REF OUT	21	D1
9	AGND(AC)	20	D0
10	REF IN	19	NC
11	N/C*	18	NC
12	BIP OFF	17	NC
13	$10V_{IN}$	16	NC
14	$20V_{IN}$	15	DGND

*This pin is not connected inside the device so it can be tied to −15V, ground, or left floating.

FEATURES...

The SP8676 features standard bipolar and unipolar input ranges of 10V and 20V. Input ranges are controlled by a bipolar offset pin and laser-trimmed for specified linearity, gain and offset accuracy. Power requirements are +5V and +12V to +15V with a maximum dissipation of 200mW at the specified voltages. Conversion time is 15µs. Available are units with 25 or 50ppm/°C temperature coefficients.

The SP8676 is available in six product grades. The -J and -K models are specified over 0°C to + 70°C commercial temperature range; the -A and -B models are specified over the -40°C to +85°C industrial temperature range; Package options include 28-pin CDIP, 28-pin plastic DIP (both narrow and wide), 28-pin PLCC and 28-pin SOIC.

CIRCUIT OPERATION...

The SP8676 is a complete monolithic capacitor DAC-based 16-bit analog-to-digital converter with integral voltage reference, comparator, successive–approximation register (SAR), sample-and-hold, clock, output buffers and control circuitry. The high level of integration of the device means it requires few external components.

When the control section of the SP8676 initiates a conversion command, the clock is enabled and the successive–approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or restarted and data is not available from the output buffers. The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal SP8676 16-bit CDAC is sequenced by the SAR starting from the MSB to the LSB to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to be greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 16-bit binary code which accurately represents the input signal to within ±½ LSB.

The CDAC reference is internal and has excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2mA to an external load in addition to that required to drive the reference input resistor (1mA) and offset resistor (1mA) when operating with ±15V supplies. If the SP8676 is used with ±12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the SP8676 reference must remain constant during conversion.

SAMPLE-AND-HOLD FUNCTION

Although there is no sample-and-hold circuit in the classical sense, the sampling nature of the capacitive DAC makes the **SP8676** appear to have a built-in sample-and-hold. The sample-and-hold function of the CDAC architecture is optimized to provide full Nyquist sampling at the maximum sampling rate. Because the S/H function is included in the ADC circuitry, the majority of the S/H specifications are included within the A/D specifications.

Note that some system architectures may use an external sample-and-hold. The built-in S/H function will provide additional isolation. Once the internal sample is taken by the CDAC capacitance, the input of the SP8676 is disconnected from the input. This prevents transients occurring during conversion from being inflicted upon the attached buffer. Other converter circuits will cause a transient load current on the input which will upset the buffer output and may add error to the conversion itself. In addition, the isolation of the input after the acquisition time allows you the opportunity to release the HOLD on an external sample-and-hold and start it tracking the next sample. This will increase system throughput with your existing components.

The sample/hold function in the SP8676 is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for multiplexer operation, the internal S/H may eliminate the need for an external S/H. The operation of the S/H function is internal and is controlled through the normal R/$\overline{C}$ control line (refer to *Figure 1*). When the R/$\overline{C}$ line makes a negative transition, the device starts the timing of the sampling and conversion. The first two clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as t_{ACQ}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle. Note that because the sample is taken relative to the R/$\overline{C}$ transition, t_{ACQ} (2.1 µs typ) is also the traditional "aperture delay" of this internal sample and hold.

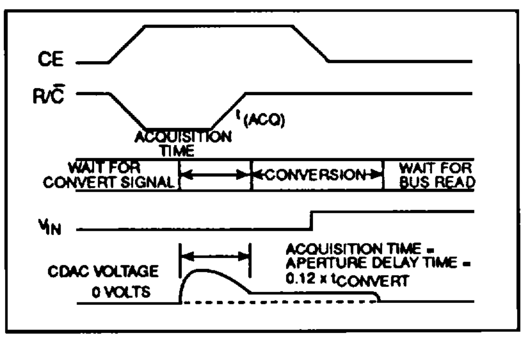


Figure 1. Sample–and–Hold Function

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the SP8676.

USING THE SP8676

Typical Interface Circuit

Strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double–sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two. If this is not possible, run analog signals between ground traces and cross digital lines at right angles only.

Grounding Considerations

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 9mA DC while the digital ground current is 1mA DC. The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance.

Power Supplies

The supply voltages for the SP8676 must be kept as noise free as possible and also regulated from transients or drops. Because the part has 16-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem.

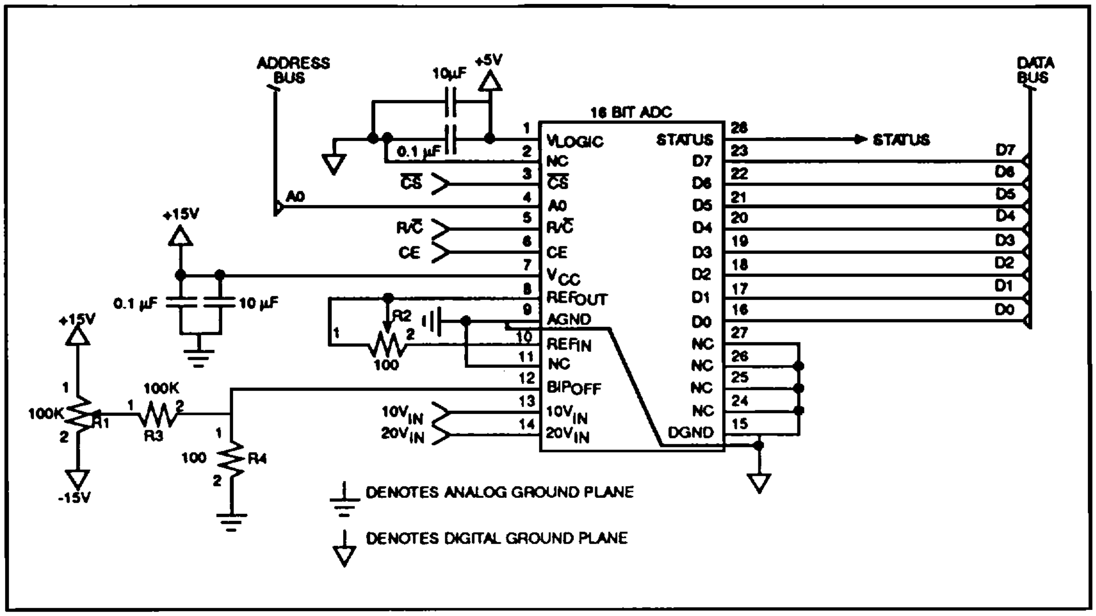


Figure 2. Unipolar Input Connections

Careful filtering and shielding should be employed to prevent noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A 10µF tantalum and a 0.1µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient.

CALIBRATION AND CONNECTION PROCEDURES

Unipolar

The **SP8676** is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary. The device has four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. *Figure 2* depicts a typical interface circuit for operation in a unipolar input mode. *Figure 3* depicts a typical interface circuit for bipolar input mode.

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to *Figure 2*, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of $+\frac{1}{2}$ LSB or 76µV for the 10V range and +153µV for the 20V range should be applied to the device. Adjust the offset potentiometer R_1 for code transition flickers between 0000 0000 0000 0000 and 0000 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is $1\frac{1}{2}$LSB below the nominal full scale which is +9.999771V for the 10V range and +19.999542V for the 20V range. Adjust the gain potentiometer R_2 for flicker between codes 1111 1111 1111 1110 and 1111 1111 1111 1111. If calibration is not necessary for the intended application, replace R_2 with a 50Ω, 1% metal film resistor.

Bipolar

The gain and offset errors listed in the specifications may be adjusted to zero using the potentiometers R_1 and R_2 (See *Figure 3*). If adjustment is not needed, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5V range or to pin 14 for a ±10V range. First apply a DC input voltage $\frac{1}{2}$ LSB above negative full scale which is -4.999924V for the ±5V range or -9.999848V for the ±10V range. Adjust the offset potentiometer R_1 for flicker between output codes 0000 0000 0000 0000 and 0000 0000 0000 0001. Next, apply a DC input voltage $1\frac{1}{2}$ LSB below positive full scale which is +4.999771V for the ±5 range or +9.999542V for the ±10V range. Adjust the gain potentiometer R_2 for flicker between codes 1111 1111 1111 1110 and 1111 1111 1111 1111.

CONTROLLING THE SP8676

Control inputs $\overline{CS}$, A0 and R/$\overline{C}$ are TTL/CMOS compatible. Converter operation is summarized in table 1. A conversion may be initiated by a logic transition on CE, $\overline{CS}$ or R/$\overline{C}$ as shown. One or all of these control inputs may be dynamically controlled and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two must be setup at least 50nS earlier.

The STATUS output is high only when a conversion is in progress. With STATUS high the output data buffers remain in a high impedance state and any additional start convert commands will be ignored. After the STATUS signal goes low data can be read by bringing R/$\overline{C}$ high. Byte read is done by reading B0 through B7 with A0 high, followed by B8 through B15 with A0 low. The A0 control can be connected to the least significant bit of the address bus to store the output data in two consecutive memory locations. With STATUS low a subsequent convert command will be accepted.

CE	$\overline{CS}$	R/$\overline{C}$	A0	STATUS	OPERATION
0	X	X	X	0	NONE
X	1	X	X	0	NONE
↑	0	0	X	0	CONVERT
1	↓	0	X	0	CONVERT
1	0	↓	X	0	CONVERT
1	0	1	0	0	B8 -B15
1	0	1	1	0	B0-B7
X	X	X	X	1	DATA HI-Z, CONVERSION IN PROGRESS

Table 1. Control Input Table

READING OUTPUT DATA

BYTE A (A0=0) BYTE B (A0=1)

D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0

MSB B8 B7 LSB

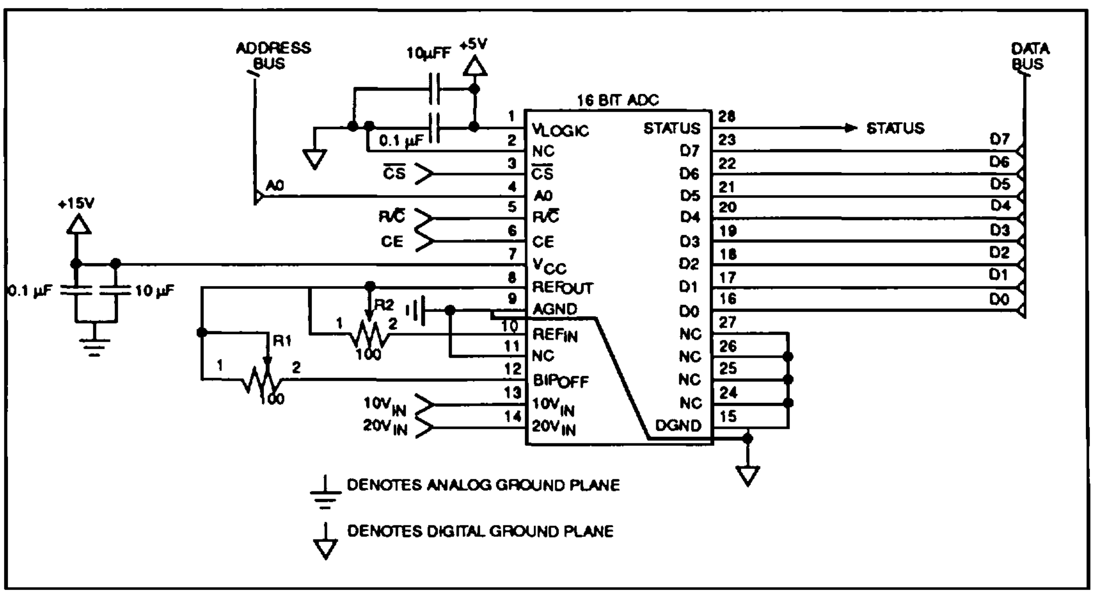
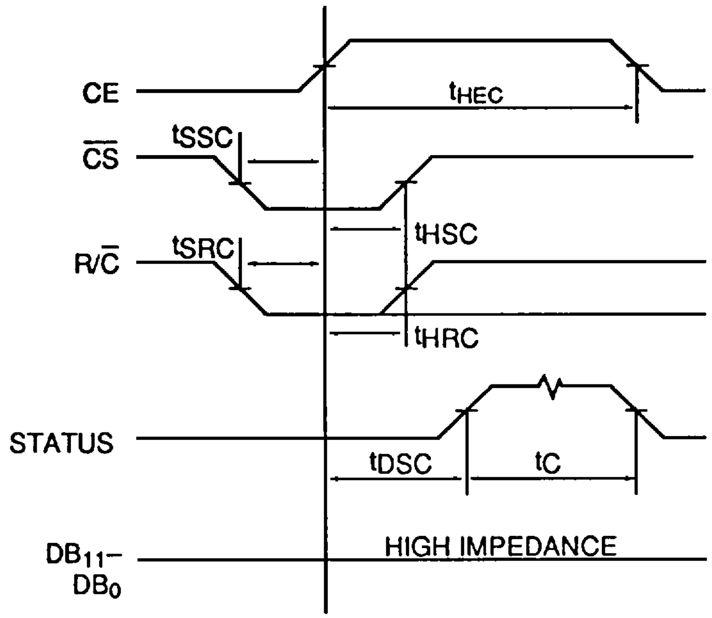


Figure 3. Bipolar Input Connections

CONVERT MODE TIMING



CHARACTERISTICS

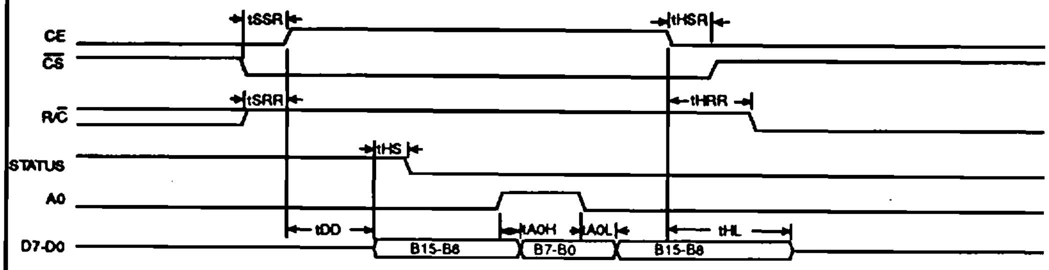
Typical @ 25°C, V_{CC} = +15V or +10V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{DSC} STATUS Delay from CE			200	ns	
t_{HEC} CE Pulse Width	50			ns	
t_{SSC} $\overline{CS}$ to CE Setup	50			ns	
t_{HSC} $\overline{CS}$ Low during CE High	50			ns	
t_{SRC} R/$\overline{C}$ to CE Setup	50			ns	
t_{HRC} R/$\overline{C}$ Low during CE High	50			ns	
t_C Conversion Time[1, 3, 4]	9		15	µs	

NOTES:
1. Parameters guaranteed by design and sample tested.
2. Parameters 100% tested @ 25°C on special orders.
3. 100% tested.
4. T_{MIN} to T_{MAX}.

Figure 6. Convert Mode Timing

READ MODE TIMING



CHARACTERISTICS

Typical @ 25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{DD}	Access Time From CE[2]			150	ns	
t_{HL}	Output Float Delay[2]	25		150	ns	
t_{SSR}	CS to CE Setup	50	0		ns	
t_{SRR}	R/C to CE Setup	0	0		ns	
t_{HSR}	CS Valid After CE Low	0	0		ns	
t_{HRR}	R/C High After CE Low	0	50		ns	
t_{AOH}	A0 High to LS Byte Valid		20		ns	
t_{AOL}	A0 Low to MS Byte Valid		40		ns	
t_{HS}	STS Delay After Data Valid	300		1000	ns	

NOTES:
1. Parameters guaranteed by design and sample tested.
2. Parameters 100% tested @ 25°C on special orders.

Figure 7. Read Mode Timing

STAND–ALONE MODE TIMING CHARACTERISTICS

Typical @ 25°C, V_{CC}= +15V or +12V, V_{LOGIC} = +5V, V_{EE} =0V, unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{HRL} Low R/$\overline{C}$ Pulse Width [2]	50			ns	
t_{DS} STS Delay from R/$\overline{C}$ [2]			200	ns	
t_{HDR} Data Valid After R/$\overline{C}$ Low [2]		25		ns	
t_{HS} STS Delay After Data Valid [2]	300		1000	ns	
t_{HRH} High R/$\overline{C}$ Pulse Width	150			ns	
t_{DDR} Data Access Time			150	ns	

NOTES:
1. Parameters guaranteed by design and sample tested.
2. Parameters 100% tested @ 25°C on special orders.

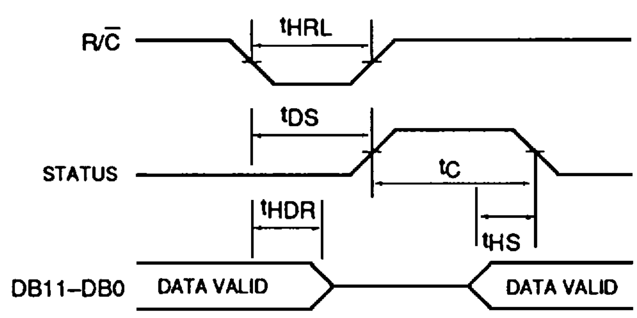


Figure 8. Low Pulse for R/$\overline{C}$ — Outputs Enabled After Conversion

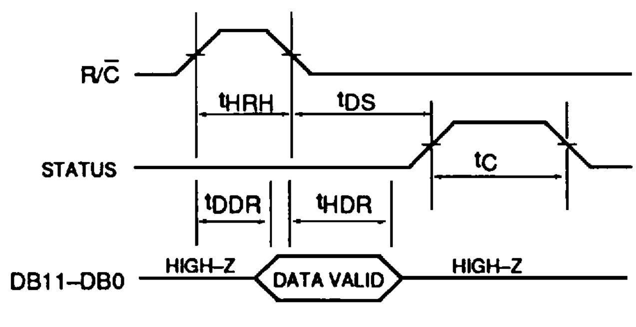
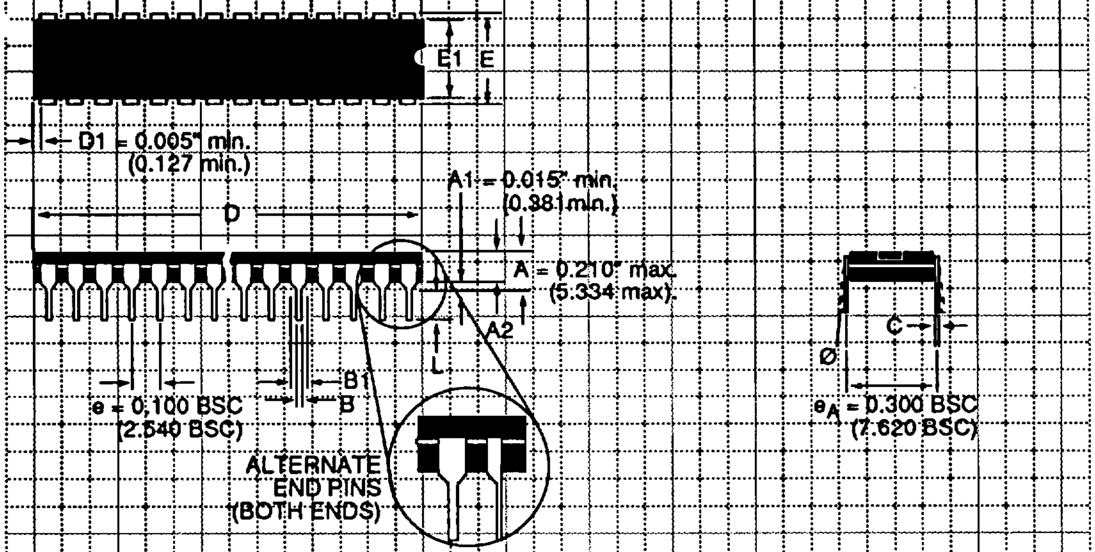
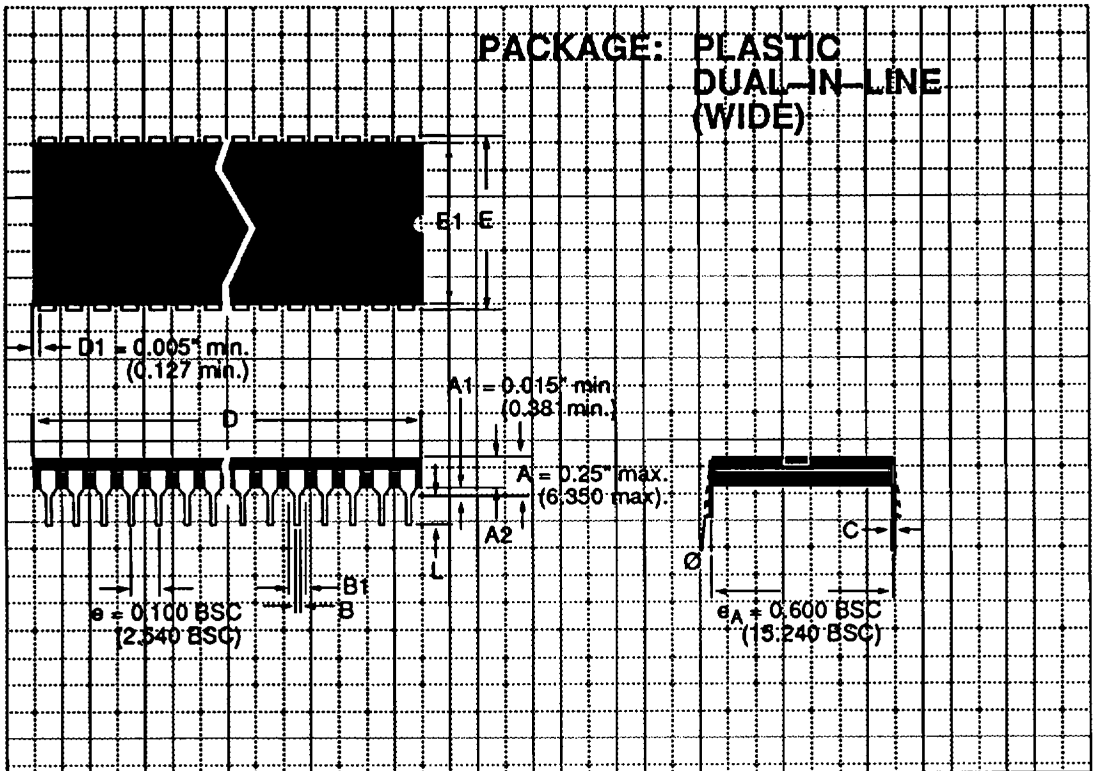


Figure 9. High Pulse For R/$\overline{C}$ — Outputs Enabled While R/C is High, Otherwise High Impedance

PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)

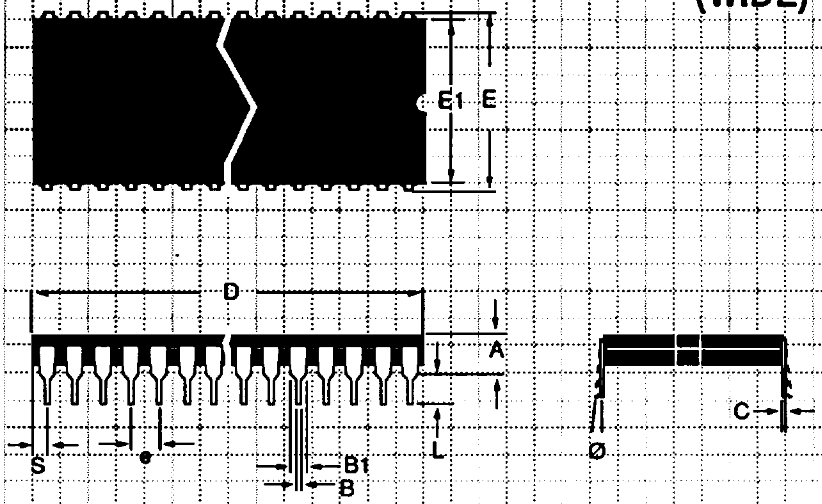


DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN				
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)				
B	0.014/0.023 (0.356/0.584)	0.014/0.022 (0.356/0.559)				
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)				
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)				
D	1.155/1.280 (29.33/32.51)	1.385/1.454 (35.17/36.90)				
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)				
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)				
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)				
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)				



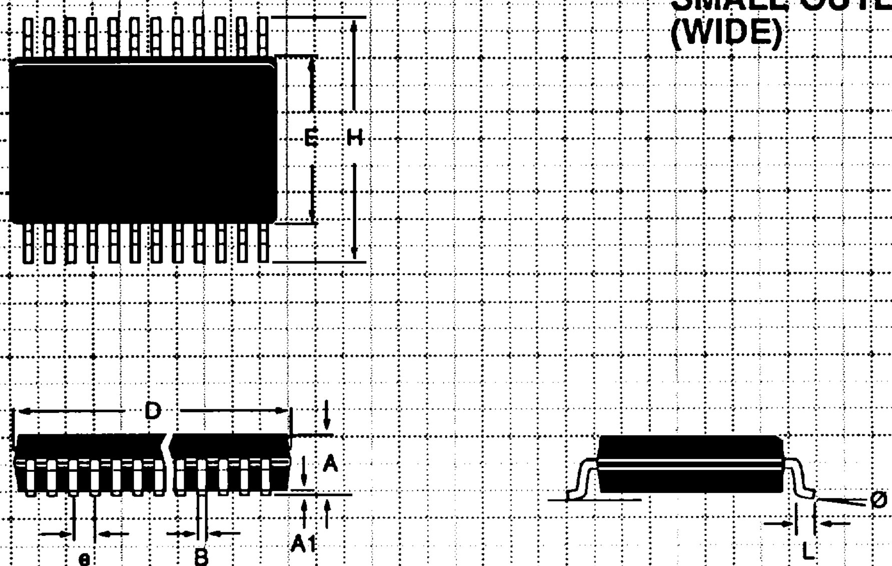
DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN	32–PIN	40–PIN	48–PIN	
A2	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	0.125/0.195 (3.175/4.953)	
B	0.014/0.022 (0.366/0.559	0.014/0.022 (0.366/0.559	0.014/0.022 (0.366/0.559	0.014/0.022 (0.366/0.559)	0.014/0.022 (0.366/0.559)	
B1	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	0.030/0.070 (0.762/1.778)	
C	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	0.008/0.015 (0.203/0.381)	
D	1.150/1.290 (29.21/32.76)	1.380/1.565 (35.05/39.75)	1.645/1.655 (41.78/42.04)	1.980/2.095 (50.29/53.21)	2.385/2.480 (60.57/62.99)	
E	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	0.600/0.625 (15.24/15.87)	
E1	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	0.485/0.580 (12.31/14.73)	
L	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	0.115/0.200 (2.921/5.080)	
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	

PACKAGE: CERAMIC DUAL–IN–LINE (WIDE)



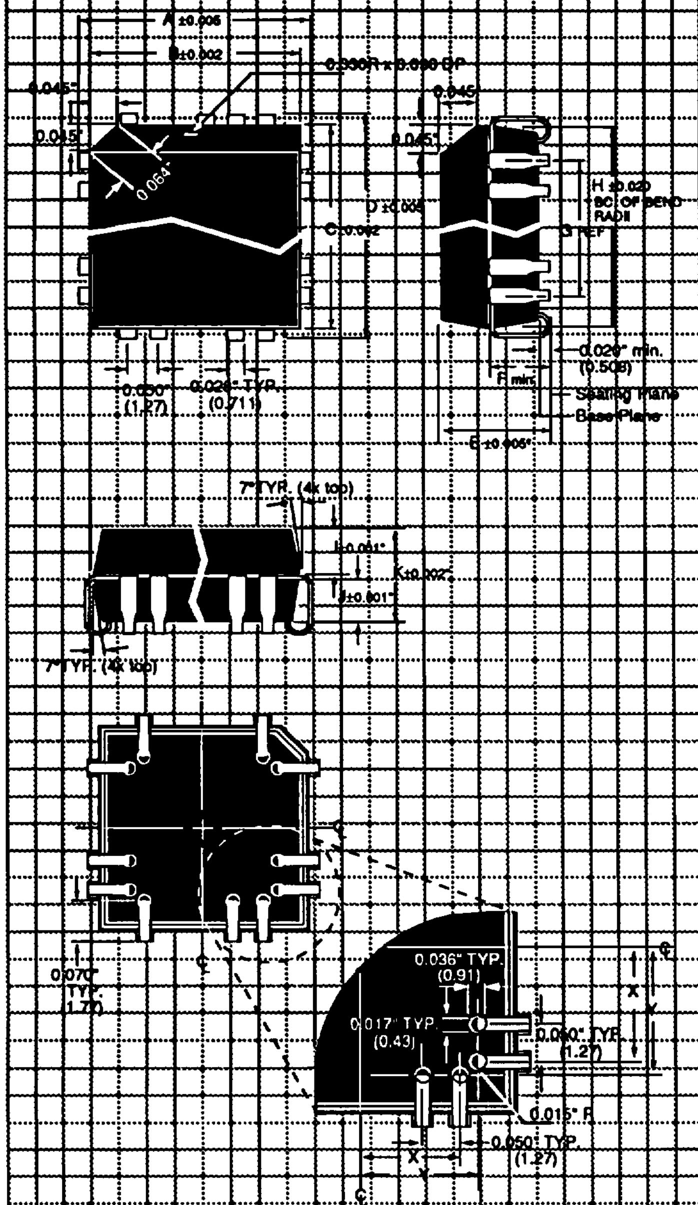
DIMENSIONS (Inches) Minimum/Maximum (mm)	28–PIN
A	0.085/0.225 (2.159/5.72)
B	0.014/0.026 (0.36/0.66)
B1	0.030/0.070 (0.76/1.78)
C	0.008/0.018 (0.20/0.46)
D	1.380/1.490 (35.052/37.846)
E	0.590/0.625 (14.99/15.875)
E1	0.500/0.620 (12.70/15.748)
e	0.100 BSC (2.540 BSC)
L	0.125/0.200 (3.175/5.08)
S	0.030/0.075 (0.762/1.905)
Ø	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (WIDE)



DIMENSIONS (Inches) Minimum/Maximum (mm)	14–PIN	16–PIN	18–PIN	20–PIN	24–PIN	28–PIN
A	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)	0.093/0.104 (2.352/2.649)
A1	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.348/0.363 (8.83/9.22)	0.398/0.413 (10.10/10.49)	0.447/0.463 (11.35/11.74)	0.496/0.512 (12.60/13.00)	0.599/0.614 (15.20/15.59)	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC))	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

PACKAGE: PLASTIC LEADLESS CHIP CARRIER (PLCC)



DIMENSIONS (Inches) Minimum/Maximum (mm)	28–PIN
A	0.485/0.495 (12.31/12.57)
B	0.450/0.456 (11.43/11.58)
C	0.450/0.456 (11.43/11.58)
D	0.485/0.495 (12.31/12.57)
E	0.165/0.180 (4.19/4.57)
F	0.085/– (2.16/–)
G	0.300 REF (7.62 REF)
H	0.390/0.430 (9.906/10.922)
I	0.070/0.072 (1.77/1.83
J	0.070/0.072 (1.77/1.82)
K	0.148/0.152 (3.75/3.86)
X	0.150 REF (3.810 REF)
Y	0.180 REF (4.572 REF)

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP8676J	0°C to +70°C	L, N, P, S
SP8676K	0°C to +70°C	L, N, P, S
SP8676A	-40°C to +85°C	L, N, P, S
SP8676B	-40°C to +85°C	L, N, P, S
SP8676S	-55°C to +85°C	Q
SP8676T	-55°C to +85°C	Q

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Sipex Corporation

22 Linnell Circle
Billerica, MA 01821
TEL: (508) 667-8700
FAX: (508) 670-9001

491 Fairview Way
Milpitas, CA 95035
TEL: (408) 945-9080
FAX: (408) 946-6191

US Regional Sales Offices:

22 Linnell Circle
Billerica, MA 01821

EASTERN U.S.:
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TEL: (508) 667-8700
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European Sales Offices:

GERMANY:
Sipex GmbH
Gautinger Strasse 10
82319 Starnberg
TEL: 49.81.51.89810
FAX: 49.81.51.29598

FRANCE:
Sipex
30 Rue du Morvan, SILIC 525
94633 Rungis Cedex
TEL: 33.1.4687.8336
FAX: 33.1.4560.0784

Far East:

JAPAN:
Tokyo Musen Kizai Co. Ltd.
3-7, Sotokanda 2-Chome,
Chiyoda-ku
Tokyo 101
TEL: 81.3.3253.0545
FAX: 81.3.3255.2738

Nippon Sipex Corporation
Haibara Building
2-3-7 Sotokanda Chiyoda-ku
Tokyo 101
TEL: 81.3.3254.5822
FAX: 81.3.3254.5824