

FEATURES

- Industry Standard Pinouts
- 50, 60, 70 or 80ns RAS Access Time (tRAC)
- Enhanced Page Mode or Static Column Mode
- RAS-Only Refresh, Hidden Refresh and CAS-before-RAS Refresh
- Separate CAS control for the 9th (parity) Data In/Data Out
- Battery Backup Mode with Automatic Refresh
- Commercial Voltage/Temperature Range
4.5 - 5.5 Volts Vcc
0 - 70°C Operating Temperature
- Available in either SIPP (Leaded) or SIMM (Leadless) configuration

See page 12 for Package and Pinout details

MM4M200 J8/J9 SERIES

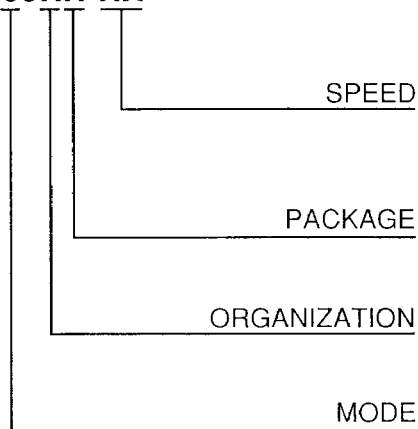
Part Number	tRAC ¹	tCAC ²	tAA ³ (tCAA)	tRC ⁴	tPC ⁵	Icc ⁶ (Standby)	Icc ⁷ (Battery Backup)	Icc ⁸ (Active)	Refresh ⁹ (tREF)
4M x 8/9 - STATIC COLUMN AND ENHANCED PAGE MODE									
MM4M200J8X-05	50ns	13ns	25ns	100ns	30ns	8mA	1.6mA	800mA	16ms
MM4M200J9X-05	50ns	13ns	25ns	100ns	30ns	9mA	1.8mA	900mA	16ms
MM4M200J8X-06	60ns	15ns	30ns	110ns	35ns	8mA	1.6mA	720mA	16ms
MM4M200J9X-06	60ns	15ns	30ns	110ns	35ns	9mA	1.8mA	810mA	16ms
MM4M200J8X-07	70ns	20ns	35ns	130ns	40ns	8mA	1.6mA	640mA	16ms
MM4M200J9X-07	70ns	20ns	35ns	130ns	40ns	9mA	1.8mA	720mA	16ms
MM4M200J8X-08	80ns	20ns	40ns	150ns	45ns	8mA	1.6mA	560mA	16ms
MM4M200J9X-08	80ns	20ns	40ns	150ns	45ns	9mA	1.8mA	630mA	16ms

NOTES:

1. tRAC defines maximum RAS Access Time.
2. tCAC defines maximum CAS Access Time.
3. tAA (alternatively tCAA) defines maximum Column Address Access Time.
4. tRC defines minimum Read or Write Cycle Time.
5. tPC defines minimum Enhanced Page Mode or Static Column Mode Cycle Time.
6. Icc (Standby) defines maximum Vcc supply current with inputs at CMOS levels and RAS, CAS ≥ Vcc - 0.2V.
7. Icc (Battery Backup) defines maximum Vcc supply current while in Battery Backup Mode with CAS ≤ VIL, other inputs at CMOS levels. Refer to Data Sheet for details.
8. Icc (Active) defines maximum Vcc supply current under normal operation with tRC = tRC min., 4.5 ≤ Vcc ≤ 5.5 volts and 0°C ≤ Ta ≤ 70°C.
9. tREF defines the Refresh Interval during which all internal rows (1024) must be refreshed when not in Battery Backup Mode.
10. MM4M200 Family devices are mounted on epoxy-glass PCBs and include 8 or 9 pieces of 0.33 μF decoupling capacitors mounted underneath the memory devices. SIMM (Leadless) module connectors are finished with solder plating over copper. SIPP leads are solder plated.

ORDERING INFORMATION:

AAA4M200JXX-XX



05: 50ns tRAC
06: 60ns tRAC
07: 70ns tRAC
08: 80ns tRAC

L: SIPP (Leaded) (note 10)
S: SIMM (Leadless) (note 10)

8: x8
9: x9

0: Enhanced Page Mode
2: Static Column Mode

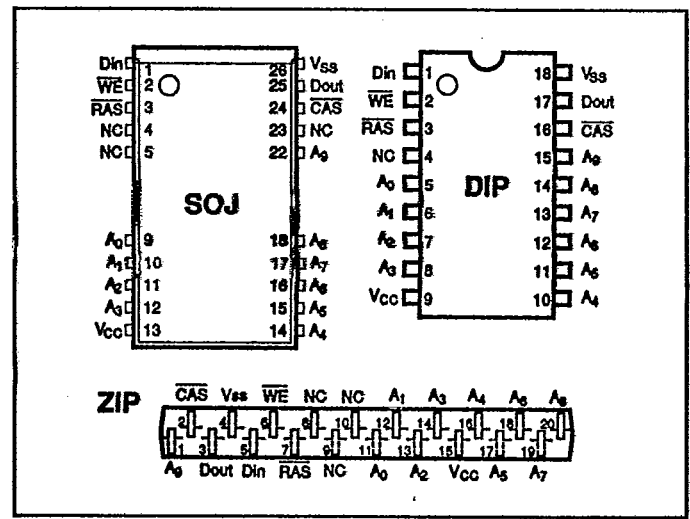
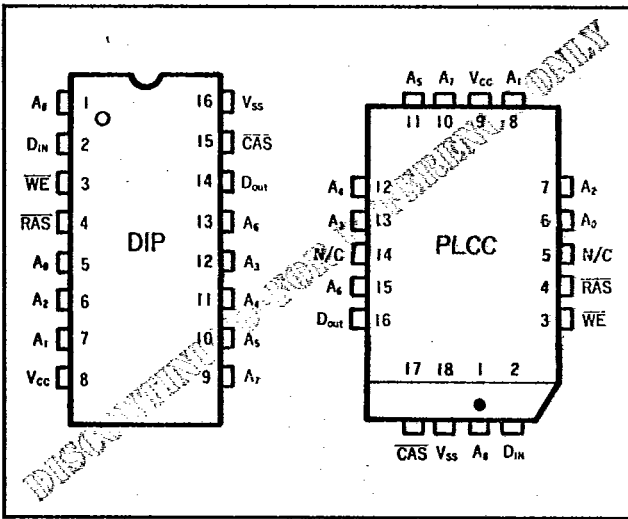
PACKAGE AND PINOUT DETAILS

N M B/ SEMICONDUCTOR DIV 45E D ■ 6429234 0000336 7 ■ NMB

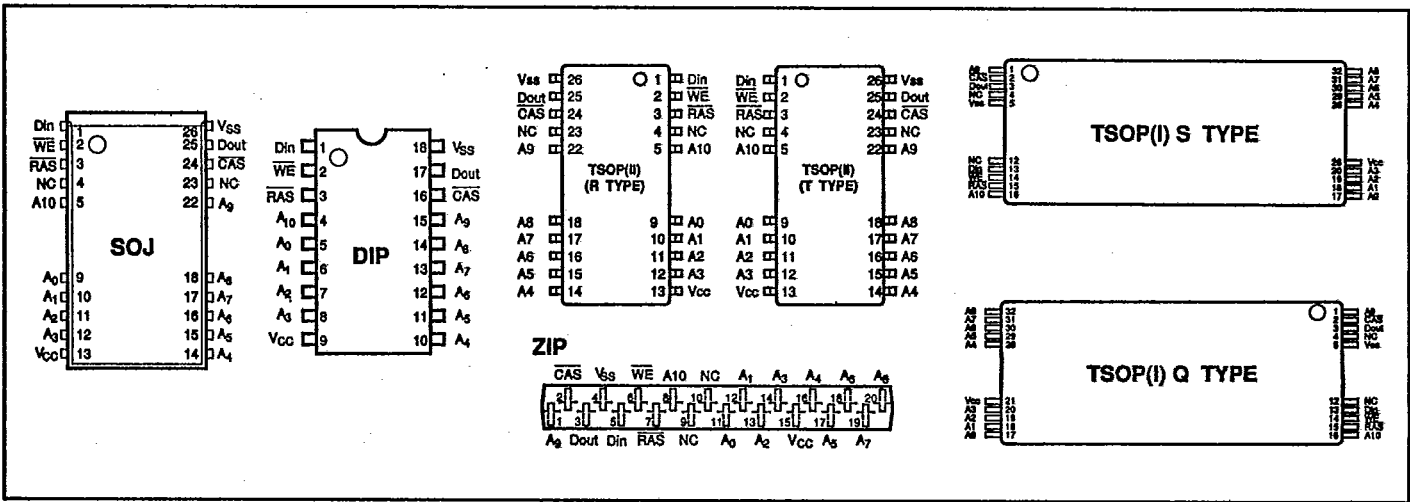
AAA2800 SERIES - 256K x 1

AAA1M300 SERIES - 1M x 1

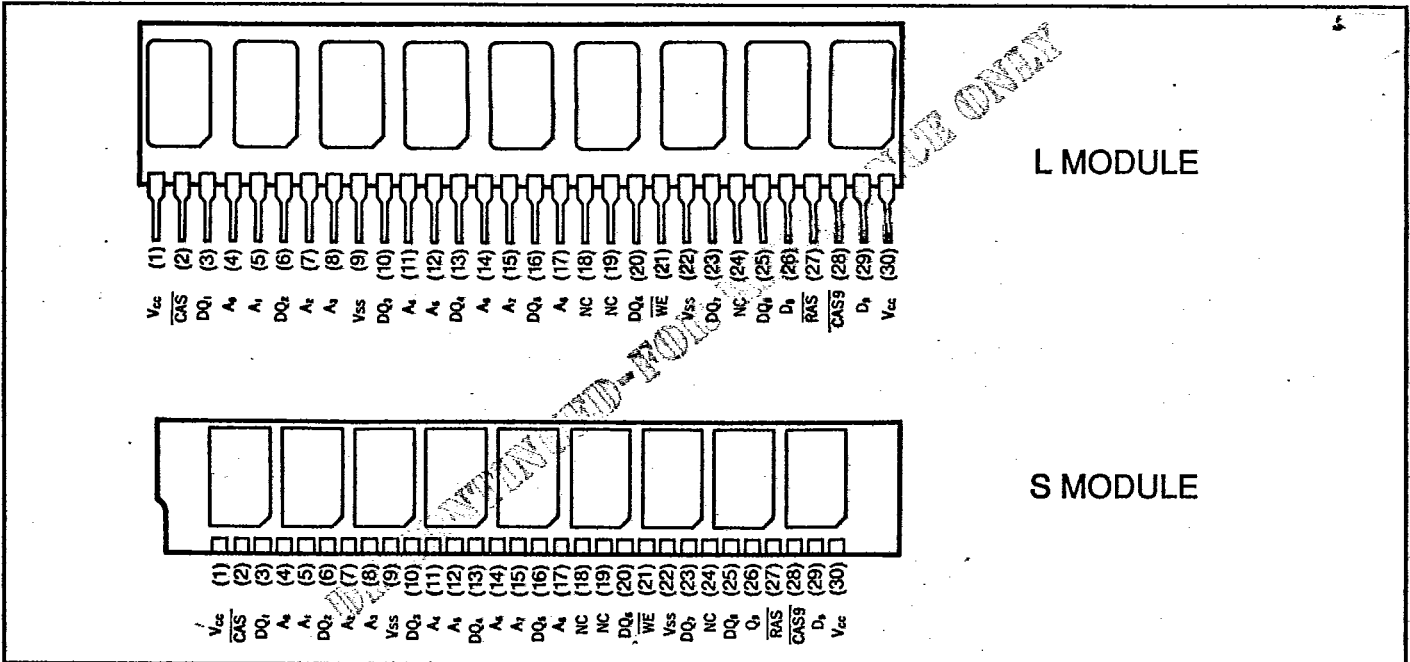
T-91-20



AAA4M200 SERIES - 4M x 1



MM2800 J8/J9 SERIES - 256K x 8/9

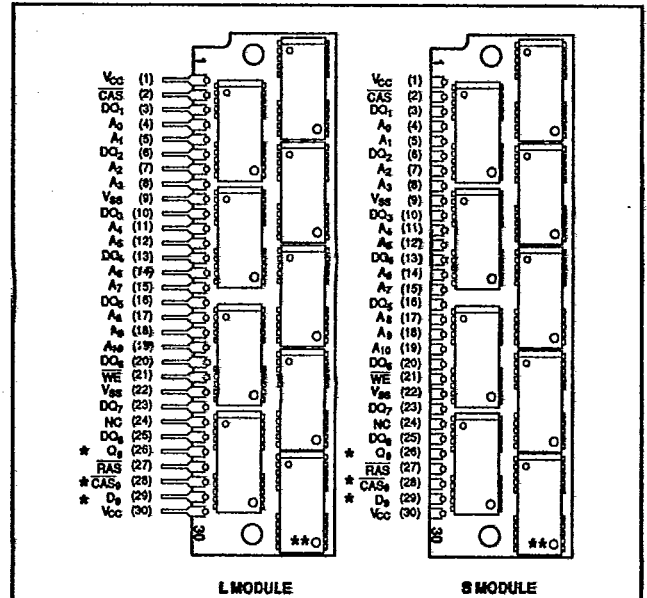
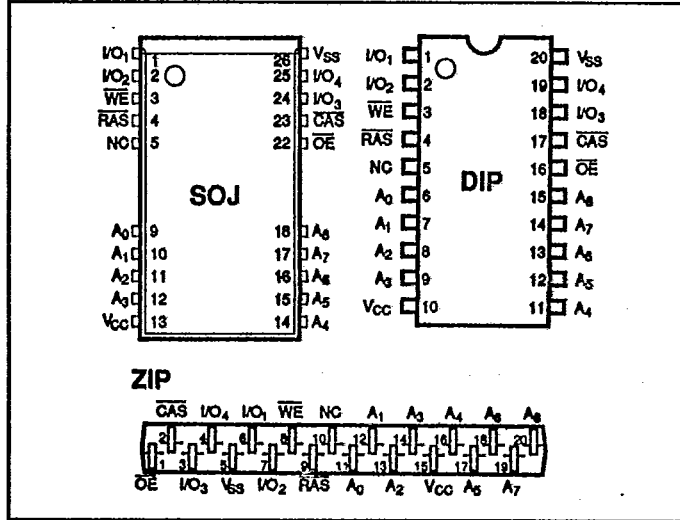


PACKAGE AND PINOUT DETAILS

N M B/ SEMICONDUCTOR DIV 45E D ■ 6429234 0000337 9 ■ NMBT-91-20

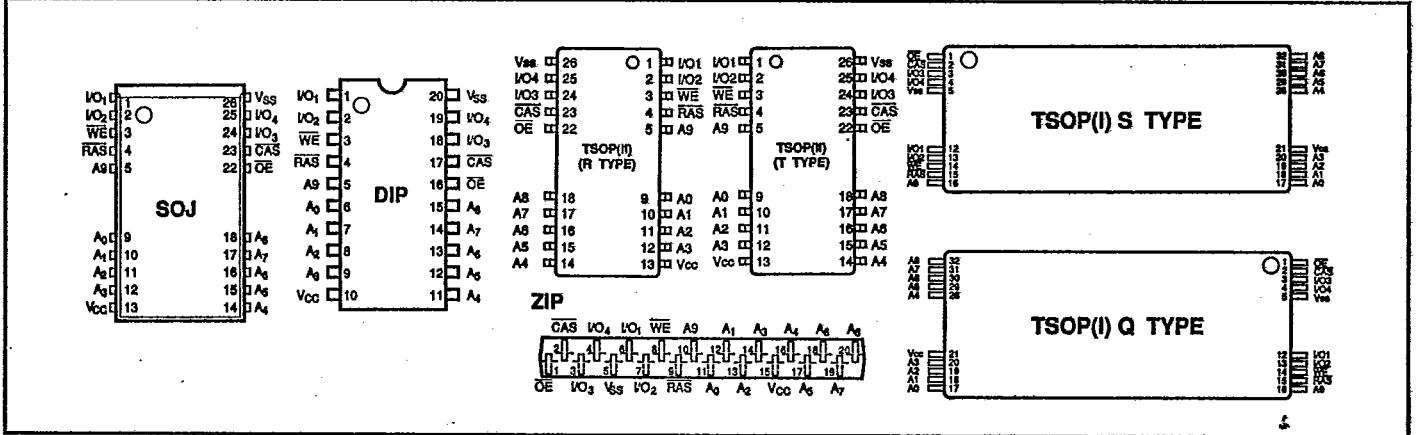
AAA1M300 SERIES - 256K x 4

MM4M200 J8/J9 SERIES - 4M x 8/9



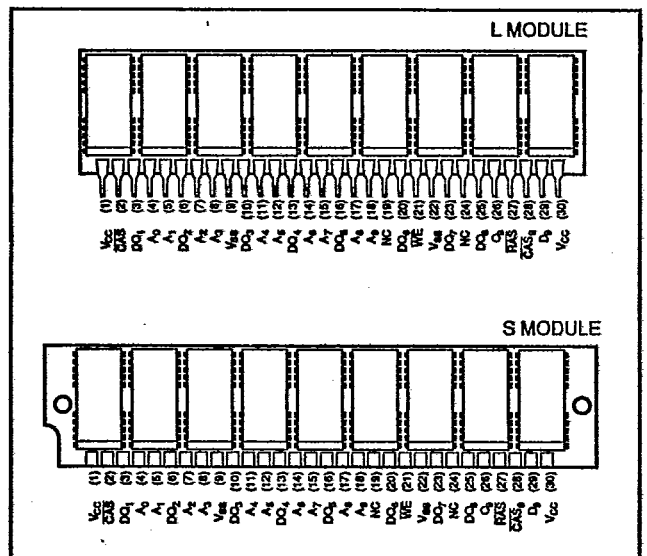
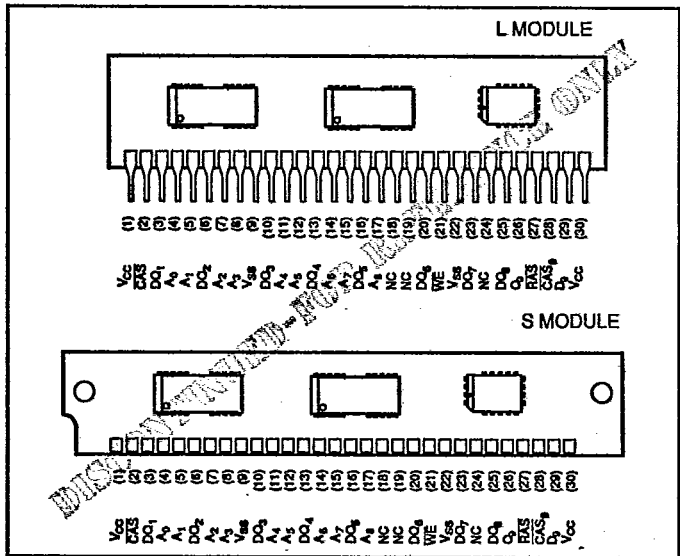
- Notes:
- * No connection (NC) for 4M x 8 bit module.
 - ** This chip is not mounted on 4M x 8 bit module.

AAA4M200 SERIES - 1M x 4



MM256K0J9 SERIES - 256K x 9 (3 CHIP VERSION)

MM1M300J8/J9 SERIES - 1M x 8/9

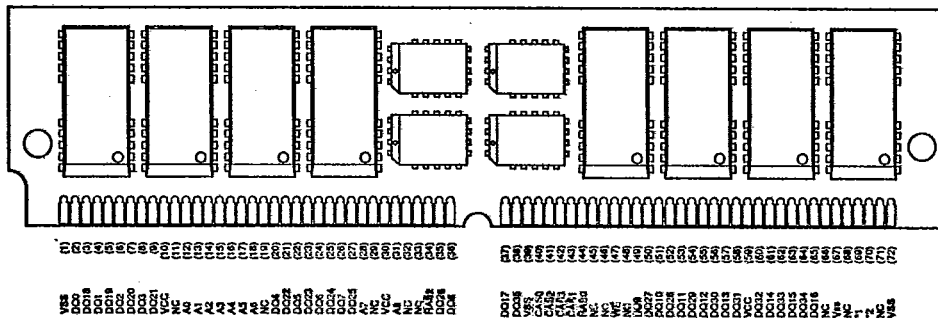


PACKAGE AND PINOUT DETAILS

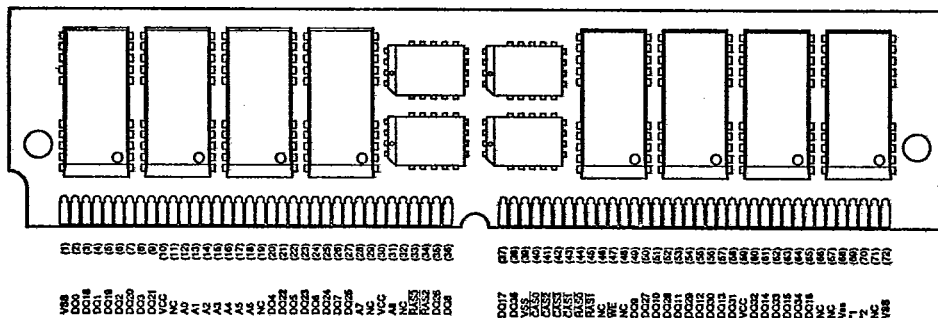
N M B/ SEMICONDUCTOR DIV 45E D ■ 6429234 0000338 0 ■ NMBT-91-20

MM256K0J36/MM512K0J36 SERIES - 256K x 36 and 512K x 36

256K x 36
(Components on one side of PCB)



512K x 36
(Components on both sides of PCB)



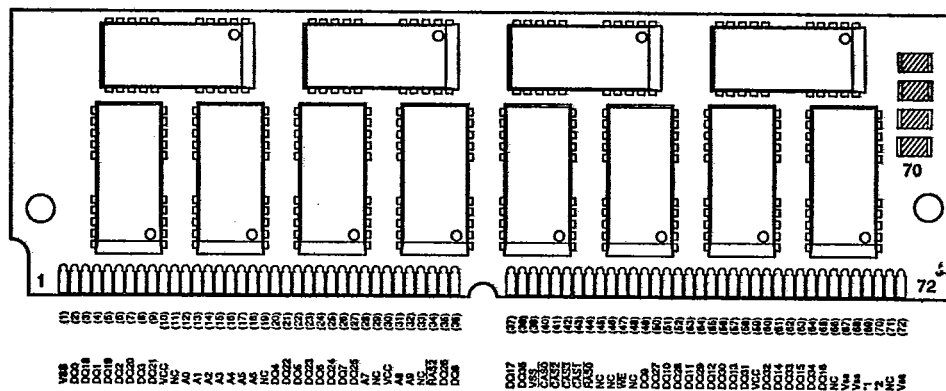
Pinout Variations

	-06	-07	-08
*1	TBD	V _{ss}	NC
*2	TBD	NC	V _{ss}

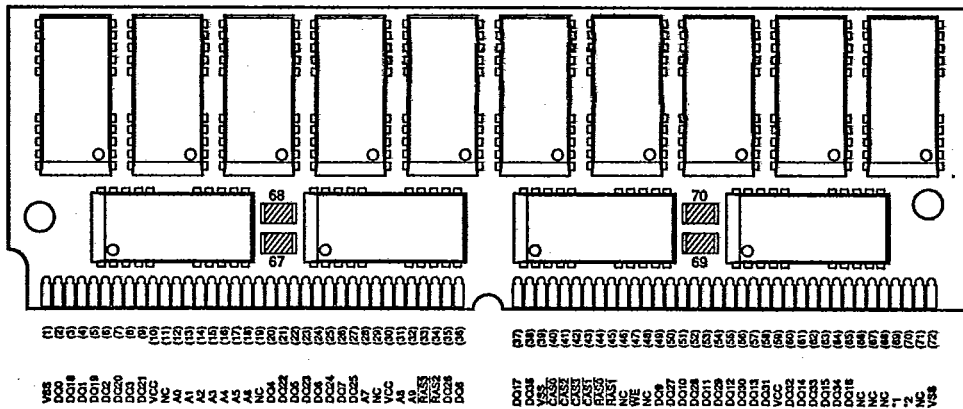
Note: TBD: To be determined

MM1M0J36/MM2M0J36 - 1M x 36 and 2M x 36

1M x 36
(Components on one side of PCB)



2M x 36
(Components on both sides of PCB)



Pinout Variations

	-06	-07	-08
*1	TBD	V _{ss}	NC
*2	TBD	NC	V _{ss}

Note: TBD: To be determined

PACKAGE AND PINOUT DETAILS

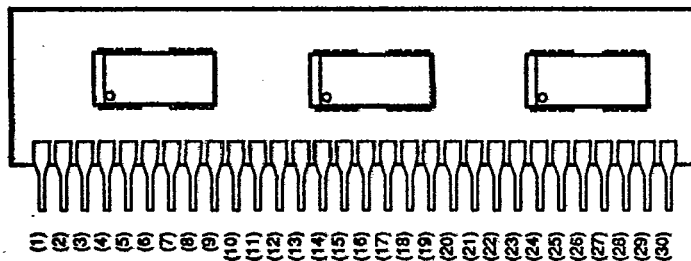
N M B/ SEMICONDUCTOR DIV 45E D ■ 6429234 0000339 2 ■ NMBT-91-20

MM256K0J8R/J9R SERIES - (3 CHIP "R" VERSION)

MM1M0J8/J9 SERIES - (3 CHIP VERSION)

MM1M0J8R/J9R SERIES - (3 CHIP "R" VERSION)

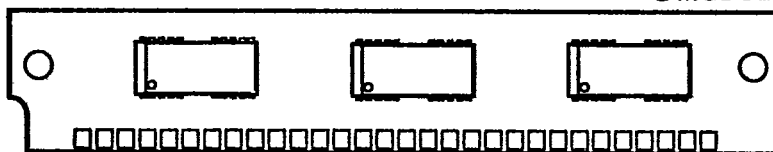
L MODULE



(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13) (14) (15) (16) (17) (18) (19) (20) (21) (22) (23) (24) (25) (26) (27) (28) (29) (30)

V_{CC} CAS₁ DQ₁ A₀ A₁ DQ₂ A₂ A₃ V_{SS} DQ₃ A₄ A₅ DQ₄ A₆ A₇ DQ₅ A₈ NC NC DQ₆ WE V_{SS} DQ₇ NC DQ₈ Q₀ RAS₁ CAS₂ D_p V_{CC}

S MODULE



(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13) (14) (15) (16) (17) (18) (19) (20) (21) (22) (23) (24) (25) (26) (27) (28) (29) (30)

V_{CC} CAS₁ DQ₁ A₀ A₁ DQ₂ A₂ A₃ V_{SS} DQ₃ A₄ A₅ DQ₄ A₆ A₇ DQ₅ A₈ NC NC DQ₆ WE V_{SS} DQ₇ NC DQ₈ Q₀ RAS₁ CAS₂ D_p V_{CC}

Pinout 18 Variations

256K x 8/9	3 Chip "R"	N/C
1M x 8/9	3 Chip	A9
1M x 8/9	3 Chip "R"	A9

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