V.23/V.21 Single Chip Modem

GENERAL DESCRIPTION

The XR-2321 is a single-chip asynchronous continuous phase FSK (Frequency Shift Keying) mode modem. Half or full duplex operation is possible over general switched network or leased line conditions. Modem functions and modes are selected through micro-controller bus structured interfaces. It is compatible with the CCITT recommended standards for V.21 and V.23 type modems.

The XR-2321 can be used with other higher speed Exar modem chips, such as the XR-2400 and XR-2900 chip sets in V.29/V.27ter/V.22bis/V.22/212A multi-modem application.

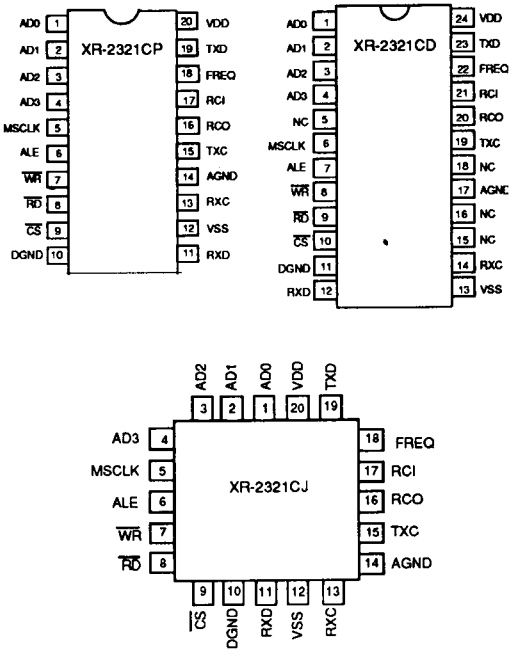
Switched capacitor techniques and CMOS technology are employed in the XR-2321 to perform all major filtering functions and modulation/demodulation respectively. The 75 BPS back channel is also provided when it is selected in V.23 mode.

The XR-2321 is available in a 20 pin DIP or PLCC package. All the digital input and output signals are TTL compatible. Power supply requirements are +/-5 volts.

FEATURES

Dual FSK Modem Chip in a 20-Pin Package
CCITT V.21 (300 BPS Full Duplex) Compatible
CCITT V.23 (1200 BPS Half Duplex Mode 2)
Compatible, also with 75 BPS FSK Back Channel
No External Filtering Required
Analog Loop Back Test Mode
2 Wire Full Duplex for 300 BPS
2 Wire Half Duplex for 1200 BPS
Universal Microcontroller Interface
Low Power CMOS
Generator & Detector for Answer & Calling Tones
Power Down Mode
Line Equalizer Enable or Disable (Selectable)
XR-2100 Pin-to-Pin Compatible

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Power Supply	
VDD	-0.3 to 7V
VSS	0.3 to -7V
Input Voltage	VSS -0.3V to VDD +0.3V
DC Input Current	±10mA
Power Dissipation (Package Limitation)	
Plastic Dip	1W
Derate Above 25°C	
Plastic Dip	5mW/°C
Storage Temperature Range	-65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2321CP	Plastic	0°C to 70°C
XR-2321CJ	PLCC	0°C to 70°C
XR-2321CD	JEDEC SO	0°C to 70°C

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25^{\circ}C$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, $MS_{CLK} = 11.0592$ MHz $\pm 0.05\%$ unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I_{DD}	Positive Supply Current		11		mA	
	Power Down Mode		5		mA	
I_{SS}	Negative Supply Current		12		mA	
	Power Down Mode		5		mA	
V_{IH}	High Level Input Voltage	2.0			V	
V_{IL}	Low Level Input Voltage			0.8	V	
I_{OH}	High Level Output Current			300	µA	$V_{OH} = 2.4$ V
I_{OL}	Low Level Output Current			2	mA	
I_I	Input Current			50	µA	V1 = 0 to V_{DD}
TXC	Transmit Carrier Output	-2	0	+2	dBM	FSK Carrier
RXC	Receiver Dynamic Range	-43		-9	dBM	V.23 option with 1200 baud receive, and the back channel enabled for TX.
		-40		-9	dBM	V.23 option, with 1200 baud transmit and the back channel enabled for RX.
		-43		+10	dBM	V.21 option
CD Off	Carrier Detect Off Level		-48		dBM	FSK
CD On	Carrier Detect On Level		-43		dBM	FSK
CD_{HYS}	Carrier Detect Hysteresis	2	6		dB	FSK,1300 Hz,2100 Hz

SYSTEM PERFORMANCE Transmit Level = -10dBm*, Receive Level = -40dBM*
Conditions: Noise BW = 5KHz, C2, 3002, B/B Line Conditions, 511 PRBP

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
V.21 MODE						
S/N	Signal-to-Noise Ratio		7		dB	BER < 10^{-5}
BIAS DIST	Bias Distortion		6 6		% %	ORIG Mode ANS Mode
V.23 MODE						
S/N	Signal-to-Noise Ratio		15		dB	BER <10^{-6} Primary Channel Receive Reverse Channel Transmit.
BIAS DIST	Bias Distortion		 7 7		 % %	Primary Channel ORIG Mode ANS Mode
S/N	Signal-to-Noise Ratio		7		dB	BER <10^{-5} Reverse Channel Receive Primary Channel Transmit
BIAS DIST	Bias Distortion		 5 5		 % %	Reverse Channel ORIG Mode ANS Mode

FREQUENCY PARAMETERS

Mode	Baud Rate (BPS)	Duplex	Transmit Frequency		Receive Frequency		FREQ Accuracy (Hz)
			Space (Hz)	Mark (Hz)	Space (Hz)	Mark (Hz)	
CCITT V.21 ORIG.	300	FULL	1180	980	1850	1650	+/-2
CCITT V.21 ANS	300	FULL	1850	1650	1180	980	+/-2
CCITT V.23 Primary	1200	HALF	2100	1300	2100	1300	+/-6
CCITT V.23 Reverse	75	HALF	450	390	450	390	+/-2

Answer Tone Frequency: 2100 Hz +/- 6Hz
** The level is measured at Tip and Ring with 600Ω load.*

PIN DESCRIPTIONS

Name	Pin #	I/O	Description
AD0 - AD3	1,2,3,4	I/O	Address/Data bus for microcontroller.
MSCLK	5	I	External master clock input of 11.0592MHz +/- .01%.
ALE	6	I	Address latch enable from microcontroller
$\overline{WR}$	7	I	Write Enable for microcontroller. Active Low.
$\overline{RD}$	8	I	Read Enable for microcontroller. Active Low.
$\overline{CS}$	9	I	Chip select. This enables the 4-bit parallel bus on the XR-2321.
DGND	10	I	Digital Ground. This pin should be routed separately from the AGND trace to the power supply.
RXD	11	O	Demodulated receive data output for V.21, V.23 main or reverse channel.
VSS	12	I	Negative power supply -5V +/- 5%. A 0.1µF ceramic bypass capacitor should be placed near the device.
RXC	13	I	Analog receive carrier input for V.21, V.23 or backward channel signal.
AGND	14	I	Analog Ground. This pin should be routed separate from DGND to the power supply.
TXC	15	O	Analog transmit carrier output for V.21, V.23 main or backward channel signal.
RCO, RCI	16,17	O/I	Receive filter output and demodulator input require 0.1µF +/- 10% ceramic capacitor connected between them.
FREQ	18	O	This pin provides a TTL compatible output of the signal received.
TXD	19	I	Transmit data input for V.21, V.23 main or reverse channel.
VDD	20	I	Positive power supply, +5V. A 0.1 µF ceramic bypass capacitor should be used for this pin.

PIN DESCRIPTION - for "CD" package

AD0-AD3	1,2,3,4	I/O	Address/Data bus for microcontroller.
NC	5,15,16,18	-	
MSCLK	6	I	External master clock input of 11.0592MHz ±0.01%.
ALE	7	I	Address latch enable from microcontroller.
$\overline{WR}$	8	I	Write Enable for microcontroller. Active Low.
$\overline{RD}$	9	I	Read Enable for microcontroller. Active Low.

Name	Pin#	I/O	Description
$\overline{CS}$	10	I	Chip Select. This enables the 4-bit parallel bus on the XR-2321.
DGND	11	I	Digital Ground. This pin should be routed separately from the AGND trace to the power supply.
RXD	12	O	Demodulated receive data output for V.21, V.23 main or reverse channel.
VSS	13	I	Negative power supply.
RXC	14	I	Analog receive carrier input for V.21, V.23 or backward channel signal.
AGND	17	I	Analog Ground. This pin should be routed separate from DGND to the power supply.
TXC	19	O	Analog transmit carrier output for V.21, V.23 main or backward channel signal.
RCO, RCI	20,21	O/I	Receive filter output and demodulator input require 0.1µF ±10% ceramic capacitor connected between them.
FREQ	22	O	This pin provides a TTL compatible limited output of the signal received.
TXD	23	I	Transmit data input for V.21, V.23 main or reverse channel.
VDD	24	I	Positive power supply, +5V. A 0.1µF ceramic bypass capacitor should be used for this pin.

FUNCTIONAL DESCRIPTION

As outlined in Figure 1, the XR-2321 consists of three main sections which perform the functions of transmitter, receiver and logic control.

Transmitter

The transmitter section consists of a Frequency Shift Keying (FSK) modulator, a Digital-to-Analog (D/A) converter, transmit filter, and an output gain stage. Its primary function is to convert binary digital data into a corresponding analog signal suitable for transmission on the telephone line system.

The binary data appears at the input of the FSK modulator at the TRANSMIT DATA (TXD) pin. The modulator creates a digitally synthesized sine wave at a given frequency depending on whether a logic 1 or logic 0 is present at the TXD pin. Following a digital filtering stage in the FSK modulator, this digital representation is converted into an analog signal by the DAC. The signal is then filtered by the transmit filter which is implemented using switched capacitor techniques. The resulting signal is finally smoothed using a continuous time low-pass filter and amplified by a programmable gain stage. The FSK-modulated carrier is then brought to the output TRANSMIT CARRIER (TXC) pin, and normally applied to the phone line through a Data Access Arrangement (DAA) interface or an acoustic coupler.

Receiver

The receiver consists of an anti-aliasing filter, a receive filter, a tone conditioner, a slicer, a FSK demodulator, a carrier detector, and a post-detection filter. Its function is to recover the binary digital information from the received analog signal.

The FSK-modulated carrier is received through a DAA or acoustic coupler and fed to the RECEIVE CARRIER (RXC) input pin. The signal is first presented to a simple low-pass anti-aliasing filter and then routed to both the receive band-pass filter and the tone conditioning section. This latter section provides a TTL compatible limited output of the received analog signal at the FREQUENCY OUTPUT (FREQ) output pin. Along the other route, the receive filter band limits the signal and passes it to the slicer section which creates a digital bit stream. This bit stream is processed by the FSK demodulator and passed through a post-detection filter. The resulting signal is squared off by the output comparator section whose output now represents the recovered data pattern. This is made available at the RECEIVE DATA (RXD) output.

A CARRIER DETECT (CD) signal is also generated from the received line carrier after the receive filter. The CD signal, which is used to indicate the presence of valid data, is read via the data bus by addressing the READ register of the XR-2321. Control programming information is discussed in the following section.

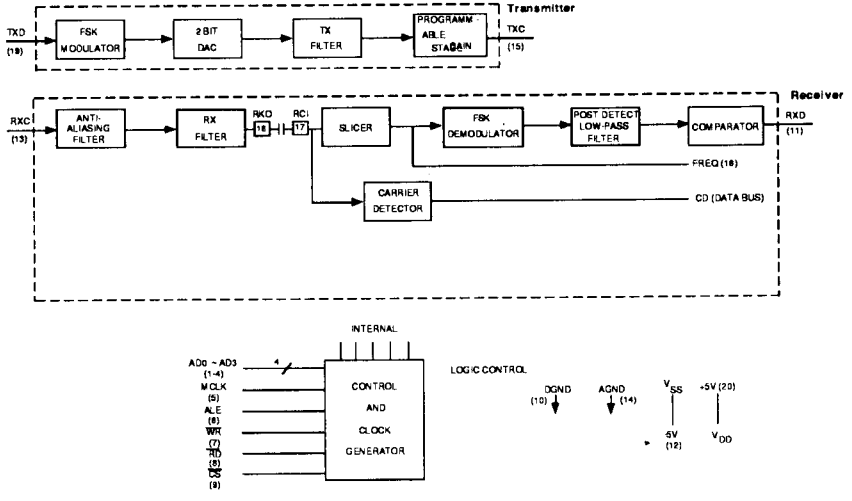


Figure 1. Functional Block Diagram

CONTROL PROGRAMMING INFORMATION

Operation of the XR-2321 is programmed via the read and write registers which are accessed by the AD0-AD3 pins. Control and mode configuration is acheived by writing control words into the appropriate write register, while status and data information can be read from the read register. Read/write register address locations are given in Table 1.

Register bit formats are shown in Table 2. By following the READ/WRITE cycle procedure outlined in Figure 2, the individual bits can be accessed. Figure 2 outlines the timing applicable to interfacing the XR-2321 with the 8031 or alike modem controllers.

Write Register Bit Description

ALB - Analog Loop Back

This bit will activate analog loop-back mode for diagnostic testing purposes.

RXDMK - Receive Data Mark

By setting this bit high, the user can force the RXD output pin high continuously. This is useful when performing functions such as handshaking protocol and/or CD is off.

A/O - Answer/Originate Mode

In the low state, this bit will configure the modem in originate mode and conversely, when set high, the modem will be in answer mode.

TONE/FSK - Transmit Tone or Transmit FSK Modulated Carrier

This bit controls the TXC output pin to transmit the 2100 Hz answer/ 1300 Hz calling tone when the bit is set high. When low, TXC will be the standard FSK-modulated carrier. (Note: TONE/DTMF = 1 for tone operation.)

TXD - Transmit Data

This bit is the data bit to be transmitted and is loaded via the data bus.

PDN - Power Down Mode
When selected, all sections of the device are powered off except for the control section. This mode allows for reduced power consumption when the modem is not receiving or transmitting.

TXEN - Transmitter Enable

When set low the transmitter output is disabled.

CPM - Call Progress Mode

This bit is set high when the modem is attempting call establishment in originate mode by monitoring dial tone, ring back tone or busy tone.

TONE/DTMF

With this bit set high, the transmitter will operate at tone frequencies corresponding to the given configuration. When set low, the transmitter is set to DTMF mode and follows the configuration programmed in the DTMF Bit Select register.

V.23/V.21

This configuration bit is to set the modem in V.23 or V.21 communications mode. V.23 is selected with this bit high, while V.21 is set with this bit low.

PTXD - Parallel Transmit Data

This bit allows the user to select whether data to be transmitted is loaded from the parallel data bus, or if it is to be loaded serially from the TXD pin. With PTXD set low, data is taken from pin 19 (TXD).

DTH3 - DTH2/DTL1 - DTL0 - DTMF Bit Select

These bits are used to set the DTMF frequencies to be transmitted. The bits are programmed according to Table 4 - DTMF Bit Selectable Table.

TX3 - TX0 - Transmit Gain Bit Select. Refer to Table 5 for gain selection.

Read Register Bit Descriptions

FREQ - Frequency Output

Reading from this bit is equivalent to pin 18 FREQ output. It provides a TTL version of the received analog signal.

CD - Carrier Detect

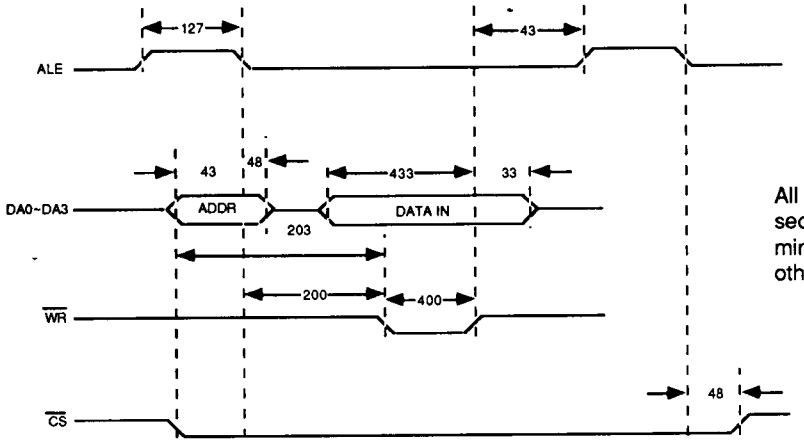
If this bit is high, it indicates the presence of a valid signal in the receive band.

RXD - Receive Data

Demodulated digital data is read from this bit. When data is read from this register, the RXD pin can be ignored.

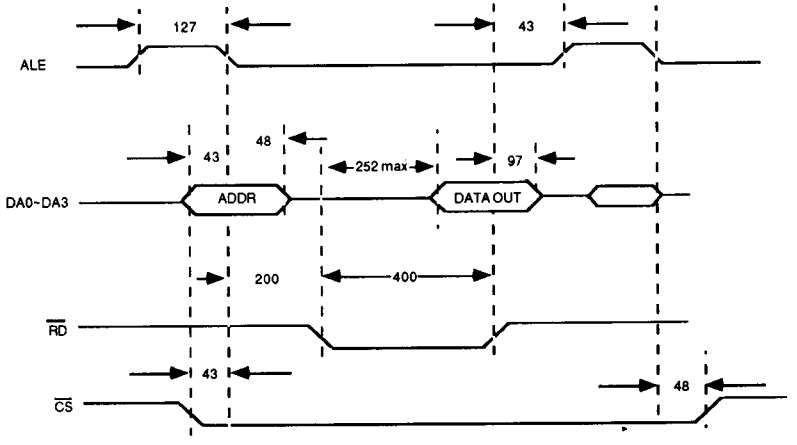
Mode Configuration Programming

Tables 3 to 5 detail the necessary bit register programming steps for each configuration mode, DTMF select and transmit carrier gain select levels respectively.



All units are in nanoseconds and are minimum values, unless otherwise specified.

Write Cycle



Read Cycle

Figure 2. Read/Write Timing Waveforms (12MHz Clock)

CONTROL REGISTERS FOR XR-2321

	ADDRESS BITS				
	AD3	AD2	AD1	AD0	HEX
$\overline{WR}$=0	1	0	0	0	(8)
	1	0	0	1	(9)
	1	0	1	0	(A)
	1	0	1	1	(B)
	1	1	0	0	(C)
$\overline{RD}$=0	1	0	0	0	(8)

Table 1. Read/Write Register Address Locations

	DATA BITS				
	BIT 3	BIT 2	BIT 1	BIT 0	ADDR
$\overline{WR}$=0	ALB	RXDMK	A/$\overline{O}$	TONE/$\overline{FSK}$	(8)
	$\overline{V.23}$ EQ	TXD	PDN	TXEN	(9)
	CPM	TONE/$\overline{DTMF}$	V23/$\overline{V21}$	PTXD	(A)
	DTH3	DTH2	DTL1	DTL0	(B)
	TX3	TX2	TX1	TX0	(C)
$\overline{RD}$=0	***	FREQ	CD	RXD	(8)

Table 2. Read/Write Register Bit Assignments

CONFIGURATION MODE BIT PROGRAMMING

D = Databit

FUNCTION	WRITE ADDRESS (HEX)	DATA BITS BIT 3	BIT 2	BIT 1	BIT 0
V.21 ORG mode, Transmit low and and receive high band.	8	0	0	0	0
	9	X	D	0	1
	A	0	X	0	0/1
V.21 ANS mode, Transmit high band and receive low band.	8	0	0	1	0
	9	X	D	0	1
	A	0	X	0	0/1
V.23 mode, Primary channel transmit and reverse channel receive.	8	0	0	0	0
	9	0/1	D	0	1
	A	0	X	1	0/1
V.23 mode, Reverse channel transmit and primary channel receive.	8	0	0	1	0
	9	0/1	D	0	1
	A	0	X	1	0/1
Transmit calling tone and prepare to detect calling tone energy.	8	0	X	0	1
	9	X	X	0	1
	A	0	1	X	X
Transmit answer tone and prepare to detect calling tone energy.	8	0	X	1	1
	9	X	X	0	1
	A	0	1	X	X
Transmit calling tone and receive CPM.	8	0	X	0	1
	9	1	X	0	1
	A	1	1	X	X
V.21 Analog loop back in originate mode.	8	1	0	0	0
	9	X	D	0	1
	A	0	X	0	0/1
V.21 Analog loop back in answer mode.	8	1	0	1	0
	9	0	D	0	1
	A	0	X	0	0/1
V.23 Primary channel analog loop back.	8	1	0	0	0
	9	0/1	D	0	1
	A	0	X	1	0/1

Table 3. Configuration Mode Programming

V.23 Reverse channel analog loop back.	8 9 A	1 X 0	0 D X	1 0 1	0 1 0/1
Read register. Pin 11 is clamped to "Mark" in V.21 mode.	8 9 A	X X 0	1 X X	X 0 0	X X X
Read register. Pin 11 is clamped to "Mark" in V.23 mode.	8 9 A	X X 0	1 X X	X 0 1	X X X
Power down mode.	8 9 A	X X X	X X X	X 1 X	X X X

Table 3 (Cont'd) - Configuration Mode Programming

DTMF BIT PROGRAMMING

WRITE ADDRESS	DATA BITS				TONE FREQUENCY		
	BIT3	BIT 2	BIT 1	BIT0	LOW	HIGH	
8 9 A	0 1 0	0 X 0	0 0 X	1 1 X			
B	0	1	1	1	941	1336	(0)
B	0	0	0	0	697	1209	(1)
B	0	1	0	0	697	1336	(2)
B	1	0	0	0	697	1477	(3)
B	0	0	0	1	770	1209	(4)
B	0	1	0	1	770	1336	(5)
B	1	0	0	1	770	1477	(6)
B	0	0	1	0	852	1209	(7)
B	0	1	1	0	852	1336	(8)
B	1	0	1	0	852	1477	(9)
B	0	0	1	1	941	1209	(*)
B	1	0	1	1	941	1477	(#)
B	1	1	0	0	697	1633	(A)
B	1	1	0	1	770	1633	(B)
B	1	1	1	0	852	1633	(C)
B	1	1	1	1	941	1633	(D)

Table 4. DTMF Programming

TRANSMIT GAIN BIT PROGRAMMING

WRITE ADDRESS	DATA BITS BIT 3	BIT 2	BIT1	BIT 0	OUTPUT TRANSMIT LEVEL (dBm)
C	0	0	0	0	-18.0
C	0	0	0	1	-16.8
C	0	0	1	0	-15.6
C	0	0	1	1	-14.4
C	0	1	0	0	-13.2
C	0	1	0	1	-12.0
C	0	1	1	0	-10.8
C	0	1	1	1	-9.6
C	1	0	0	0	-8.4
C	1	0	0	1	-7.2
C	1	0	1	0	-6.0
C	1	0	1	1	-4.8
C	1	1	0	0	-3.6
C	1	1	0	1	-2.4
C	1	1	1	0	-1.2
C	1	1	1	1	0

Table 5. Transmit Gain Programming

APPLICATIONS INFORMATION

1) Analog (AGND) and digital (DGND) grounds should be routed separately to the power supply. They should be single-point connected at the supply in order to minimize higher digital currents from interfering with the more sensitive analog sections.

2) Power supply pins should bypass as close as possible to the IC with a 0.1 µF ceramic capacitor.

In the XR-2400 modem schematic, the XR-2321 is shown integrated into a V.22bis/V.22 modem with the XR-2400 chip set.(For schematic, call the factory). The XR-2321 provides the V.23 and V.21 functions resulting in a quad modem solution. If the user is upgrading from a XR-2100 (V.21 single-chip modem) design, the circuit can be retrofitted with the pin-for-pin compatible XR-2321 by replacing the XR-2100 and removing the jumper on pin 18 (FREQ out).